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Editorial

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With the start of the year 2021 we begin volume 37 of *JETTA* . Let me introduce two key individuals in our publisher's office. Maria Rhea Perilla-Bainto is a Team Leader, Journals Editorial Office (JEO). Rhea, as we call her, manages the flow of manuscripts through the web-based Editorial Manager system once it is submitted. Maria Cathelyn P. Mercullo is Production Coordinator, Journals Production. Cathelyn is responsible for the production of each issue after its table of contents becomes available. We have been fortunate to have their support. They deserve the strongest appreciation from our editors, authors, reviewers and readers.

We will miss Michel Renovell who is leaving our Editorial Board. We are grateful to him for many years of collaboration.

Peer reviewing has been an essential part of *JETTA*'s paper selection process. We acknowledge the contributions of our reviewers and thank them for devoting their expertise and time. A list of those who completed reviews for *JETTA* in 2020 appears in this issue.

This issue contains ten articles, including one *JETTA Letter*. The topics discussed are verification, hardware security, aging, analog and RF circuit testing, microfluidic device testing, single event upset in FPGA, machine intelligence for finding physical defects, and power supply noise suppression.

The first paper reviews pre-silicon verification methodology for systems involving hardware and software. Emphasis is on FPGA-based virtual prototyping, which allows verification of software before the hardware is completed. The authors are Farooq from Dhofar University, Salalah, Oman, and Mehrez from Sorbonne University, Paris, France.

Next, there are two papers on hardware security. Appearing as second and third in this issue, these papers address the security problems arising due to the isolation and lack of trust between the designer, manufacturer and supplier of a VLSI chip.

The second paper proposes a method for identifying an old device being recycled as new, or a counterfeit as it is sometimes referred to. The decision is made by assessing the age of the device from quiescent currents at two selected input vectors. A normalized difference of the two currents tends to minimize the effects of process variation on the decision. After simulating a 32 nm device the authors claim that devices used longer than six months can be isolated. Contributors are Chowdhury from University of Texas at Dallas, Richardson, TX, USA, and Guin, Singh and Agrawal from Auburn University, Auburn, AL, USA.

The third paper is on detection of a hardware Trojan on a chip. A popular term these days, hardware Trojan refers to the hardware maliciously added onto the chip somewhere in the supply chain to either alter the circuit function or steal data. The authors use a phenomenon they call "pulse killing" to detect such hardware. Basically, a gate cannot produce a pulse at its output if the pulse width is smaller than the gate delay, which depends upon the gate output capacitance. The proposed method propagates pulses through circuit paths likely to have increased capacitance due to Trojan hardware. The pulse width for a path is set to minimum that can pass through in the absence of any Trojan. The authors are Deyati, Muldrey and Chatterjee from Georgia Institute of Technology, Atlanta, GA, USA, and Singh from Auburn University, Auburn, AL, USA.

The fourth paper, presents a method to monitor aging in SRAM for maintaining reliable performance. A hardware monitor consists of a ring oscillator whose duty cycle changes with the age of the circuit. Simulation results illustrate the correlation between the duty cycle and various characteristics of storage cells and sense amplifiers. Authors are Dounavi, Sfikas, and Tsiatouhas from University of Ioannina, Ioannina, Greece.

In the fifth paper, supervised machine learning is used to diagnose parametric faults in a linear analog circuit. The weighted cosine K-Nearest Neighbor (K-NN) algorithm is claimed to classify faults with better than 95% accuracy.

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Authors are Pandaram, Rathnapriya and Manikandan from Coimbatore Institute of Technology, Coimbatore, India..

Sixth and seventh papers discuss testing of microfluidic devices.

The sixth paper provides a test procedure for a fluidic device with just five control pins. The device contains a two dimensional grid of electrodes, such that neighboring electrodes are controlled by separate pins. This requires a minimum of five control pins and is referred to as the control-5 structure. This paper is contributed by Huang, Xu and Zhang from Guilin University of Electronic Technology and Guangxi Key Laboratory of Automatic Detecting Technology and Instruments, Guilin, China.

The seventh paper gives an efficient method for test and diagnosis using multiple droplets. Both online and offline tests are devised, which can also find an alternative working path for fault tolerance in case of a fault. Authors are Ghosh from the Institute of Engineering and Management, Kolkata, India, and Roy and Giri from Indian Institute of Engineering Science and Technology, Shibpur, India.

Eighth paper develops an experimental method of fault injection in SRAM FPGA that emulates the single event upset (SEU) likely to occur in space applications. Contributors are Mengru Wang, Jinbo Wang, Jianmin Wang and Shan Zhou from Chinese Academy of Science, Beijing, China.

Ninth paper discusses the use of machine learning for preventing lithography hotspots in silicon manufacturing. Here convolutional neural networks are used to screen layout patterns to identify hotspot producing areas prior to chip manufacture. Authors are Xiao, Huang and Liu from University of Electronic Science and Technology of China, Chengdu, China.

The last item is a *JETTA Letter* by three authors from West Bengal, India, Mitra from Maulana Abul Kalam Azad University of Technology, Haringhata, Bhaumik from Jadavpur University, Kolkata, and Sarkar from Kalyani Government Engineering College, Kalyani. They provide a method to find an optimum distribution of decoupling capacitors on a system-on-chip to reduce power supply noise. Two of the computing algorithms used by the authors are symbiotic organism search (SOS) and particle swarm optimization (PSO).

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Editor-in-Chief