Editorial

Vishwani D. Agrawal [1]

With the start of the year 2020 we begin volume 36 of *JETTA*. It is my pleasure to welcome Mottaqiallah Taouil to the Editorial Board of *JETTA*. His picture and biography follow this editorial. Leaving the Board after several years of service are Kwang Ting (Tim) Cheng, Said Hamdioui, John Hayes, Michael Hsiao and Prabhat Mishra. We are grateful to them for their valuable contributions to the journal.

Peer reviewing is an essential part of *JETTA*'s paper selection process. We acknowledge the contributions of our reviewers and thank them for devoting their expertise and time. A list of those who completed reviews for *JETTA* in 2019 appears in this issue.

This issue contains ten articles, including one *JETTA Letter*. The topics discussed are reliability, hardware security, fault tolerance, reversible logic, system test, design for testability and approximate computing. Papers appearing as fourth and seventh are expanded versions of those presented at the *Twentieth IEEE Latin-American Test Symposium* (LATS) during March 11–13, 2019 in Santiago, Chile. *JETTA* Editor Leticia M. B. Poehls, who has a longstanding association with LATS, directed the peer reviewing of the journal versions of these papers. Parts of the ninth article were presented at the *Twenty-eighth IEEE North Atlantic Test Workshop* (NATW), Essex, Vermont, May 13–15, 2019. Tian Xia is the *JETTA* Editor responsible for that paper.

The first paper examines the failure probability of a system in which component reliabilities are correlated and components are not identical. Such cases, though common in real life, are often ignored in the technical literature. Authors are Banitabal, Ahari and Karbasian from Islamic Azad University, Najafabad, Isfahan, Iran.

The second paper proposes a method for detecting Trojan hardware in asynchronous circuits using a quiescent current transient (I_{ddt}) signature. Contributors are Guazzelli, Trindade, Guimarães, de Paiva Leite, Fesquet and Bastos from University of Grenoble Alpes and TIMA in Grenoble, France.

The third, fourth and fifth papers focus on issues related to fault tolerance.

The third paper examines various schemes of duplication and comparison for achieving fault tolerance. The authors demonstrate advantages of using approximate circuits for reducing the area, delay and power overheads. Researchers reporting this work are Deveautour, Virazel and Girard from LIRMM – University of Montpellier, CNRS, Montpellier, France, and Gherman from the Atomic Energy and Alternative Energies Commission (CEA), France.

Next, Serrano-Cases, Cuenca-Asensi and Martínez-Álvarez from University of Alicante, Spain, and Restrepo-Calle from Universidad Nacional de Colombia, Bogotá, Colombia, describe software based fault tolerance in processor operation. They use duplicated threads in multi-threaded execution as described in the fourth paper.

For the fifth paper the authors are Choudhury from New Alipore College, Kolkata, India and Sikdar from Indian Institute of Engineering Science and Technology, Shibpur, Howrah, India. Proposing an analytical model for the effectiveness of remapping based fault tolerance in a chip multiprocessor (CMP) cache they define two metrics, expected miss ratio (EMR) and expected latency ratio (ELR), which are functions of cell failure probability, block size and number of cores.

The sixth and seventh papers discuss system test.

The sixth paper enhances the swallow swarm optimization (SSO) procedure for selecting system tests. The basic idea introduced is to use a genetic algorithm (GA) to avoid the trap of a local optimum. Author are Yao, Zhu, Zhang and Wang from University of Chinese Academy of Sciences, Beijing, China.

The seventh paper describes generation of implementation independent tests for reduced instruction set computer (RISC) architecture. For the control part a high-level fault model leads to tests and for datapath pseudo-exhaustive tests are generated. Contributors of this work are Oyeniran, Ubar, Jenihhin and Raik from Tallinn University of Technology, Tallinn, Estonia.

✉ Vishwani D. Agrawal
  agrawvd@auburn.edu

[1] Auburn University, Auburn, AL 36849, USA

The eighth paper introduces multiple missing gate faults (MMGF) for generating tests for reversible logic circuits containing k-CNOT gates. A complete test set can be large but is minimized using integer linear programming (ILP). Authors are Handique and Deka from Indian Institute of Technology Guwahati (IITG), Guwahati, Assam, India, and Biswas from Indian Institute of Technology Bhilai, Chhattisgarh, India.

The ninth paper considers testing of circuits with logic built-in self-test (LBIST) that generates pseudo-random patterns. Since fault coverage of such patterns is often a concern, it is common to insert test points (TP) in the hardware. This paper explores the effectiveness of inversion type of TP. The results show improved coverages of stuck-at and delay faults compared to those by other types of TP. The authors are Roy, Millican and Agrawal from Auburn University, Auburn, Alabama and Stiene from Nvidia, Madison, Alabama.

A *JETTA Letter* is contributed to this issue by Patel, Garg and Rai from Thapar Institute of Engineering and Technology, Patiala, Punjab, India. They design carry lookahead adder (CLA) circuits that approximate sums within acceptable accuracy. The benefits are 70 to 80% reduction in area and a similar percentage decrease in energy consumption.