Journal of Electronic Testing (2018) 34:213–214
https://doi.org/10.1007/s10836-018-5731-z

Guest Editorial: Special Issue on Analog, Mixed-Signal, and RF Testing

Ke Huang[1] · **Manuel J. Barragan**[2]

Received: 20 April 2018 / Accepted: 20 April 2018 / Published online: 2 May 2018

Nowadays, complex nano-electronic systems are being developed and deployed for applications covering every facet of modern life. To interact with environment and users, integrated circuits need analog, mixed-signal, RF or MEMS blocks. However, as it happens with design automation, analog and mixed-signal test solutions are much less generic than their siblings from the digital world. Thus, even if these functions represent a small fraction of system silicon area, testing them accounts for a large portion of the overall manufacturing cost. Moreover, with the rise of safety-critical applications, reliability requirements are increasing and quality is nowadays a strong asset in competitive markets. Specification-based test at the production line cannot be considered enough any longer and testability, reliability, and robustness along the complete lifetime of the system are becoming a design specification. Undoubtedly, this is an opportunity for the analog and mixed-signal test community.

This special issue of *JETTA* brings together 12 excellent papers from academia and industry. These papers are expanded versions of preliminary work presented at the 22nd International Mixed-Signal Testing Workshop (IMSTW), held in Thessaloniki, Greece, 3–5 July, 2017, as well as new contributions beyond the workshop community through submissions from our open call-for-papers.

Accurate signal generation and measurements in analog/RF circuits are key factors for successfully implementing various test strategies ranging from Automatic Test Equipment (ATE) solutions to Built-In Self-Test (BIST) implementations. In the first paper, contributed by Sarson et al., the authors demonstrate a phase switching algorithm for improving the performances of an Arbitrary Waveform Generator (AWG). The technique allows the use of a low-cost tester resource to test Intermodulation Distortion (IMD) with a higher dynamic range than what was previously possible. The second paper by Sarson et al. proposes a method for measuring group delay of frequency down-converter devices using a chirped RF modulated signal. The group delay test is implemented based on base-band domain analysis. Group delay measurements in an RF mixer and pre/post down convert RF/IF filters are demonstrated. The third paper by Li et al. deals with non-linearity issues and linear distortion produced by RF power amplifiers (PAs). An inverse autoregressive moving-average (ARMA) model is proposed to linearize the RF PAs based on a method of digital predistortion (DPD). The proposed model is applied to several typical protocols in the Internet of Things (IoT) applications including Bluetooth, Wi-Fi, and LTE-M. The fourth paper by Malloug et al. develops new harmonic cancellation strategies with the goal of simplifying the practical on-chip implementation of the scaling weights in accurate sinusoidal signal generators, which are usually a key limiting factor for the effectiveness of the harmonic cancellation. The feasibility of the proposed harmonic cancellation strategies is demonstrated with statistical behavioral simulation of a sinusoidal signal generator. In the fifth paper by David-Grignot et al., the authors present an analytic study of various potential digital-based solutions for on-chip sine-wave signal generation in the context of biosensor and BIST applications. The authors show that the technique based on setting the phase shifts and various amplitude values of the square-wave signals is the most efficient approach and they propose a method for selecting the optimal square-wave signal parameters to cancel low-order harmonics of the generated signal.

The next two papers focus on hardware security. The sixth paper, by Naija et al., proposes a new full-fledged high frequency tag architecture in Radio Frequency IDentification (RFID) devices for enhancing the safety features in mutual authentication protocol. The implementation is

✉ Ke Huang
khuang@sdsu.edu

Manuel J. Barragan
Manuel.Barragan@univ-grenoble-alpes.fr

[1] Department of Electrical and Computer Engineering, San Diego State University, San Diego, CA 92182, USA

[2] Université Grenoble Alpes, CNRS, Grenoble INP, TIMA, 38000, Grenoble, France

achieved using a Field-Programmable Gate Array (FPGA) platform. Security analysis against various attacks including electromagnetic/desynchronization attack is shown. The hardware implementation of these security enhancement techniques shows a low overhead as compared to previous solutions. Hardware Trojan detection problem is tackled in the seventh paper by Zhang et al. In particular, a golden-free detection method for detecting hardware Trojans in processors is proposed by exploiting the bit power consistency. The methodology is successfully demonstrated on an FPGA chip with inserted hardware Trojans.

Alternate test in analog/RF circuits and its BIST implementations are discussed in the next three papers. The eighth paper, by Lee et al., proposes a time-domain digital intensive built-in tester for analog circuits. The tester allows characterizations of AC response and DC gain for various analog circuits having a low-pass frequency characteristic. The tester was fabricated in 65 nm standard CMOS process with small area overhead of 0.026 mm^2. The ninth paper, by Ahcene et al., proposes a new technique for overcoming the need of generating a large set of Monte Carlo samples to accurately estimate Test Escape (TE) and Yield Loss (YL) in analog/RF alternate test applications. The approach only requires a small number of simulations to determine the region separating the process parameters generating pass and fail circuits based on machine learning classifiers. The tenth paper, by Huang et al., proposes an on-chip implementation of the learning modules in analog/RF BIST for alternate test applications. The authors show that model refinement and dynamic adaption of the BIST structure can be realized in real time using the proposed on-chip implementation. Effectiveness of the approach is demonstrated using an RF Low Noise Amplifier (LNA) and its BIST implementation.

Finally, reliability analysis for state-of-the-art devices are discussed in the last two papers. The eleventh paper by Dibaj et al. deals with Gate Oxide Short (GOS) defect in Fin Field Effect Transistors (FinFETs), which is one of the dominant defects that has significant impact on circuit reliability. A GOS defect model for FinFETs is presented by introducing the defect as a pinhole in the gate oxide of a triangular fin shape structure. The model is demonstrated by 3D Sentaurus TCAD simulation for circuit-level fault modeling to generate more realistic test patterns. Reliability testing of 3D-printed electromechanical scanning devices is presented in the twelfth paper by Ferhanoglu et al. Reliability tests and analysis of 3D-printed actuators are performed by monitoring the deviations in the fundamental mechanical resonance, scan-line, and the quality factor. A total of 9 scanning devices having 10 mm $\times$ 10 mm die size are tested for analyzing deviations in the selected test parameters.

Acknowledgments We would like to thank all authors and reviewers for their contributions to this special issue. Without their work and support, this issue would not have been possible. Special thanks are due to Prof. Vishwani Agrawal, Editor-in-Chief, for his invaluable help and guidance. We hope you enjoy reading this special issue and find it interesting and useful.

Ke Huang received the B.S. and M.S. degrees in electrical engineering from Joseph Fourier University (now Grenoble Alps University), Grenoble, France, in 2006 and 2008, respectively, and the Ph.D. degree in electrical engineering from the University of Grenoble (now Grenoble Alps University), Grenoble, France, in 2011. He was a Postdoctoral Research Associate at the University of Texas at Dallas, Richardson, TX, USA, from 2012 to 2014. In 2014, he joined the Department of Electrical and Computer Engineering at San Diego State University, San Diego, CA, USA, where he is now an Assistant Professor. His research focuses on applications of machine learning in testing analog/RF circuits, hardware security, and computer-aided design of integrated circuits (ICs).

He served as the Program Co-Chair of the 2017 IEEE International Mixed-Signal Testing Workshop. He was a recipient of the Best Paper Award from the 2015 IEEE VLSI Test Symposium (VTS'15), and a recipient of the Best Paper Award from the 2013 Design Automation and Test in Europe (DATE'13) Conference.

Manuel J. Barragan received a degree in Physics in 2003 and a Ph.D. in Microelectronics in 2009, both from the University of Seville, Spain. He is currently a researcher with the French National Research Council (CNRS) at TIMA Laboratory, Grenoble, France. His research is focused on the topics of test and design for testability of analog, mixed-signal, and RF systems. He served as the Program Chair of the 2016 and 2017 IEEE International Mixed-Signal Testing Workshop. He currently serves in the Technical Program Committee of the Design, Automation, and Test in Europe (DATE) Conference, IEEE European Test Symposium, and IEEE VLSI Test Symposium. His Ph.D. research won a Silver Leaf Award at the IEEE PRIME conference in 2009 and, in 2011, his work was selected for inclusion in the 20th Anniversary Compendium of Most Influential Papers from the IEEE Asian Test Symposium. He received the Best Special Session Award in the 2015 IEEE VLSI Test Symposium.