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Editorial

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In the last issue (December 2016), we announced the 2015 *JETTA-TTTC Best Paper Award*. TTTC Board President, Yervant Zorian presented the award at the International Test Conference in Fort Worth, Texas on November 17. The photograph shows (left to right) Yervant Zorian and two of the authors, Barry Muldrey Jr. and Abhijit Chatterjee, who received the award on behalf of all authors of the paper, "Low Cost Sparse Multiband Signal Characterization Using Asynchronous Multi-Rate Sampling: Algorithms and Hardware," *Journal of Electronic Testing: Theory and Applications*, Volume 31, Number 1, pp. 85–98, February 2015.

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This issue contains eight papers and two letters. The topics discussed are power constrained testing, test scheduling, soft error tolerance, multiprocessor reliability, fault tolerance, hardware security, approximate computing and RF circuit analysis. The third, fifth and sixth papers, initially presented at the Seventeenth Latin American Test Symposium, Foz do Iguaçu, Brazil, during April 6–8, 2016, were rewritten in journal versions by the authors and *JETTA* Editor, Leticia M. B. Poehls conducted their peer reviews.

The first paper presents a test cost model for multicore devices. This allows optimization of the test schedule by simulated annealing. Authors are SenGupta, Nikolov and Larsson from Lund University, Lund, Sweden and Ingelsson of Semcon, Linköping, Sweden.

Next, three papers deal with soft error effects. The first in these papers proposes a method for hardening a minimal set of gates for a given soft error tolerance. Authors are Wali, Deveveautour, Virazel, Bosio and Girard from LIRMM, University of Montpellier, France and Sonza Reorda from Politecnico di Torino, Torino, Italy.

The second paper in the soft error group provides a compact model for simulating radiation induced errors. This research is contributed by Petrosyants, Sambursky, Kharitonov and Lvov from National Research University, Higher School of Economics, Moscow, Russia.

The third soft error paper addresses the problem of dependability versus performance trade-off for various data compression algorithms when used in high radiation environment. The authors are Avramenko, Sonza Reorda and Violante from Politecnico di Torino, Torino, Italy and Fey from German Aerospace Center (DLR), Bremen, Germany.

In the fifth paper of this issue, Esposito and Violante of Politecnico di Torino, Torino, Italy consider the reliability of multi-core processors. Their proposal combines some hardware redundancy, watchdog processor and timer, voter logic and software redundancy.

The next article focuses on the problem of finding application specific redundant faults of hardware. Authors are Bartsch, Villarraga, Stoffel and Kunz from University of Kaiserslautern, Germany. The presented solution relies on a program netlist that actually is a hardware-dependent software model of the system. This netlist allows the use of the standard automatic test pattern generation (ATPG) tools for identifying redundant faults.

Hardware security is the topic of the seventh and eighth papers. First, Nasr and Abdulmageed from Al-Azhar University, Cairo, Egypt discuss the development of AHTDT, an automatic hardware Trojan detection and description tool. This tool analyzes the physical layout to identify any hidden Trojan (malicious) hardware. The second paper, authored by Hoque and Bhunia from University of Florida, Gainesville, FL, USA, Narasimhan and Wang from Case Western Reserve University, Cleveland, OH, USA and Mal-Sarkar from Cleveland State University, Cleveland, OH, USA, examines side-channel analysis methods for Trojan detection. They point to the inadequacy of using a golden model for a system that is affected by process variation. The proposed method, termed as TeSR or temporal self-referencing approach, compares specified signatures of the chip at two different time windows to detect Trojan hardware.

In the first letter, Jothin of KGiSL Institute of Technology, Coimbatore, India and Vasanthanayaki of Government College of Technology, Coimbatore, India present their design of an approximate computing adder for image enhancement application. They incorporate accuracy adjustment logic, still claiming high speed and energy efficiency.

The second letter is contributed by Gu, Fu, Na, Zhang and Ma from Tianjin University, Tianjin, China. They discuss automated modeling techniques that help analyze effects of electromigration on the reliability of interconnects in radio frequency (RF) power amplifiers.

JETTA Editorial Board held its annual meeting at Fort Worth, Texas on November 16, 2016. This photograph taken at the meeting shows attending editors (left to right) Adit Singh, Haralampos Stratigopoulos, Xiaowei Li, Jacob Abraham, Suraj Sindia, Hans-Joachim Wunderlich, Yervant Zorian, Krishnendu Chakrabarty, Mehdi Tahoori, Charles Glaser (Executive Editor, Springer), Rubin Parekhji, Mark

Tehranipoor, Prathima Agrawal (guest), Hans Manhaeve, Cheng-Wen Wu, Salvador Mir, Vishwani Agrawal, Said Hamdioui, Kuen-Jong Lee, Yiorgos Makris, Magdy Abadir, Stephen Sunter, and 2015 *JETTA-TTTC Best Paper Award* winners Abhijit Chatterjee and Barry Muldrey Jr. Not in the picture, *JETTA* Editor Enamul Amyeen was also present.