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Editorial

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We have selected a paper for the *2014 JETTA-TTTC Best Paper Award*. The award committee appointed by the Test Technology Technical Council (TTTC) Chair, Michael Nicolaidis, was the same as in 2013 and consisted of Matteo Sonza Reorda (Chair), Vishwani Agrawal, Salvador Mir, Adit Singh and Xiaoqing Wen. We congratulate the winning authors, Rafal Baranowski, Michael A. Kochte and Hans-Joachim Wunderlich. Their paper, "Access Port Protection for Reconfigurable Scan Networks," appeared in *JETTA*, Volume 30, Number 6, pages 711–723, December 2014. See the award page in this issue. The award will be presented this month at the International Test Conference in Anaheim, California.

This issue of *JETTA* contains seven papers and one letter. The topics covered are VLSI yield, analog and radio frequency circuit testing, 3D stacked integrated circuit testing, hardware security and soft errors in memories.

The first paper discusses a yield enhancement methodology. Authors, Hsieh, Wang, Kuo, Huang and Chih of National Sun Yat-sen University, Kaohsiung, Taiwan, pursue the idea that certain faults that merely degrade performance leaving the function otherwise intact can be tolerated in the sense of producing usable devices.

The next four papers focus on analog and RF circuit testing. The first of these provides digital testing methods for measuring phase noise or jitter. Depending upon the available oversampling rate as many as 32 devices can be tested in parallel. Authors are David-Grignot, Azaïs and Latorre of Université Montpellier, France and Lefevre from NXP Semiconductors in France.

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The next paper in the analog and RF group explores the possibility that the occurrence of a fault may not cause an instant failure but in fact reduce the remaining useful life (RUL) of the circuit. The new test methodology attempts to predict the impending failures as circuit components degrade. This research is contributed by Hu, Xiao, Zhang, Song and Yang from Air Force Engineering University in Shanxi Xi'an, China.

The third analog and RF paper addresses minimization of specification tests by preserving the defect level. The method relies on Monte Carlo simulation and integer linear programming. Given that test time and cost are serious considerations, demonstration of 50 % reduction seems significant. Authors are Sindia of Intel Corporation, Hillsboro, Oregon and Agrawal of Auburn University in Alabama. An earlier version of this work was presented at the 15th IEEE Latin American Test Workshop, Fortaleza, Brazil, 12–15 March, 2014 and the review process of the present version for *JETTA* was conducted by Leticia M. Bolzani Pöhls as Guest Editor.

The fourth paper on analog circuit test gives a dictionary based diagnosis method for nonlinear circuits. Contributors are Tadeusiewicz, Kuczyński and Hałgas from Lodz University of Technology, Łódź, Poland.

Next, we have a paper on 3D stacked integrated circuits authored by Aghaee, Peng and Eles from Linkoping University in Sweden. They rearrange tests to cause accelerated temperature cycling during test. Thus, many early life failures can be isolated without the need for expensive life testing.

Hardware security is discussed in a paper by Gören, Gürsoy and Yildiz of Yeditepe University, Istanbul, Turkey. The authors use FPGA based fault emulation to determine sites for fault injection elements (FIE) in a circuit with logic locking. Such a design would function correctly only when a specified key input is applied to deactivate FIEs.

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We end this issue with a *Letter* by Li and Ma from Dalhousie University, Halifax, Canada, Li, Wang, Liu, Newton and Chen from University of Saskatchewan, Saskatoon, Canada, and Wu from China University of Petroleum, Qingdao, China. They present a layout for a six-transistor SRAM cell with increased tolerance for single event upsets.

The annual meeting of *JETTA* Editorial Board is scheduled in Anaheim, California for October 7, 2015.