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Editorial

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I am pleased to announce seven additions to the editorial board of *JETTA*. New editors are Kuen-Jong Lee, Yiorgos Makris, Salvador Mir, Subhasish Mitra, Ozgur Sinanoglu, Xiaoqing Wen and Tian Xia. Their pictures and biographies appear in this issue.

Retiring from the board are Tony Ambler, Karim Arabi and Peter Maxwell. Each has served the journal for several years and we gratefully acknowledge their contributions.

Peer reviews are an essential part of *JETTA*'s editorial policy. We acknowledge the contributions of our reviewers and thank them for devoting their expertise and time to serve the profession. A list of those who completed reviews for *JETTA* in 2014 appears in this issue.

This issue contains ten papers and one *Letter*. The topics covered are security, delay test, test compression, power constrained testing, analog and RF testing, power supply noise and reliability testing. The third, sixth, seventh and ninth papers are derived from the program of the Twenty-third *IEEE North-American Test Workshop* (NATW) of 2014. Guest Editors Themistoklis Haniotakis and Tian Xia deserve credit for editing these papers.

The first paper is on hardware security and is authored by Kelly, Zhang and Tehranipoor from University of Connecticut, Storrs, Connecticut, USA and Ferraiuolo from Cornell University in USA. They implement a ring oscillator network (RON) to monitor the power supply network, which is supposed to be affected by malicious Trojan activity. Low voltage testing (LVT) and variable source resistance testing (VSRT) are investigated as methods to enhance the sensitivity of the monitor.

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The second and third papers address delay testing. T. Liu and Y. Liu from Hangzhou Dianzi University, Hangzhou, China, and Zhou and Cai from Hunan University, Changsha, China demonstrate that certain transition faults can only be activated by signal hazards. They provide an algorithm for generating hazard-based detection tests for such faults. Gao, Zhang, Chakraborty and Walker from Texas A&M University, College Station, Texas, USA and Pokharel from NVIDIA Corporation, Santa Clara, California, USA examine testing of path delay faults involving non-scan cells and functional memory arrays. Their tests contain both slow clock and at-speed clock vectors.

In the fourth paper, authors Yuan, Guo, Mei and Song from Beijing University of Technology, Beijing, China and Sun from Tsinghua University, Beijing, China combine the don't care handling and coding techniques for test data compression and reduction of test time and power consumption.

Next, we have four articles on analog and radio frequency test. First, Zhao and He from Beihang University, Beijing, China use a probabilistic measure to select test points for distinguishing between faults. Second, Farid Rahman, Pengpeng, T. Wang and G. Wang from University of South Carolina, Columbia, South Carolina, USA and Xia from University of Vermont, Burlington, Vermont, USA provide a method for on-wafer measurements in frequency range 1 to 67 GHz. Third, Metwally, L'Esperance and Xia from University of Vermont, Burlington, Vermont, USA use a technique known as orthogonal frequency division multiplexing (OFDM) for testing of radar. The fourth paper in this group is authored by Tzou, Bhatta, Muldrey Jr., Moon, Wang, Choi and Chatterjee from Georgia Institute of Technology, Atlanta, Georgia, USA. They develop a sub-Nyquist rate sampling method for

characterization of radio frequency signals. Built-in hardware is used and emphasis is on reducing the cost of the overhead.

The ninth paper aims at post-silicon validation with respect to the power supply noise (PSN). Authors, Zhang, Gao and Walker from Texas A&M University, College Station, Texas, USA generate patterns to activate various levels of PSN while testing long delay timing paths of the circuit.

The tenth paper, by Vock, Escalona and Turner from University of Ulster in United Kingdom, describes case studies on test programming and automatic test equipment (ATE) applications related to stress testing for reliability assessment of a device under test.

A *JETTA Letter* is contributed by Yu and He from Hunan University, Changsha, China. They compute sensitivities of performance parameters of an analog circuit with respect to deviations in component values. The analysis leads to multivariate nonlinear equations, which are solved by a Newton–Raphson procedure.