Editorial

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The International Workshop on Microprocessor Test and Verification (MTV) is a forum for discussing the design and test of processor and system-on-chip (SoC) devices. This issue of *JETTA*, for which we sent out a call for papers at the 13th MTV (Austin, Texas, December 2012), is a special issue on the workshop theme. Guest editors, Sandip Ray, Jay Bhadra, Magdy Abadir and Li-C Wang, deserve our gratitude for initiating this effort and bringing it to completion. Their guest editorial describes the contents, which, I am certain you will find to be of interest. To discuss continuing advances, the 14th MTV is scheduled in Austin during December 11 through 13, 2013.

Implicit in the present theme are the topics of validation, verification and test. *Test* is related to the process of manufacturing. From the same design, a product is often manufactured in large quantities. Each individual product can have fabrication defects that must be detected through test and fixed, if necessary. Having said that, I found myself at a loss while trying to define *validation* and *verification*?

As is usual these days, I searched through the internet. The "Verification and validation (software)" page of *Wikipedia* differentiates between the two terms by quoting from Barry Boehm's book (*Software Risk Management*, IEEE Computer Society Press, 1989):

- Validation: Are we building the right product?
- Verification: Are we building the product right?

Answering both questions in affirmative will validate and verify whatever we are doing. Suppose, a user needs a transport with a speed of 500 miles per hour to carry passengers through distances up to 1,000 miles, then a design of an automobile cannot be validated. Given that an aircraft will provide a valid design, verification will involve conforming to user's specifications on speed, number of passengers, distance of travel, fuel efficiency, etc. Although the *Wikipedia* quote refers to software and my example is a mechanical system, I think the concepts are applicable to any product or system, including microprocessor or system-on-chip.

The list of topics on the call for papers for this issue included: validation of microprocessors and SoCs, experiences on test and verification of high performance processors and SoCs, high-level test generation for functional verification, emulation techniques, silicon debugging, low power verification, formal techniques and their applications, verification coverage, test generation at the transistor level, electronic system level (ESL) methodology, virtual platforms, software verification, circuit level verification, switch-level circuit modeling, timing verification techniques, design error models, design for testability or verifiability, and optimizing SAT procedures for application to testing and formal verification. Evidently, this is far too long a list for a single issue and I hope we will revisit the area in the near future.

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