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Editorial

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The first three papers in this issue complete our *Special Issue on Defect and Fault Tolerance*, put together by Guest Editors, Prashant Joshi and Massimo Violante. The complete set contains 16 papers, of which the first 13 appeared in the last issue of *JETTA* (volume 29, number 3, June 2013). That issue also contains a Guest Editorial.

The first paper presents an analysis of single event upsets in SRAM-based FPGA. Good accuracy is shown and the analysis is applied to determine MTBF (mean time between failures) versus neutron flux for various architectures. Authors are Thibeault, Hobeika and Tazi from Ecole de Technologie Superieure, Montreal, QC, Canada, Hariri of CMC Microsystems, Kingston, ON, Canada, and Hasan, Savaria and Audet from Ecole Polytechnique de Montreal, Montreal, QC, Canada.

In the second paper, Sindia and Agrawal from Auburn University, Auburn, AL, USA, train a neural network for avoiding errors in video processing on an array of processing elements (PE) in which some PEs may be faulty. PEs found to be fault free are reused to complete the computation in the absence of redundant PEs in this scheme.

The third paper, authored by Neishaburi and Zilic of McGill University, Montreal, QC, Canada, proposes dynamic virtual channel allocation for reliable communication in a network on chip (NoC). The method emphasizes low power and latency.

The remaining papers are regular submissions to *JETTA*. First two papers discuss thermal effects in system on chip (SoC) devices. Aghaee, Peng and Eles of Linkoping University, Linkoping, Sweden, discuss dynamic scheduling of SoC tests by monitoring the temperature distribution obtained from embedded sensors. Another paper, by Schor, Bacivarov, Yang and Thiele of ETH Zurich, Switzerland, develops a thermal model considering the neighborhood heat exchange effects in a multiprocessor system on chip (MPSoC). The model is then used for task assignment on the MPSoC. This paper was originally presented at 2012 *Latin American Test Workshop* and was reprocessed for *JETTA* by Guest Editor Raoul Velazco.

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Next two papers discuss error tolerant storage elements. Asli and Shirinzadeh, of University of Guilan, Rasht, Iran, use time redundancy to design a radiation hardened latch. Their 45nm CMOS design also shows tolerance to process, voltage and temperature variations. Namba, Katagiri and Ito, of Chiba University, Japan, use two dual edge triggered latches and a C-element to generate the output, while a window generator and a simple four-transistor error detector provides an error signal.

Analog circuit testing is featured in two papers appearing next. Ao, Shi, Zhang and Li of University of Electronic Science and Technology of China, Chengdu, China, develop an analysis for the ratio of normal random variables with an application to the diagnosis of linear circuits. A previously defined slope fault model (SFM) is used. From the same institution in China, Li, Xian, Long and Wang present a technique for prognosis of filters. During the lifetime of a device this procedure predicts the remaining time for which useful performance can be guaranteed.

Online Test is discussed in the next two papers. Wu, Liu, Liu, Guo and Sun of National University of Defense Technology, Changsha, China, present a method for concurrent test. Inputs to the system are compared with stored test vectors and whenever a match occurs the system output is compared with the expected test response. This work aims at minimizing the logic overhead of test logic. In the next paper, Gherman, Evain and Bonhomme, from Commissariat à l'Energie Atomique, France, investigate correction of more data bit errors than is normally considered possible with the available error correction bits. This is done at the cost of a small increase in decoder latency. This paper is from 2012 *European Test Symposium* and was processed for *JETTA* by Guest Editor Massimo Violante.

The final contribution is a *JETTA Letter* authored by Ren, Chen and Wang of University of Saskatchewan, Saskatoon, Canada, Wen and Wong from Cisco Systems, San Jose, CA, USA, van Vonno from Intersil, Milpitas, CA, USA, and Shi, Gao and Guo from China Institute of Atomic Energy, Beijing, China. They describe experimental work on single event transients using pulsed laser and heavy ions.