J Electron Test (2013) 29:1–2
DOI 10.1007/s10836-013-5353-4

Editorial

Vishwani D. Agrawal

Received: 29 January 2013 / Accepted: 29 January 2013 / Published online: 10 February 2013
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To begin 2013 and the volume 29 of *JETTA*, I should address several organizational items. We are adding two new editors to the editorial board of *JETTA*. They are Stephen K. Sunter of Mentor Graphics (Canada) and Theocharis (Theo) Theocharides of University of Cyprus. Their pictures and biographies are included in this issue. Steve is a well-known expert in the area of analog and mixed-signal circuit testing. Theo is the new TTTC Newsletter Editor replacing Partha Pande on the Editorial Board.

Retiring from the board are Partha Pande, Sharad Seth and Charles Stroud. Each has served the journal for several years and we are grateful to them for their service.

A list of reviewers who conducted reviews for *JETTA* in 2012 appears in this issue. We acknowledge their contribution to the journal and thank them for devoting their expertise and time to serve the profession.

This issue contains eight papers and one *Letter*. The topics covered are system test, delay test, asynchronous FIFO test, power constrained testing, single event upset, analog circuit testing, and scan testing. The first paper is derived from the program of the *IEEE Latin-American Test Workshop* (LATW) of 2011 and the third paper is from the *IEEE European Test Symposium* (ETS) of 2011. Guest Editors, Fernanda Kastensmidt and Cecilia Metra deserve credit for the editing of these papers. Two other papers, appearing as sixth and eighth papers, are from the LATW of 2012 and were edited by Guest Editor Leticia Maria Bolzani Pohls.

System Test is the topic of the first two papers. The authors of the first paper are from four universities in Brazil. They are Colanzi (UEM), Assunção and Vergilio (UFPR), de Freitas Guilhermino Trindade (UENP) and Zorzo (UNIARP). They derive system tests by examining software products with common features. The second paper, authored by Mashkov, Barilla and Simr of University J. E. Purkine, Usti nad Labem, Czech Republic, considers a multicore processor system in which the processors test each other in a random order. A Petri net model is used to analyze various self-test strategies for the system.

The next paper uses n-detect tests for sensitizing long paths to detect small delay defects (SDD). The quality of the tests is determined by identifying critical transition delay faults for which the time slack is less than a specified threshold. The authors are Bao and Tehranipoor of University of Connecticut, USA, Peng and Winemberg from Freescale Semiconductor, Austin, Texas, USA, Yilmaz from Nvidia Corporation, Santa Clara, California, USA, and Chakrabarty of Duke University, Durham, North Carolina, USA.

The next paper presents a method for testing two-D-flip-flop synchronizers of an asynchronous first-in-first-out (FIFO) interface. Timing and clock signals are generated and calibrated before they are used to test the FIFO. The article is contributed by Kim and Jone of University of Cincinnati, Ohio, USA, Wang from SynTest Technologies, Inc., Sunnyvale, California, USA, and Wu of The Chinese University of Hong Kong, Shattin, Hong Kong.

The authors of the next paper are Almukhaizim and Bunian of Kuwait University, Kuwait City, Kuwait and Sinanoglu of New York University - Abu Dhabi, United Arab Emirates. They devise an online testing procedure in which the concurrent error detection mechanism is disabled or enabled depending on the availability of power budget.

In the next paper, Mansour and Velazco of TIMA Labs, Grenoble, France, evaluate the error rate of a processor due to single event upsets (SEU). Faults are injected in the VHDL model and evaluation is based on simulation.

Analog circuit test is discussed in the next paper by Han, Wang, Tian and Zhang from Chengdu, Sichuan, China. The authors adopt the concept of *Mahalanobis Distance* from statistics (P. C. Mahalanobis, "On the Generalized Distance in Statistics," *Proceedings of National Institute of Science*

V. D. Agrawal (✉)
Department of ECE, Auburn University, 200 Broun Hall,
Auburn, AL 36849, USA
e-mail: vagrawal@eng.auburn.edu

(India), volume 12, pp. 49–55, 1936). Mahalanobis distance is a measure of similarity (or difference) between two statistical multivariate samples and is analogous to the Euclidean distance between two deterministic vectors.

In the next paper, Sinanoglu of New York University - Abu Dhabi, United Arab Emirates and Agrawal of Auburn University, Auburn, Alabama, USA, apply *retiming* to eliminate the performance penalty of scan testing. Retiming is a function preserving transformation that allows moving flip-flops across a block of combinational logic (C. E. Leiserson and J. B. Saxe, "Retiming Synchronous Circuitry," *Algorithmica*, volume 6, pp. 5–35, 1991). The authors use retiming to move the scan multiplexers and fanouts from critical paths across flip-flops and into the adjoining non-critical paths.

The single *JETTA Letter* of this issue is contributed by Li and Xie of University of Electronic Science and Technology of China, Chengdu, China. They invoke the principle of maximum entropy in which the entropy (a measure of uncertainty or information) in the observable output during test is maximized.