J Electron Test (2009) 25:285
DOI 10.1007/s10836-009-5120-8

Editorial

Vishwani D. Agrawal

Published online: 23 October 2009

The first paper in this issue contributes to formal verification methods. The authors, Jenihhin, Raik, Chepurov and Ubar from Tallinn University of Technology in Estonia, propose a temporal extension of the high-level decision diagram (HLDD). They then use an HLDD simulator for assertion checking.

In the next paper Wegener, Mattes, Kirmser, Demmerle and Sattler from Infineon Technologies AG, Germany, investigate the testing of a mixed-signal core embedded in a system-on-chip (SoC). They use on-chip test resources in a functional mode such that a core under test receives stimuli from other cores on the chip that also examine the test response. Advantages are reduced interaction with external tester and a possibility for parallel testing of SoCs.

The third paper also researches the SoC test scenario. Authors, Kupp and Makris of Yale University, USA, Drineas of Rensselaer Polytechnic Institute, USA, and Slamani of IBM, USA, provide methods to estimate the confidence level in specification testing of a radio frequency (RF) component by other non-RF components on the same chip.

The three papers I mentioned above include research originally reported at the *Thirteenth IEEE European Test Symposium* held at Verbania, Italy during May 25–29, 2008. I am thankful to Cecilia Metra of our editorial board to carry out the additional responsibility of serving as guest editor for these papers.

V. D. Agrawal (✉)
ECE Department, Auburn University,
200 Broun Hall,
Auburn, AL 36849, USA
e-mail: vagrawal@eng.auburn.edu

Continuing with contents of this issue, the fourth paper considers minimization of power consumption of scan test. The authors are Wu, Hu and Huang of National Taiwan University in Taiwan. Their technique fills don't care bits considering both shift activity and capture activity.

Next, there are three *JETTA Letters*. The first is authored by Nan, Wang and Li of Hunan University, China, Yang of Hunan University of Technology, China, and Ma of China University of Mining and Technology, China. They present a new method to estimate the deterministic and random components of jitter in a periodic signal.

The second *Letter* is authored by Pulukuri and Stroud of Auburn University, USA. They investigate complete tests for adders under uncertainty about their architecture and hardware implementation. The objective is to provide built-in self-test for adders of an embedded digital signal processor core on a Xilinx Vertex-4 field programmable gate array chip.

The third *Letter*, the final contribution in this issue, is authored by Kim of Dankook University, South Korea and Saluja of University of Wisconsin-Madison, USA. They introduce a novel design of a core wrapper that supports hierarchy in SoC design.

Although this is Volume 25, with this issue we complete 20 years of publication of *JETTA*. A discrepancy in volume numbers exists because in the early years we published multiple volumes. This volume contains one special issue on "Defect and Fault Tolerance," guest edited by Cristiana Bolchini and Yong-Bin Kim. For 2010, two special issues are in the works, "Mixed-Signal Test" with Karim Arabi as guest editor and "High-Level Design Validation and Test" with Prabhat Mishra as guest editor. Another special issue on "Defect and Fault Tolerance" with Spyros Tragoudas as guest editor is being planned.