



# Device design and optimization of CNTFETs for high-frequency applications

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## Abstract

Carbon nanotube (CNT) field-effect transistors (FETs) have recently reached high-frequency (HF) performance similar to that of silicon RF-CMOS at the same gate length despite a tube density and current per tube that are far from the physical limits and suboptimal device architecture. This work reports on an investigation of the optimal device design for practical HF applications in terms of cut-off frequencies, power gain, and linearity. Different fundamental designs in the gate contact arrangement are considered based on a 3D device simulation of both CNTs and contacts. First, unit cells with a single CNT and minimal contact sizes are compared. The resulting simulation data are then extended toward a structure with two gate fingers and realistic contact sizes. Corresponding parasitic capacitances, as well as series and contact resistances, have been included for obtaining realistic characteristics and figures of merit that can be used for comparison with corresponding silicon RF MOSFETs. Finally, a sensitivity analysis of the device architecture with the highest performance is performed in order to find the optimal device design space.

**Keywords** Carbon nanotube field-effect transistor · Compact modeling · CNT device simulation · Device optimization · High-frequency

## 1 Introduction

The development of field-effect transistors (FETs) built with single-walled carbon nanotubes (CNTs) as channel material has recently made significant progress. On the digital application side, three-dimensional (3D) integration of CNT-based memory and logic gates for building a microprocessor have been demonstrated [1, 2]. On the analog high-frequency (HF) side, extrinsic cut-off frequencies around 100 GHz have recently been demonstrated for CNTFETs with 160 nm channel and 110 nm gate length [3]. This HF performance is now at the same level as that of RF CMOS with the same channel length, despite an average density of just 50 tubes/ $\mu\text{m}$  and an average current per CNT of only 5  $\mu\text{A}$ . These results show for the first time the great potential of CNTFET technology for achieving significantly higher

HF performance than RF CMOS for the same lithography node and for co-integration with digital CMOS.

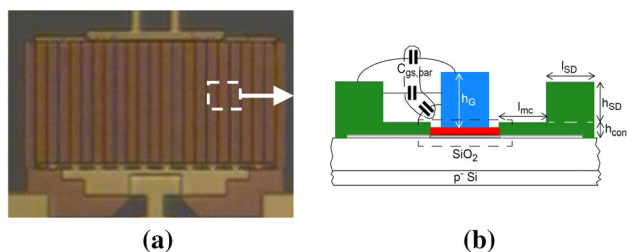
The CNTFETs in [3] are based on a T-shaped top gate structure, which may not be the best option for achieving maximum speed since the tall gate and especially its metal overlaps over the source and drain contact cause significant additional parasitic capacitances. Therefore, the main goal of this work is the investigation of different device design alternatives and the identification of the best option in terms of HF performance, including cut-off frequencies, power gain and linearity. The analysis here is based on three-dimensional (3D) device simulation of a CNTFET structure, in which the tubes are represented by hollow cylinders that are embedded in a realistic 3D contacting scheme. This allows to capture the effects of the competing screening fields of the contacts in their different arrangements on tube potential and thus on drain current and charge.

Generally, for achieving sufficient output power and impedance matching in a 50  $\Omega$  system, transistors with many contact fingers and up to thousands of CNTs are required [4–6]. The layout of a typical HF CNTFET is shown in Fig. 1a. Since such a large device cannot be simulated, a typical unit-cell is considered as shown in Fig. 1b. It contains a

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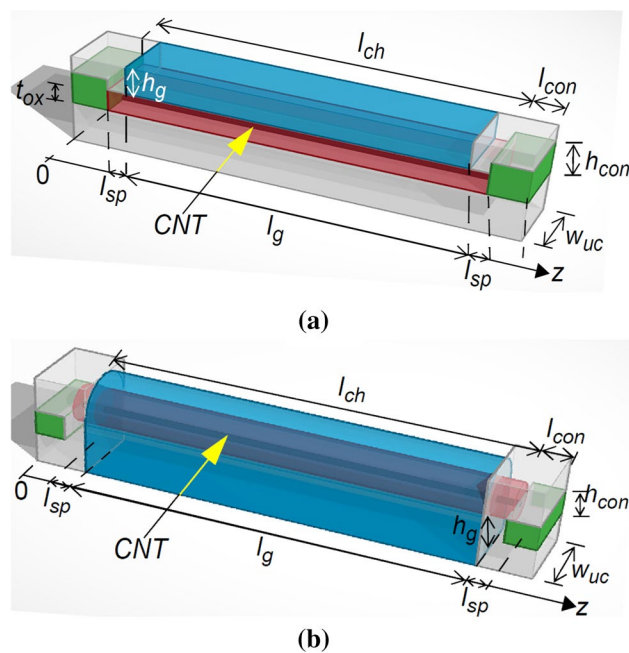
**Fig. 1** **a** Micrograph of a multi-finger HF transistor layout with multiple single-walled CNTs as channel material; the dashed box indicates the subregion represented in simulation. **b** Schematic cross section along the arrowed line in **(a)** with relevant dimensions as well as the parasitic capacitance and its contributions (shown only on the left side of the gate); the dashed box indicates one of the unit-cell cross sections used in simulation

single tube and the necessary source, drain and gate contact blocks and arrangement.

In this work, two major device design scenarios have been considered. First, a unit-cell structure with a single CNT is simulated with different gate contact arrangements: a top gate, two (local) buried gate variants, and a gate-all-around structure as a reference for maximum channel control. Also, the source/drain contact height and length are kept at minimum to avoid electrostatic field related artefacts due to the boundary conditions (cf. dashed box in Fig. 1b). These unit-cell structures allow the identification of fundamental differences in the HF performance due to the different gate arrangements. Second, a two-finger CNTFET with 20 μm finger width and realistic heights of source, drain and gate contact is considered (as schematically shown in Fig. 1b). The calculation of its HF performance is based on the unit-cell characteristics for the internal device behavior, but also includes all known external parasitic effects such as finger capacitances and contact resistance. As it turns out, one of the buried gate device designs exhibits the overall best HF performance. Thus, finally, the device design of this structure is further analyzed in terms of process variables such as gate-source spacer length and oxide thickness.

## 2 Investigated unit-cell structures

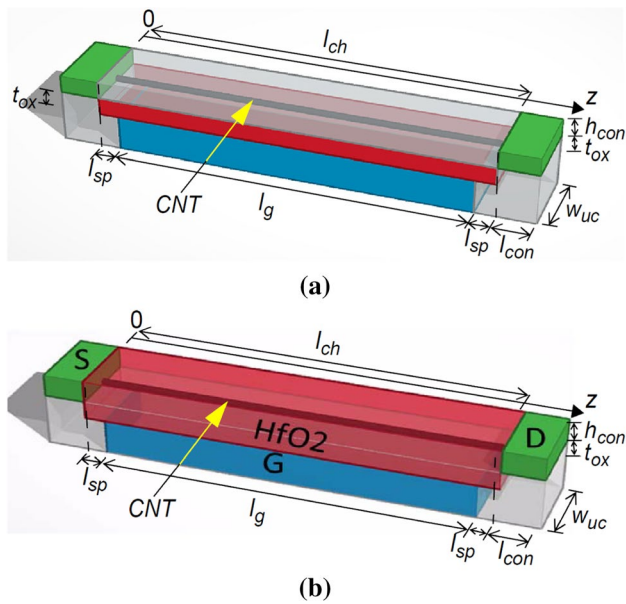
Figure 2a shows the 3D view of the simulated unit cell of a top gate (tG) structure. The latter corresponds to the typically fabricated architecture [5–7], in which the CNT is assumed to be deposited on a low-κ oxide layer (acting as isolation to the semiconductor wafer material underneath). On top of this oxide the high-κ gate oxide is grown, leading to an Ω-shaped coverage of the CNT. The 3D view also contains a definition of the relevant dimensions, while z is the direction of carrier transport along the tube.



**Fig. 2** **a** 3D view of the simulated top-gate unit-cell CNTFET structure (width  $w_{uc}$ ) derived from the cross section in Fig. 1b and consisting of a channel with a single semiconducting CNT. **b** 3D view of the gate-all-around unit-cell CNTFET structure. Green color indicates source/drain metal, blue color gate metal, red color high-κ gate oxide, and grey color low-κ isolation oxide (Color figure online)

Most theoretical investigations assume a gate-all-around (GAA) structure as shown in Fig. 2b, in which the CNT is fully enclosed in a high-κ oxide and a surrounding cylindrical gate contact. The height of the latter has been chosen here to be the same as in the tG structure. The gate height  $h_g$  here refers to the distance from the bottom of the gate oxide to the bottom of the unit cell structure. Such a GAA structure has already been fabricated in, e.g., [8], and is considered to represent the ultimate limit of FET scaling for digital applications. Its results are therefore considered in this work as reference for the comparisons. However, the GAA structure is suboptimal for HF applications since it limits the reduction of CNT spacing in multi-tube transistors [9].

A so far less investigated CNTFET structure is shown in Fig. 3, containing a buried gate (bG) instead of a top gate. The advantages of such a bG FET versus a tG FET in terms of fundamental speed versus linearity trade-offs were outlined first in [10, 11] for fairly long channel and spacer lengths and using a line charge model for the CNT. In Fig. 3a, the CNT is deposited on the high-κ oxide grown on top of the buried gate and is then covered by a low-κ oxide. This corresponds to structures fabricated in [12–16], but the high-κ oxide coverage may be suboptimal, since the gate control weakens at the top of the CNT due to the lower κ. Thus, for comparison, the case of full high-κ oxide coverage



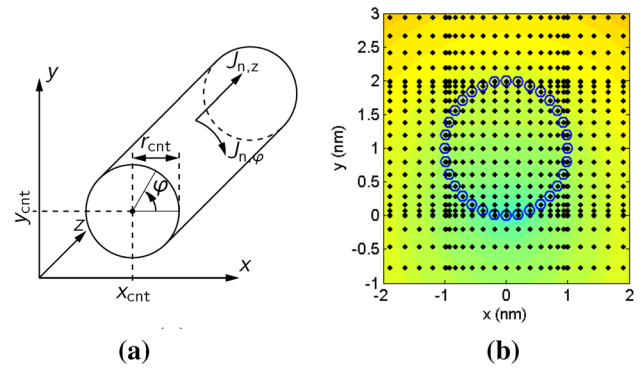
**Fig. 3** 3D views of the simulated buried-gate unit-cell CNTFET with a single CNT: structure with (a) partial high-κ oxide coverage (bGs) and (b) full high-κ oxide coverage (bGf). The same color code as in Fig. 2 applies

**Table 1** Structural parameters of the simulated unit-cell CNTFET

Description	Parameter	Value
Channel length	$l_{ch}$ ( $= l_g + 2 * l_{sp}$ )	100 nm
Spacer length	$l_{sp}$	5 nm
Gate length	$l_g$	90 nm
High-κ oxide thickness	$t_{ox}$	2 nm
Gate contact height	$h_g$	15 nm
Source/drain contact metal length	$l_{con}$	10 nm
Source/drain contact metal height	$h_{con}$	6.3 nm
Unit-cell width	$w_{uc}$	20 nm
CNT diameters	$d_{cnt}$	1.5 nm
Schottky barrier height	$\Phi_{sb}$	0.1 eV

around the CNT as shown in Fig. 3b has also been investigated in this work.

For the device simulations, it is assumed that the CNTs in a multi-tube HF structure are spaced by an average distance  $w_{uc}$  that is large enough so as to neglect electrostatic screening effects between adjacent CNTs. The impact of such effects on the terminal characteristics can be taken into account according to [9] but does not significantly change the results of the comparison between different basic CNT-FET architectures. The dimensions of the simulated unit cells as defined in Figs. 2 and 3 are summarized in Table 1. The S/D contact metal height  $h_{con}$  and length  $l_{con}$  minimize the parasitic capacitances in order to more clearly show the



**Fig. 4** a Schematic representation of the tube that is simulated as a hollow cylinder. b Discretization in a subregion of a planar CNTFET structure, highlighting the discrete points (dotted circles) defining the tube surface at which the carrier transport equations are solved

differences in the transistor characteristics between the different structures. The contacts shown can be realized in a fabricated structure as low-height metallization extensions of a thicker and wider S and D metal further away from the gate.

### 3 Device simulation method

For comparing and optimizing 3D device structures, CNT-FET terminal characteristics relevant for circuit design have to be calculated over a wide bias range. This requires a computationally efficient simulation approach. Thus, augmented drift-diffusion (DD) transport coupled with a 3D Poisson solver has been employed here. Since in a planar transistor structure with a gate oxide thickness in the order of the tube diameter carrier transport on the 3D tube surface depends on the distance of that surface to the planar gate electrode, the DD equations are solved on the cylindrical tube surface defined by the axis  $z$  in tube direction and the axis in tube circumference direction that is represented by the angle  $\varphi$  (cf. Fig. 4a). The corresponding discretization in an  $(x, y)$  cross section is shown in Fig. 4b.

The physical parameters describing the DD carrier transport were carefully calibrated to solutions of the Boltzmann transport equation [17]. Fermi statistics have been included since they are essential for being able to properly model tube (i.e., channel) charge and current above threshold and especially in the bias region that is of interest for circuit design and which is beyond the typically considered quantum capacitance limited operation region. Note that even in the absence of a contact resistance, the absolute value of the drain current still depends strongly on the band edges in the source/drain metal covered tube region. This results in a heterojunction rather than a true Schottky junction [18] between the channel and the metal covered portion of

a CNT. Tunneling through these source and drain heterojunction barriers<sup>1</sup> has been taken into account by evaluating the WKB approximation within the barrier region for the numerically calculated band edges. The resulting tunneling currents have been properly included in the generation term of the continuity equations, thus making the simulation self-consistent. Note that band-to-band tunneling has also been included but does not play a role for tube diameters below about 1.6 nm.

For simulating the single CNT unit cell structures, periodic boundary conditions are applied at the lateral borders of the considered domain with the width  $w_{uc}$ . At the other surfaces, vanishing electric fields and current densities in normal direction are assumed. The results shown in this work are valid for quasi-static operation.

### 4 Comparison of unit cell results

In this section, device simulation results of the earlier defined unit cell structures are compared. The corresponding terminals are denoted as  $S'$ ,  $G'$ , and  $D'$ . As relevant device parameters, the transconductance

$$g_{m,t} = \left. \frac{dI_{D,t}}{dV_{G'S'}} \right|_{V_{D'S'}}, \tag{1}$$

and the output conductance

$$g_{ds,t} = \left. \frac{dI_{D,t}}{dV_{D'S'}} \right|_{V_{G'S'}}, \tag{2}$$

are considered, which are associated with a single tube (index “t”). Furthermore, figures of merit (FoMs) relevant for HF circuit design and related here to just the single-tube unit cell were calculated from device simulation. The low-frequency (intrinsic) voltage gain

$$A_{V,t} = \left. \frac{dI_{D,t}}{dV_{G'S'}} \right|_{V_{D'S'}} / \left. \frac{dI_{D,t}}{dV_{D'S'}} \right|_{V_{G'S'}} = \frac{g_{m,t}}{g_{ds,t}}, \tag{3}$$

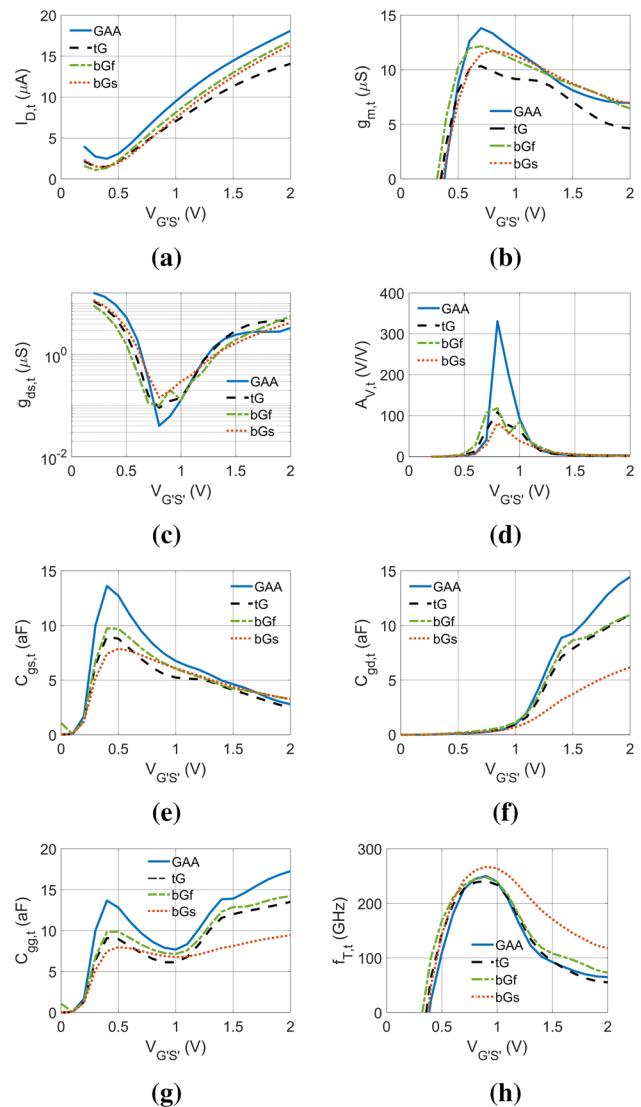
indicates the impact of high output leakage or low transconductance on power gain. Furthermore,

$$C_{gs,t} = - \left. \frac{dQ_t}{dV_{S'}} \right|_{V_{G'}, V_{D'}} = \left. \frac{dQ_t}{dV_{G'S'}} \right|_{dV_{D'S'}} \quad \text{and} \tag{4}$$

$$C_{gd,t} = - \left. \frac{dQ_t}{dV_{D'}} \right|_{V_{G'}, V_{S'}} = \left. \frac{dQ_t}{dV_{G'D'}} \right|_{dV_{D'S'}}$$

are the GS and GD capacitances, calculated from quasi-static change of the tube charge  $Q_t$ . Finally,

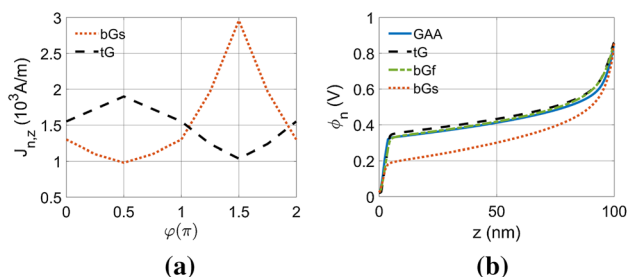
<sup>1</sup> These are typically called Schottky-barriers in the literature.



**Fig. 5**  $V_{G'S'}$  dependent characteristics of the GAA, tG, bGs and bGf structures, all related to a single-tube: **a** drain current, **b** transconductance, **c** output conductance, **d** voltage gain, **e** GS capacitance, **f** GD capacitance, **g** total gate capacitance, and **h** intrinsic transit frequency.  $V_{D'S'}=1$  V

$$f_{T,t} = \frac{g_{m,t}}{2\pi C_{gg,t}} \tag{5}$$

is the intrinsic transit frequency with  $C_{gg,t} = C_{gs,t} + C_{gd,t}$ . Above definition of  $f_{T,t}$  corresponds to a quasi-static variable from a single-pole low-pass behavior, which is consistent with the definition applied in practice for measuring and reporting the extrinsic  $f_T$  at foundries. Since HF FoMs such as power gain, linearity and power gain cut-off frequency depend strongly on parasitics, they are not considered for the unit cell but only for the two-finger structure in the next section.



**Fig. 6** **a** Current density in tube axis on the surface along the circumference and **b** mean value of electron quasi-Fermi potential along the tube axis for the GAA, tG, bGf, bGs structure at  $V_{G'}=1$  V and  $V_{D'}=1$  V

Figure 5 shows a comparison of the device characteristics and related FoMs for the various unit cell architectures defined in Sect. 2. Notice that all data are related to the single tube in this unit cell. Differences in  $I_{D,t}$  and peak  $g_{m,t}$  are close to  $\pm 15\%$  relative to the buried gate structures (Fig. 5a, b). Note that the observed offset current in Fig. 5a can be eliminated by increasing the spacer length  $l_{sp}$  between source and gate. Although the GAA structure exhibits the highest peak  $g_{m,t}$ , the drop of  $g_{m,t}$  is largest. In contrast, the buried gate structures have a lower peak  $g_{m,t}$ , but maintain higher  $g_{m,t}$  values beyond the peak, which is advantageous for circuit applications and in particular from a linearity point of view. Due to the optimal gate control in the GAA structure, its output conductance is lowest (Fig. 5c), leading to a significantly higher peak of the voltage gain  $A_{V,t}$  than for the other structures (Fig. 5d).

The capacitances defined by (4) include only the charge on the CNT and therefore yield only the tube-related capacitance without any parasitics. The parasitic capacitances used for calculating the figures of merit of the realistic two-finger structure are calculated by solving the 3D Poisson equation of just the contact structure (which is equivalent to the procedure pursued in measurements for obtaining the intrinsic transit frequency). In order to display the bias behavior of just the bias-dependent tube-related capacitance (and charge), the parasitic capacitances related to the contact metals are subtracted in Fig. 5e–g. As expected, the GAA structure has the highest tube charge and thus capacitance values due to its best gate control. In contrast, the bGs structure has lower capacitances, especially beyond the minimum of  $C_{gg,t}$ . This much lower gate bias dependence corresponds to a lower nonlinearity of the high-frequency input impedance.

The lower  $C_{gg,t}$  of the bGs structure is also the cause for its higher intrinsic  $f_{T,t}$  in Fig. 5h, especially beyond the peak. The physical reason for this is the larger gradient of the electron quasi-Fermi potential (QFP) in the bGs structure as shown in Fig. 6a, which results in a smaller charge required for carrying the same drain current. A similar effect has been observed in nanowire FETs [19]. In addition, as compared to

a top gate, the buried gate has a better channel control over the adjacent tube surface in particular in the spacer region where the field lines from the gate do not have to compete against those from the vertical source metal surface. As can be seen from Fig. 6b, this leads to a larger current density in the surface region close to the gate and thus to a larger (average) drain current and transconductance for the same bias point. The overall higher and less bias point-dependent  $f_{T,t}$  along with the competitive  $g_{m,t}$  and the lower less bias-dependent  $C_{gg,t}$  make the bGs FET the most promising architecture for HF applications.

## 5 Realistic HF transistor structure

The previous discussion referred to the performance of a single tube based unit cell without parasitics. For obtaining results that reflect conditions in fabricated CNTFETs, series resistances and parasitic capacitances of a realistic structure have to be added. In this section, a HF CNTFET with two gate fingers of  $20\ \mu\text{m}$  width  $w_g$  each is considered. The schematic cross section of a single gate finger is shown in Fig. 1b. The corresponding dimensions in addition to those of the unit cell are  $h_G = h_{con} + h_{SD} = 200$  nm,  $l_{mc} = l_{SD} = 100$  nm. The simulations were performed assuming a CNT density of  $n_t = 50$  CNT/ $\mu\text{m}$ , which has been achieved in recently fabricated HF CNTFETs [3] and allows to neglect electrostatic screening effects [9]. The tube density ( $n_t$ ) is defined as the number of tubes per  $1\ \mu\text{m}$  gate width. A unit cell contains a single tube; thus, the unit cell width is defined by  $w_{uc} = 1/n_t$ .

The series resistances of source and drain are dominated by the contact resistance between bulk metal and metal covered tube portion. A nominal value of  $R_{S,t} = R_{D,t} = 20$  k $\Omega$  per contact has been assumed, leading to a total source/drain series resistance of  $R_{S/D} = R_{S/D,t}/(2w_g n_t) = 10$   $\Omega$ . A gate contact metal stack consisting of 30 nm Al ( $2.74\ \mu\Omega\text{cm}$ ) for adhesion, 20 nm Ni ( $5.6\ \mu\Omega\text{cm}$ ) for blocking diffusion, and 150 nm Au ( $2.2\ \mu\Omega\text{cm}$ ) at the top was assumed, leading to  $R_G = 4.4$   $\Omega$ . The gate stack structure and material follow the fabricated device in [3]. The low-height S/D extensions have been implemented by our fabrication partner at TU Chemnitz (no publication exists yet on this structure). The parasitic capacitances (per gate width), given by the field lines between the S/D and gate metal surfaces, have been calculated by solving Poisson's equation for a cross section within the finger width. The values of  $C_{gs,par}$  and  $C_{gd,par}$  used in the simulation are (in fF/mm) 238.1 (GAA), 245.5 (tG), 231.5 (bGf), 184.5 (bGs), showing the lowest parasitic capacitance for the bGs structure<sup>2</sup>. Note that the ratio of the

<sup>2</sup> For the GAA structure, the value is slightly lower than that of the tG structure because the high- $\kappa$  gate oxide in the GAA structure is limited to a cylinder around the tube compared to extending across

parasitic capacitance to the total gate terminal-related tube capacitance ( $n_t C_{gg,t}$ ) is different here from that of the unit cell due to the larger contact heights of the realistic structure.

For determining the extrinsic HF FoMs representing a fabricated device with  $n_t$  parallel semiconducting CNTs, the internal nodes have to be connected to the terminal nodes through the series resistances and the parasitic capacitances have to be added between the nodes. The extrinsic transconductance of the complete transistor structure is then given by

$$g_m = n_t \frac{g_{m,t}}{1 + g_{m,t}R_{S,t} + g_{ds,t}(R_{S,t} + R_{D,t})} \tag{6}$$

with  $R_{S,t}$  and  $R_{D,t}$  as source series resistance for a single tube. Similarly, the extrinsic output conductance is

$$g_{ds} = n_t \frac{g_{ds,t}}{1 + g_{m,t}R_{S,t} + g_{ds,t}(R_{S,t} + R_{D,t})}. \tag{7}$$

The relevant device capacitances are now given by

$$\begin{aligned} C_{gg} &= n_t C_{gg,t} + C_{gs,par} + C_{gd,par}, \\ C_{gd} &= n_t C_{gd,t} + C_{gd,par} \end{aligned} \tag{8}$$

with  $C_{gs,par}$  and  $C_{gd,par}$  as total electrostatic parasitic metal finger capacitances of the realistic transistor structure as shown in Fig. 1b. The extrinsic transit frequency then reads approximately

$$f_T \approx \frac{g_m}{2\pi C_{gg}} \tag{9}$$

with  $g_m$  as extrinsic transconductance from (6). For a given transistor size, the maximum unilateral power gain

$$\begin{aligned} U &\cong \frac{g_m^2}{4R_G(\omega^2 C_{gg}^2 g_{ds} + \omega^2 C_{gd} C_{gg} g_m)} \\ &= \frac{\omega_T^2 / \omega^2}{4R_G(g_{ds} + g_m C_{gd} / C_{gg})} \end{aligned} \tag{10}$$

with  $g_{ds}$  as extrinsic output conductance from (7) and the gate resistance

$$R_G = \frac{1}{3} \rho_{mG} \frac{w_g}{h_g l_g n_f}. \tag{11}$$

The factor 3 accounts for the distributed character of the dynamic current flow, while  $\rho_{mG}$  is the gate metal conductivity,  $w_g$  ( $= 20 \mu\text{m}$ ) is the width of a single gate finger and  $n_f$  ( $= 2$ ) is the number of gate fingers. The maximum

frequency of the unilateral power gain is approximately given by

$$f_{MAX} \cong \frac{f_T}{2\sqrt{2\pi f_T C_{gd} R_G + R_G g_{ds}}}, \tag{12}$$

which yields somewhat too optimistic results due to missing additional terms.

Finally, high-frequency linearity in an amplifier can be evaluated by applying eq. (51) [20] to a FET with  $\xi = 0$ ,  $\beta_0 = \text{“infinity”}$  and  $\alpha_0 = 1$ . This yields for the bias-dependent third-order output intercept point

$$OIP_3 \approx \sqrt{\frac{4}{3}} \frac{(\frac{\hat{\omega}_T}{\omega R_S^*})^{3/2}}{(G_{3HF}^2 + G_{3IT}^2)^{1/4}} \tag{13}$$

with the high-frequency limit

$$\begin{aligned} G_{3HF} &= \frac{1}{\omega^3 R_S^{*3}} \\ &\left| -\frac{1}{6} \hat{\omega}_T^2 \hat{\omega}_T'' + \hat{\omega}_T \hat{\omega}_T' \left[ \frac{1}{6} \hat{\omega}_T' - \frac{1}{3} \frac{\dot{g}_{mi}}{g_{mi}^2} \frac{\hat{\omega}_T}{1 + g_{mi} R_S} \right] \right| \end{aligned} \tag{14}$$

and the ideal-transistor limit

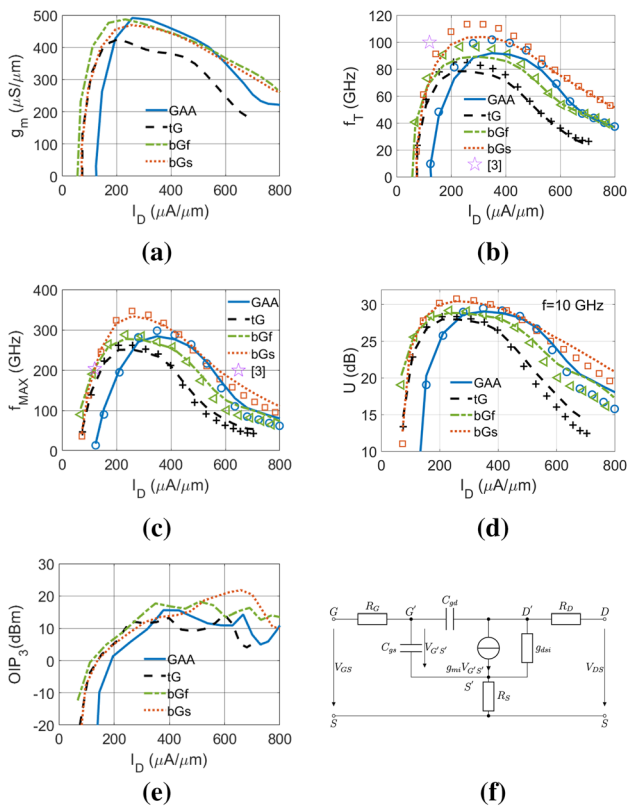
$$G_{3IT} = \frac{(\frac{\hat{\omega}_T}{\omega R_S^*})^4}{\omega^4 R_S^{*4}} \left| \frac{1}{6} \ddot{g}_{mi} - \frac{1}{2} \frac{\dot{g}_{mi}^2}{g_{mi}} \left[ \frac{1}{3} + \frac{g_{mi} R_S}{1 + g_{mi} R_S} \right] \right| \tag{15}$$

where  $R_S^*$  is the sum of the source series resistance  $R_S$  and the generator resistance ( $50 \Omega$ ),  $\hat{\omega}_T$  is the “loaded” radian transit frequency; the primes indicate the order of the derivative of  $\hat{\omega}_T$  with respect to  $I_D$  (at  $V_{DS} = \text{const.}$ ), while  $\dot{g}_{mi}$  corresponds to the second derivative of  $I_D$ . According to (13–15),  $OIP_3$  can be maximized by operating the transistor in a bias range, where the transit frequency depends most weakly on bias so that the derivatives approach zero and  $OIP_3$  approaches infinity. Notice that in contrast to bipolar transistors [20]  $G_{3IT}$  is not negligible versus  $G_{3HF}$  and needs to be included for all bias points and useful operating frequencies.

Based on the CNT characteristics of the unit cells and the analytical formulations (6–13), the small-signal FoMs for a complete two-finger structure have been calculated. The results are shown in Fig. 7 as a function of the drain current per unit gate width, which is of practical relevance for circuit design. The tG and GAA structure still have the most narrow peak region for  $f_T$  and  $f_{MAX}$  as well as the lowest  $OIP_3$  in the circuit design relevant bias range. In particular, the bGs structure has visibly higher  $f_T$  and  $f_{MAX}$  over a wider current range. The higher  $f_{MAX}$  is a result of the higher  $g_m$  and lower  $C_{gd}$  that lead to a higher power gain as shown in Fig. 7d. Furthermore, as a consequence of the lower bias dependence (i.e., curvature) of its  $f_T$ , the

Footnote 2 (continued)

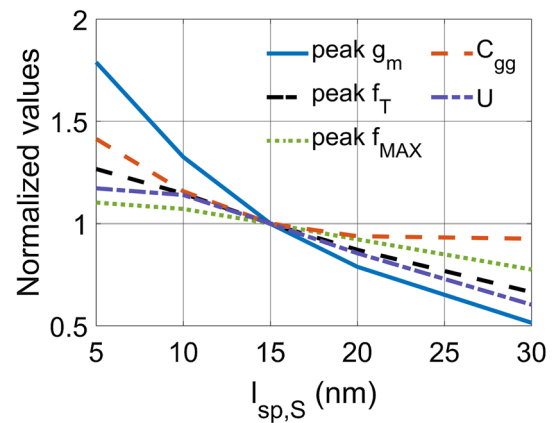
the entire unit cell in the other structures (cf. Fig. 1). In other words, there is less high- $\kappa$  gate oxide between G and S/D contact in the GAA structure than in the tG structure.



**Fig. 7** Extrinsic FoMs for a  $2 \times 20 \mu\text{m}$  HF CNTFET with 50 CNT/ $\mu\text{m}$  and different gate arrangements: **a** transconductance, **b** transit frequency and **c** maximum oscillation frequency. **d** Unilateral power gain and **e**  $OIP_3$  were determined at 10 GHz. Symbols indicate small-signal circuit simulation results.  $V_{D,S} = 1 \text{ V}$ . **f** Small-signal equivalent circuit used for circuit simulation

$OIP_3$  of the bGs structure in Fig. 7e has the highest peak, which is reasonably wide, and is also the highest when averaged over the circuit design relevant bias range. For verification, the FoMs have also been determined with a circuit simulator and a small-signal compact model equivalent circuit derived from [21] as shown in Fig. 7f. For calculating its bias-dependent element values from (6–8), the intrinsic transistor parameters were taken directly from device simulation at each bias point. The corresponding results, indicated by symbols in Fig. 7b–d, demonstrate that the analytical Eqs. (6–12) are well suited for estimating device performance and hence for guiding process technology development based on a few key device parameters.

Apparently, the bGs structure exhibits overall the best HF performance also when parasitics are included. In addition, according to [11], this architecture enables optimizing for higher linearity and speed more easily by changing the spacer length between S and G, which is limited for a tG or GAA structure. The buried gate structure is also advantageous for digital circuits [14].



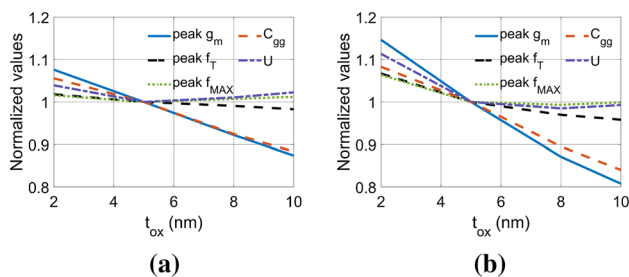
**Fig. 8** Source spacer length dependence of the peak values for  $f_T, f_{MAX}, g_m$  as well as of  $C_{gg}$  taken at peak  $g_m$  and  $U(10 \text{ GHz})$  for the bGs unit-cell. All values have been normalized to their values at  $l_{sp,S} = 15 \text{ nm}$ .  $V_{DS} = 1 \text{ V}$

The obtained cut-off frequencies match those of recently fabricated HF CNTFETs in [3] reasonably well after (1) eliminating probe series resistances and capacitances, which do not belong to the transistor structure, (2) reducing the still relatively high contact resistance to the value assumed in this work and (3) adjusting  $R_g$  to the shorter gate width used here. The resulting data points are inserted in Fig. 7b, c with  $f_{MAX}$  being about 20% lower than the predicted value for the corresponding tG structure. This is attributed to the higher (average) output conductance and somewhat lower (average) internal transconductance per tube of the experimental data as well as the higher parasitic DG capacitance of a T-gate structure.

### 6 Optimum CNTFET structure

According to the previous results, the buried gate (i.e., bGs) structure yields the best overall HF performance. It is therefore analyzed in more detail regarding the sensitivity of HF FoMs with respect to structural variations in the unit cell, namely the GS spacer length  $l_{sp,S}$  (at constant GD spacer length) and the thickness  $t_{ox}$  of the high- $\kappa$  gate oxide. For these investigations, the tube density  $n_t$  was kept at 50 CNT/ $\mu\text{m}$  in order to avoid electrostatic screening effects in current and charge. These still relatively low densities are representative of the best HF CNTFETs fabricated so far. The results are shown in normalized form for peak values of  $g_m, f_T, f_{MAX}$ , and  $U$  as well as for  $C_{gg}$  taken at peak  $g_m$ .

The variation of  $l_{sp,S}$  results in a strong dependence of peak  $g_m$  and a more moderate dependence of  $C_{gg}$  as shown in Fig. 8. Their increase toward smaller  $l_{sp,S}$  is caused by the stronger influence of the gate field on the potential in the source barrier region, which increases the transmission through the barrier.



**Fig. 9** Gate oxide thickness dependence of the peak values for the same variables as in Fig. 8 for (a) the bGs and (b) the bGf structure. All values have been normalized to their values at  $t_{ox} = 5$  nm

The parasitic capacitance, not shown separately here, exhibits a very similar dependence, which is somewhat weaker than  $1/l_{sp,S}$  though. The similar behavior of  $g_m$  and  $C_{gg}$  causes  $f_T$  to decrease relatively weakly with  $l_{sp,S}$ . The weaker drop of  $f_{MAX}$  results from its proportionality mainly to  $\sqrt{f_T/R_G}$ , where a larger GS spacer decreases the gate finger cross section and thus increases  $R_G$ . The latter is also the reason for the slightly stronger drop of  $U$  versus that of  $f_T$  toward larger  $l_{sp,S}$ , since  $U$  is proportional to  $f_T/R_G$  (as long as  $g_{ds}$  is negligible). However, toward small  $l_{sp,S}$  the SD leakage and thus  $g_{ds}$  increases rapidly, compensating for the changes in  $f_T$ ,  $R_G$ , thus leading to a weak increase in  $U$ . Notice that the sensitivity results of the bGf structure are very similar.

Varying  $t_{ox}$  yields the results shown in Fig. 9a. As expected, peak  $g_m$  decreases with increasing  $t_{ox}$  due to the reduced influence of the gate field on the source barrier potential and the nonlinear dependence of the transmission through the barrier on the electric field. The decrease in  $C_{gg}$  is slightly less pronounced due to the smaller drop of  $C_{gg,par}$ . Again, the very similar trend of  $g_m$  and  $C_{gg}$  causes  $f_T$  to change only weakly with  $t_{ox}$ . The levelling-off and even increase in  $f_{MAX}$  and  $U$  toward larger  $t_{ox}$  is due to a stronger decrease in  $C_{gd}$  than of  $f_T$  with  $t_{ox}$ . Notice the visibly larger sensitivity of the electrical parameters for the bGf structure in Fig. 9b especially toward a thinner gate oxide. Above results shows that decreasing  $l_{sp,S}$  below 5 nm and  $t_{ox}$  below 2 nm will not lead to a significant increase in power gain and device speed ( $f_T$ ) anymore. Also, a thinner  $t_{ox}$  may lead to unacceptable gate leakage. However, in a circuit application in which a high capacitive load needs to be driven, a higher  $g_m$  due to a further reduction of  $l_{sp,S}$  below 5 nm may still be beneficial. The bGs architecture allows such an optimization in contrast to a tG and GAA architecture.

## 7 Summary and conclusion

The high-frequency performance of different fundamental CNTFET device architectures with respect to the gate contact arrangement has been investigated based on 3D device

simulation. First, unit cell structures containing a single CNT and having a width corresponding to CNT spacing in most recent fabricated HF CNTFETs were simulated. The results, in terms of transconductance and CNT charge-related capacitances, showed an advantage for a local buried gate device design over a top gate or gate-all-around structure. Based on the electrical characteristics of the unit cells, the device structures were extended to that of a two-finger CNTFET with 20 nm gate width, 100 nm gate length, and realistic contact sizes. Including realistic values for all series resistances and parasitic capacitances of the structures, the device parameters and figures-of-merit relevant for HF circuit design were calculated employing analytical equations. The latter were also verified by circuit simulation using a small-signal model of the complete 3D CNTFET with bias-dependent elements for the intrinsic portion. The results confirmed the advantages of a local buried gate architecture regarding power gain and linearity within the circuit relevant bias region also for realistic HF CNTFET structures. Considering in addition the results of a sensitivity analysis with respect to possible process variations of the gate-source spacer length and gate oxide as well as the more flexible fabrication of CNTFETs with non-symmetric gate location for tailoring the electrical performance toward higher speed, linearity and breakdown, makes the buried gate architecture preferable over other architectures. Overall, considering the still relatively low tube density in the channel and current per tube, the results indicate that CNTFET technology is expected to achieve a significant HF performance improvement versus RF-CMOS.

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## Declarations

**Conflict of interest** The authors declare that they have no competing interests.

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