

Parasitic Effects Affecting Responsivity of Sub-THz Radiation Detector Built of a MOSFET

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Abstract In this paper, an analysis of parasitic elements that are found in all typical metal-oxide-semiconductor field-effect transistors (MOSFETs) has been performed from a viewpoint of a designer of sub-THz radiation detectors. A simplified model of the extrinsic MOSFET device has been proposed. Typical values of its parameters have been assumed. The authors have also built a model of the MOSFET's channel (intrinsic device) employing the standard transmission line approach and defining a Z-matrix of the circuit in order to facilitate its integration with the parasitic elements. The full effective circuit model of the MOSFET has been employed to analyze the behavior of the detector when subjected to sub-THz radiation delivered through the Gate and Source pads. Finally, predictions of the responsivity of an example detector built of a typical MOSFET integrated with a patch antenna fabricated on a 40- μm -thick silicon membrane have been compared with measurements of several structures employing MOSFETs of various channel widths. Good agreement between the predictions and the measurements has been demonstrated, which indicates that despite its simplicity, the presented model can significantly help to better understand operation of MOSFET-based detectors and also to use the existing silicon-based manufacturing processes.

Keywords Submillimeter wave detectors · MOSFETs · Semiconductor device modeling · Equivalent circuits · Microstrip antennas

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1 Introduction

In the literature dedicated to detection of the sub-THz radiation for scientific or commercial applications, the detecting circuits described most often are based either on Schottky diodes [1], bolometers [2], or the SIS devices [3], which have been known for years and successfully employed in numerous fields. The detecting structure is typically integrated with some antenna printed on a thick dielectric substrate of relatively high dielectric constant (e.g., GaAs, Si) in order to improve the responsivity of the detector through a better coupling between the incoming radiation and the active device. In order to monolithically integrate the detector with an antenna, a large area of the wafer needs to be taken up by the complete structure since the antenna is, by definition, comparable to the wavelength, and nearly always much larger than the active device itself. While this is acceptable in relatively simple single-pixel detecting circuits or even large detecting arrays aimed at scientific applications, it makes the use of sub-THz imaging for commercial applications very expensive when typical manufacturing processes are to be employed.

A mass-produced imaging detectors working in the sub-THz frequency range were only possible after the theory that predicted effective operation of field-effect transistors (FETs) in such a range was first presented in [4] and extended in [5] to account for detection mechanism applicable—among other FET devices—to metal-oxide-semiconductor field-effect transistors (MOSFETs) and analyzed later in a number of papers dedicated to the underlying physics of the mechanism [6–8]. A MOSFET-based detector of the sub-THz radiation consisting of a detecting device monolithically integrated with an antenna as well as an amplifier of the detection signal and often quite complex read-out circuitry [9] can be relatively easily copied many times to form an imaging array consisting of many pixels and manufactured using well-known and widely available silicon-based technologies offered commercially by a large number of foundries through the so-called multi-project wafer (MPW) services.

In the literature, description of a number of successful realization of silicon MOSFET-based detectors realized using a commercially available manufacturing process can be found [9–11]. The reported circuits differ with the frequency band they aim at (typically one of the atmospheric transmission windows at 340 or 650 GHz), or the construction of the antenna integrated with the detector. However, all the reported circuits based on MOSFETs seem to rely on a rough 1-dimensional model of the detection mechanism itself [7, 8]. It is believed that the antenna should be well-matched to the device in order to improve the responsivity of the device as shown in [12] or [13]. The detectors known in the literature are typically equipped with narrow-band antennae which are expected to work in a well-defined frequency band as shown in [9–12]. An alternative approach is based on broad-band antennae which maintain constant level of the impedance and which again feed the detecting device as in [10]. These two approaches work when the input impedance of the detecting device is relatively low and comparable to the output impedance of the antenna. This cannot be, however, predicted exactly as it seems no good models of MOSFETs are available that can be used also for designs operating in the sub-THz frequency band, which is well above the f_t (the frequency related to the minimal transit time through the active region of the device) of the devices employed. As a result, a very rough effective circuit model of the MOSFET's channel [14] based on selected properties of the semiconductor material is often employed to predict the level of impedance and to facilitate the design process.

In this paper, an attention is drawn to the existence of parasitic elements in all typical n-channel MOSFET (n-MOSFET) devices that are often employed in sub-THz detectors and the

role they play in the effective input impedance that should be expected from typical MOSFETs when employed at frequencies as large as 300 GHz or higher. Such parasitics are very often neglected in calculations that concentrate on the Dyakonov-Shur detection mechanism [5]. It is usually extended only with some access resistance added to the complex impedance of the channel alone [15] while the other effects (e.g., lumped gate capacitances) are not accounted for. This results in a very rough approximation of the impedance level, which, in turn, leads to similarly approximate designs of the antenna like in [12]. The overall goal of this paper is to extend [12] and to provide some technological information to the on-going discussion dedicated to construction of improved versions of MOSFET-based detectors of the sub-THz radiation. Although the role of parasitics in the operation of such detectors was already mentioned in [13], the major focus of the paper was different, and it does not answer questions related directly to the layout of FETs employed in detecting circuits. The work presented herein aims at filling this gap. Additionally, the authors' intention is also to indicate that some available explanations (e.g., in [13]) of the relationship between the device's responsivity and its bias voltage based on the power transfer between the antenna and the transistor channel should be rather treated as an approximation only. It seems rather that at very high frequencies, the role of the parasitics becomes dominant, which makes much less significant the influence of the actual level of the channel impedance on the effective impedance that loads the antenna.

The composition of the paper is the following: in Section II, a simplified technological model of a typical n-MOSFET is presented together with its effective circuit consisting of lumped parasitic elements; Section III describes a RC-ladder model of the transistor channel and its closed-formula model obtained using the transmission line theory; In Section IV, the complete circuit model of the device is employed to analyze the behavior of the detector under various operating conditions, and finally, in Section V, predictions of the responsivity of a detector built of a typical MOSFET integrated with a patch antenna fabricated on a locally thinned silicon substrate are compared with measurements of several structures employing MOSFETs of various channel widths. Good agreement between the predictions and the measurements is demonstrated, which indicates that despite its simplicity, the presented model can significantly help to use the existing silicon-based manufacturing processes.

1.1 A Model of the Extrinsic Part of a n-MOSFET

A typical n-MOSFET is fabricated on p-type silicon substrate or, in practice, silicon substrate where a p-doped well was processed, first (e.g., [16], p. 35). In high-density complementary MOS (CMOS) bulk technologies, employing doped wells beneath individual devices helps manufacturing n- and p-channel transistors on one substrate as well as provides electrical isolation between neighboring transistors. The central part of the device is covered with an insulating layer of silicon dioxide (SiO_2) of thickness of the order of tens of nanometers (Gate oxide). On top of the insulator, a low-resistivity Gate with heavily doped polycrystalline silicon (poly-Si) is formed. Besides the Gate, two more heavily doped low-resistivity regions are formed in the adjacent substrate to act as Source and Drain ohmic contacts. Despite the existence of the Gate acting as a mask, the highly doped regions extend slightly below the Gate due to lateral diffusion, which is inevitable in consecutive high-temperature fabrication processes. Such a construction of a typical n-MOSFET gives rise to a number of effects that result in increased losses particularly when the device is subjected to signals of frequencies from the sub-THz range. A vertical cross-section through a transistor of this type is shown in Fig. 1, together with lumped elements that represent the loss mechanisms spread over the structure.

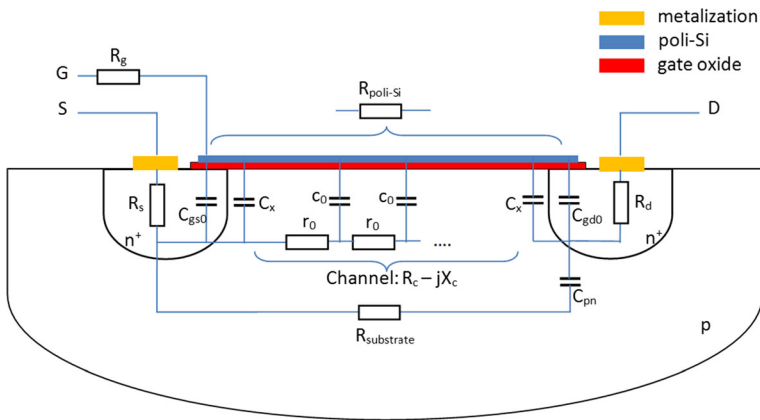


Fig. 1 A simplified view on a n-MOSFET fabricated on a p-type well with two ohmic contacts to Source and Drain and polysilicon Gate on thin gate oxide with basic mechanisms responsible for parasitic losses indicated

Depending on the selected foundry and the employed manufacturing process, the values of the elements do vary. The parameters that allow calculating these values are usually provided to customers in form of a device model and covered with non-disclosure agreements (NDA). Nevertheless, the order of magnitude of the indicated lumped element values is more or less independent on the foundry and, as shown in Section IV, can still be used to successfully analyze the operation of an example detector for a number of operating conditions. The values of the resistances depend on the finite conductivities of highly doped regions of the MOSFET. Thus, the R_s and R_d resistors represent resistances of a contact between metallization layer of negligible resistivity to the n^+ ohmic contact regions and a finite sheet resistance R_n of the n^+ region itself over a distance L_n from the contact to the edge of the gated region. The R_g resistor represents the resistance of a contact between the metallization layer (not shown in Fig. 1 for the sake of simplicity) and the poly-Si region of the Gate. The values of these resistances can be further influenced by design choices made during preparation of the device layout when the number of single contacts used to connect metal layers with the n^+ or the gate regions is chosen. As a result, the R_s and R_g resistances can be treated as the access resistance employed in calculations shown in [15]. However, there are at least two more resistances that should also be accounted for, when an effective circuit of a n-MOSFET is prepared. The first one—the $R_{\text{poli-Si}}$ resistor—results from finite (although low) conductivity of the poly-Si Gate electrode running along the channel. The other one is the resistivity of highly doped p-well beneath the device, which can be described with the $R_{\text{substrate}}$ resistor.

Besides resistances, the model of the n-MOSFET should also account for capacitances that are present in the structure, and which are sensitive only to the DC biasing voltages of the device, which are kept constant. First of all, the two parallel plate capacitors formed by the poly-Si layer separated by the gate oxide from the S- or the D-side n^+ region should be evaluated. Despite the fact that these regions extend only slightly below the Gate electrode, the resulting overlap capacitors C_{gsd} and C_{gd0} cannot be neglected because of the extremely thin gate oxide separating the conductive plates, which greatly increases these capacitances. Typically, while calculating the values of these capacitances, the fringing effect (extension of the electric field beyond the parallel plates) is also accounted for assuming that the two effects (the overlap and the fringing capacitance) scale with the channel width W . What should

also be accounted for is the actual Gate parasitic capacitance $2C_x$ which is not sensitive to slight fluctuations of the sub-THz signal and can be approximated as the overlap capacitance C_{GB0} formed by the poly-Si electrode separated from the substrate with the oxide layer. The C_{GB0} capacitance is formed only at longitudinal edges of the Gate electrode, and hence, it is proportional to its length. Because in typical manufacturing processes (i.e., local oxidation of silicon – LOCOS), one obtains the oxide layer of thickness that varies from very thin in areas directly under the poly-Si layer to relatively thick in areas further away from the channel; the unit value of C_{GB0} cannot be obtained analytically and usually comes from measurements of dedicated test structures. For the sake of this analysis, it can be assumed that C_{GB0} is comparable to the other overlap capacitances since the mechanism that creates it is the same in all these cases. Finally, one should also account for the capacitance C_{pn} of the p-n junction formed by the n^+ region under the Drain contact and the p-well. Given the standard operating conditions of the MOSFET-based detector described in [5], when there is no externally applied Drain-Source voltage V_{DS} , the junction is reversely polarized, which introduces some junction capacitance that is proportional to the surface area of the D-side n^+ area. There is no need to introduce a similar capacitance on the S-side of the channel because in typical designs (also in detectors described in Section V), the p-well and the Source potentials are kept equal using a dedicated so-called substrate contact made at the Source n^+ area.

For the sake of analysis described in Section IV, realistic (accurate to the order of magnitude) values of the parasitic elements needs to be chosen. The R_s and R_d contact resistances usually have values ranging from single Ohms to tens of Ohms, and 20Ω can be safely assumed as a representative value, especially when a minimum number of contacts are used in order to keep small the layout of the overall device. A very similar or slightly smaller value can be used as the R_g value since the corresponding contact is shorter. Depending on the doping level, the sheet resistance $R_{\text{poly-Si}}$ of the poly-Si track also changes from ten to several tens of Ω/square , and the value of $20 \Omega/\text{square}$ seems reasonable and approx. twice as large as values reported in [17] for poly-Si layers slightly thicker than those used in integrated circuit (IC) manufacturing. The same value can be chosen as the sheet resistance R_n of the n^+ region. This, together with an assumption that the L_n distance is small and does not typically exceed a few micrometers at most, allows fully defining the resistances R_s and R_d . The last sheet resistance value is $R_{\text{substrate}}$, and it depends on the doping level of the p-well. A value ranging from several hundreds to a few thousands Ω/square can be expected here, which results in significant level of resistance for devices of typical dimensions (close to a square). As a result, the resistance $R_{\text{substrate}}$ can usually be neglected (assumed infinite) in effective circuit models and is accounted here for the sake of completeness only. Representative values of capacitances can be estimated in a similar way. Assuming the typical thickness of the gate oxide of 50 nm, and the maximal overlap distance of $0.2 \mu\text{m}$ (the value provided in [16], p. 36, doubled to account also for inaccuracies in mask positioning) as well as the relative electrical permittivity of SiO_2 $\epsilon_r(\text{SiO}_2)=3.9$, one obtains the overlap capacitance C_{gs0} and C_{gd0} of approx. $1.4 \text{ fF}/\mu\text{m}$. The C_{GB0} capacitance for the same oxide thickness is again $1.4 \text{ fF}/\mu\text{m}^2$, while the C_{pn} capacitance is comparable to the oxide capacitance of similar surface area. It can be safely neglected, however, since it is in-series with large $R_{\text{substrate}}$ resistance that significantly limits any currents flowing though this path. It needs to be stressed out at this point that the decision to divide the total Gate capacitance $2C_x$ in two equal parts and place them in the circuit symmetrically on both sides of the channel is purely arbitrary, although it seems reasonable. As shown in Section IV, locating this capacitance on the Source side only does not significantly change the obtained results, thus the symmetrical distribution of parasitic capacitances is kept

in the model. Thus, in this approach, it is the biased channel that breaks the symmetry of the structure, which is necessary in order to record any photo-detection signal as is often reported. The values of all the parasitic elements were collected in Table 1. Obviously, the table shows only some estimation of the values aiming mostly at identifying their order of magnitude. The parameters listed there can be evaluated much more accurately given the parameters of a particular CMOS process or more elaborate close-form expressions (e.g., as in [16]).

1.2 Effective Circuit Model of the n-MOSFET’s Channel

The most important part of the MOSFET structure is its channel where the detection of sub-THz radiation occurs. In Fig. 1, the channel is represented with a RC-ladder circuit consisting of a large number of unit resistances r_0 and shunt capacitances c_0 , which connects the Source and the Drain. According to [15], in the most general case, the transistor channel can be modeled using the RC-ladder shown in Fig. 1 augmented with the so-called kinetic inductance (per unit length) l_0 arising from the inertia of the electrons in the channel and a parasitic conductance g_0 parallel to the gate capacitor (leaky gate). A modified circuit of the intrinsic transistor (the channel) is shown in Fig. 2a. When channel losses are small, the conductivity g_0 can be safely neglected in the model. It can be further simplified when the non-resonant detection only is allowed, which is justified for relatively large (like those used in this work) silicon transistors where the plasma waves are expected to be effectively damped before they can travel the whole length of the channel. In that case, a circuit shown in Fig. 2b is applicable.

The circuit shown in Fig. 2b is a known transmission line model of characteristic impedance Z_0 supporting transverse electromagnetic (TEM) waves that propagate along it with a propagation constant γ_0 :

$$Z_0 = \sqrt{\frac{r_0}{j\omega c_0}} = \sqrt{\frac{r_0}{2\omega c_0}} - j\sqrt{\frac{r_0}{2\omega c_0}} \tag{1a}$$

$$\gamma_0 = \sqrt{r_0 j\omega c_0} = \sqrt{\frac{\omega r_0 c_0}{2}} + j\sqrt{\frac{\omega r_0 c_0}{2}}, \text{ and} \tag{1b}$$

$$r_0 = \frac{1}{n^{(2D)} e \mu W} \text{ and } c_0 = \frac{\epsilon_0 \epsilon_r W}{d} \tag{1c}$$

where $n^{(2D)}$ is the effective 2-dimensional gate-bias-dependent carrier concentration in the channel, e is the elementary charge, μ is the carrier mobility in the channel, W is the channel width, and d is the thickness of the oxide layer, while ϵ_r is the relative permittivity of SiO₂.

As shown, the definition of the channel unit resistance r_0 neglects the diffusion current. This is one of the implicit assumptions behind the Dyakonov-Shur theory presented in [4] and

Table 1 Values of the parasitic elements of the effective circuit model of the n-MOSFET

R_s, R_d	R_g	$R_{\text{poli-Si}}$	$R_{\text{substrate}}$	$C_{\text{gs0}}, C_{\text{gd0}}$	C_x	C_{pn}
[Ω]	[Ω]	[Ω]	[Ω]	[fF]	[fF]	[fF]
20+20 L _n /W	10	20 W/L	5000 L/W	1.4 W	1.4 L	0.35 L•W

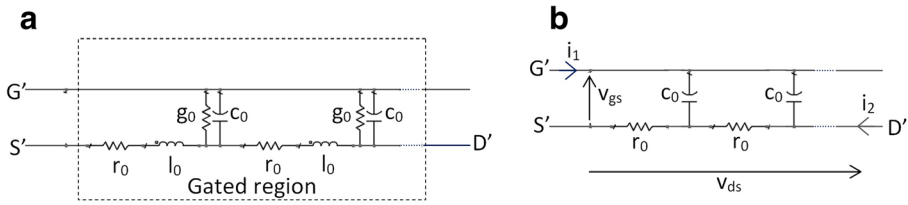


Fig. 2 A general effective circuit model of the MOSFET channel (a) and its simplified version with feeding THz signal voltages and currents indicated, which is applicable to non-resonant detection and non-leaky gate where l_0 and g_0 can be neglected (b)

which was explicitly declared in [8]. This lies outside of the scope of this paper to analyze the validity of this assumption, especially that the type of the current does not seem to be of major importance to the topic of parasitics, which is our main focus. Technically, the channel unit resistance r_0 should also be augmented with the sheet resistance of the poly-Si layer. However, the typical operating conditions that guarantee the maximum responsivity of the MOSFET-based detector require that the channel is almost closed, which means that the component related to the electron density in the channel dominates, and accounting for the poly-Si layer will not improve the model noticeably. The finite conductivity of the poly-Si track forms an alternative current path that allows the sub-THz signal to bypass the channel and decrease the responsivity. Thus, it seems reasonable to employ the $R_{\text{poli-Si}}$ as an element of the extrinsic rather than the intrinsic device. Also, the value c_0 is expressed as the oxide capacitance only as if the applied gate bias was driving the gate capacitance into accumulation ([16], p. 85). In reality, it is expected rather that the capacitance is in the weak to moderate inversion state (at a point when the MOSFET channel starts to form), where its value is smaller. It is, however, of similar order of magnitude to the oxide capacitance C_{OX} , and for this reason and also for the sake of simplicity, it was decided to use the C_{OX} as the c_0 capacitance here.

Using the Z-matrix of the transmission line of characteristic impedance Z_0 and propagation constant γ_0 and the well-known transmission line theory [18], the impedance matrix of the circuit shown in Fig. 2b can be defined as:

$$\begin{bmatrix} v_{gs} \\ v_{ds} \end{bmatrix} = Z_C \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} Z_0 \coth(\gamma_0 L) & Z_0 \tanh\left(\frac{\gamma_0 L}{2}\right) \\ Z_0 \tanh\left(\frac{\gamma_0 L}{2}\right) & 2Z_0 \tanh\left(\frac{\gamma_0 L}{2}\right) \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \quad (2)$$

where L is the channel length.

Similar results were obtained in an analysis applied to a high electron mobility transistor (HEMT) in order to extract parameters of its effective circuit model at lower frequencies than the sub-THz band shown in [19]. Figure 3 shows the real and imaginary part of the $\coth(\gamma_0 L)$ factor calculated for $f=300$ GHz, $n^{(2D)}=5 \times 10^{11} \text{ cm}^{-2}$, $\mu=331 \text{ cm}^2/\text{Vs}$ assumed after [15], and $d=50$ nm like in Section II. Based on eq. (2), the input impedance of the MOSFET (the v_{gs}/i_1 ratio with the Drain maintained open or i_2 kept at 0A) as seen by the antenna are again equal to the characteristic impedance of the channel Z_0 , as long as relatively large devices ($L > 0.4 \mu\text{m}$) are being used. The intrinsic part of a MOSFET of square area of tens of micrometer square is represented by the input impedance of several hundreds to a few thousands Ohms depending on the bias applied. It should be stressed out that for devices operating in the microwave frequency range, offering much higher electron mobility than silicon-based MOSFETs (e.g.,

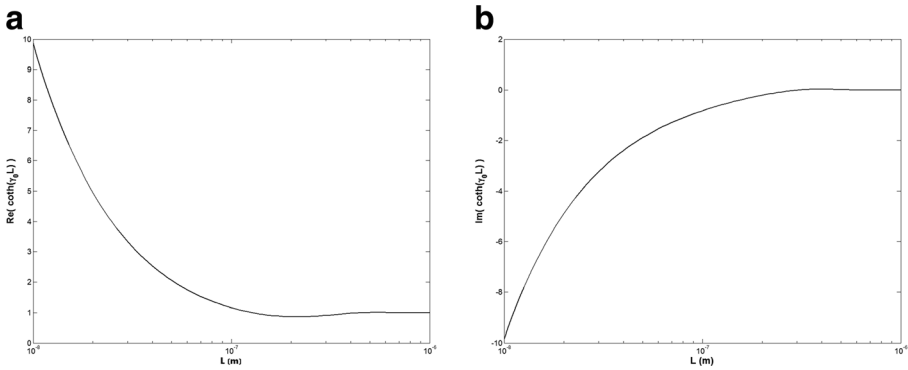


Fig. 3 Real (a) and imaginary (b) part of the $\coth(\gamma_0 L)$ factor that modifies the input impedance of the channel of a MOSFET with varying channel length L

AlGaIn/GaN HEMTs with mobility $\mu \cong 2000 \text{ cm}^2/\text{Vs}$) and lower Gate capacitances, the input impedance given by eq. (2) becomes dominated by the capacitive component as soon as L falls below $1 \text{ }\mu\text{m}$, hence the gate capacitance present in typical circuit models of MOSFETs reported in the literature.

1.3 Effective Circuit Model of the n-MOSFET

Based on the model of the extrinsic part of the MOSFET presented in Section II as well as the effective circuit model of the device’s channel shown in Section III, a model of the complete transistor can be proposed, which accounts for the parasitic effects present in the structure. It is shown in Fig. 4, where the channel is represented with the Z-matrix of the 2-port defined with Eq. (2). The Drain is open (or loaded with a large impedance of a read-out circuit), and, thus, the R_d resistance can be neglected.

Using the effective circuit model, it is possible to check the input impedance of a typical MOSFET as seen from the G-S contact pads, where an antenna is usually connected. Figure 5 shows the small-signal Z_{gs} impedance ($\partial v_{gs}/\partial i_g$ ratio) calculated for several values of the $Z_0 = R_c(1-j)$ channel impedance corresponding to different gate-biases or the channel sizes. The value of parasitic elements was obtained for a device of dimensions of $W=10 \text{ }\mu\text{m}$ and $L=$

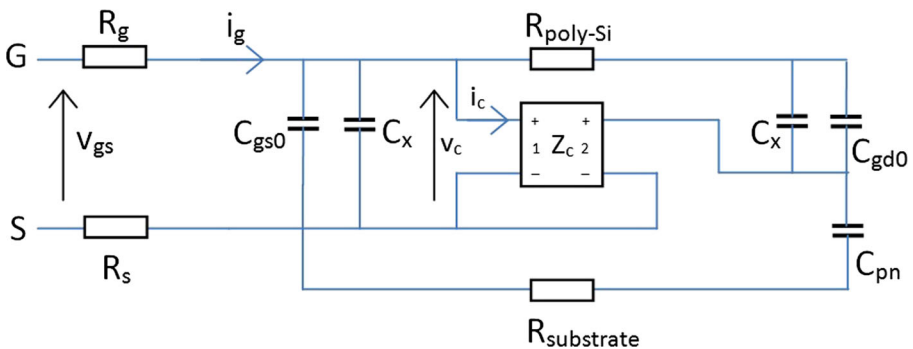


Fig. 4 Effective circuit model of a typical MOSFET as seen through the G-S electrodes

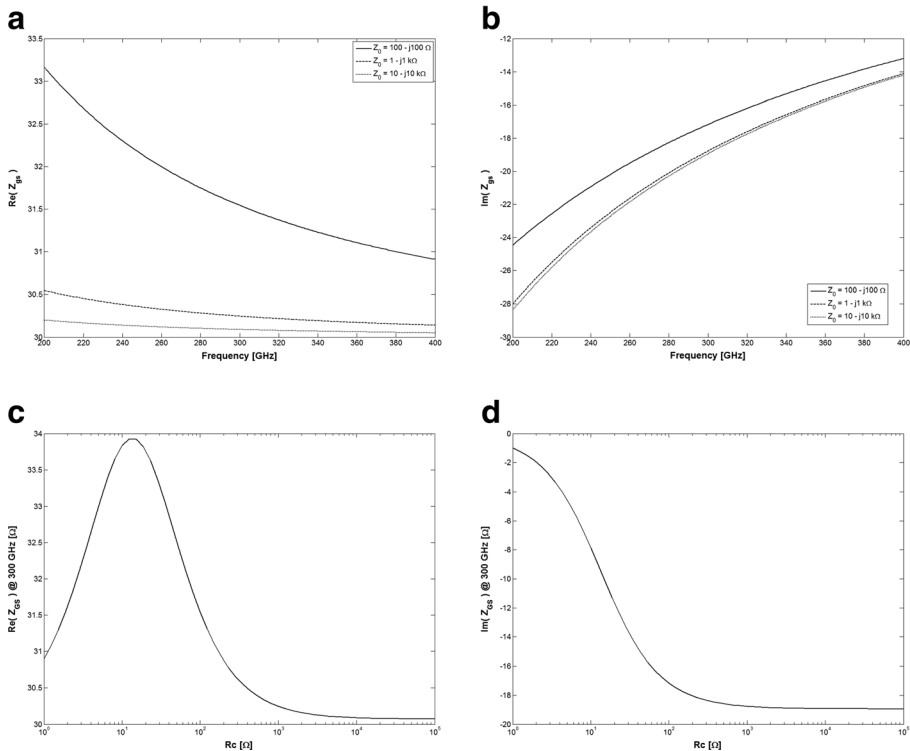


Fig. 5 Input impedance Z_{gs} of the $10 \mu\text{m} \times 10 \mu\text{m}$ MOSFET seen from the G-S pads vs. frequency (**a**, **b**) and calculated at $f=300$ GHz vs. Z_0 value (**c**, **d**)

$10 \mu\text{m}$. A constant Z_0 value was assumed for simplicity, which seems justified as in relatively narrow frequency band of interest; the frequency-dependent changes of the Z_0 values are much smaller than the range of values used in calculations. The exact values of Z_0 employed for this numerical experiment correspond to various carrier concentrations in the channel (ranging from cir. 5×10^8 up to $5 \times 10^{12} \text{ cm}^{-2}$) and were selected so that different operating conditions of the MOSFET are well represented. The Z_{gs} impedance was additionally calculated at a single frequency of $f=300$ GHz but in wide range of the Z_0 values.

It can be safely assumed that the value R_c for MOSFET employed as a sub-THz radiation detector (device with gate-bias at the threshold value) does not fall below 100Ω . Thus, for standard operating conditions, no significant influence of the channel conductivity on the input impedance Z_{gs} can be observed. Its real part only weakly depends on frequency and is dominated by the contact resistance to the n^+ area and to the poly-Si track (in the analyzed case $R_s + R_g \cong 30 \Omega$). An increase of the resistive component of Z_{gs} observed for $R_c \cong 10 \Omega$ does not seem to have any practical use because maximum value of the impedance is anyway only a few percent higher than the value obtained for nearly closed channel. A slightly stronger frequency dependence of the imaginary part of the input impedance results from the existence of the overlap capacitances. By placing the total overlap capacitance on the Source side of the channel (instead of dividing it into two parts), this influence can be made even stronger. However, in that case, the practical

level of the imaginary part of Z_{gs} would be only twice larger than shown in Fig. 5d, which does not seem to be crucial when Z_{gs} is to be analyzed in order to better design an antenna and improve its impedance matching to the transistor.

It must be stressed out that the analysis presented above accounts for the MOSFET treated as a passive structure, hence the small-signal approximation of the impedance observed at its input. It accounts only for the influence of the parasitic elements on amount of energy of the THz signal actually delivered to the MOSFET's channel and the resulting impedance as seen by any feeding structure (e.g., an external antenna). It suggests, however, that it is an oversimplification to directly employ the channel impedance of the MOSFET into calculations of the THz power that is actually transferred into the channel from an external antenna. Thus, it seems that deriving the relationship between MOSFET's responsivity and the gate bias based on such oversimplified basis will be burdened with a large error and should be avoided. With the presence of parasitic elements (mostly capacitances), a change of the impedance channel due to applied gate voltage V_{GS} hardly influences the Z_{gs} impedance, which means it is neither a way to adjust the impedance matching between the MOSFET and its antenna nor a method to change the amount of power transferred into the device.

As shown in [6], for the MOSFET operated in the non-resonant detection regime, the photo-detection signal ΔU is related to the channel voltage v_c shown in Fig. 4 and is given with the formula:

$$\Delta U = \frac{e|v_c|^2}{4\kappa k_B T} \quad (3)$$

where e is the elementary charge ($e=1.602 \times 10^{-19}$ C), κ is the transistor ideality factor (for the sake of simplicity assumed in this paper to be equal to 1), k_B is the Boltzman constant ($k_B=1.38 \times 10^{-23}$ J/K), and T is the temperature of the transistor channel.

The amplitude of the v_c voltage depends on the values of the parasitic elements as well as the channel impedance. Since the amount of parasitic losses depends on the size of the device as summarized in Table 1, an estimate of MOSFET's responsivity can be obtained by analyzing the amplitude of v_c versus W and L . Figure 6 shows the results of such an analysis made for the MOSFET represented with circuit introduced in Fig. 4, which is fed from an ideal voltage source of unit amplitude and the constant frequency $f=300$ GHz, so the applied gate voltage is $v_{gs}=\cos(2\pi f)$ [V]. The curves shown in Fig. 6 were for this reason, normalized to 1 V or the amplitude of the feeding signal; hence, the resulting unit is indicated as [V/V]. As the channel impedance, a representative value of $Z_0=371-j371 \Omega$ is assumed, which was obtained for the same parameters like the ones used to prepare graphs shown in Fig. 3. The calculations were done using a Spice-like circuit simulator. The observed fall of the channel voltage v_c for the devices of decreasing widths should be attributed to the existence in the structure of a short piece of track with sheet resistivity R_n described in Section II, which becomes pronounced particularly for narrow devices. For such cases, the in-series resistance R_n that adds to the access resistance of the channel is particularly large (being proportional to L_n which is constant for given technology and inversely proportional to W) significantly reducing the v_c voltage.

The obtained results confirm the intuitive expectation that in order to increase the responsivity of a detector of the sub-THz signals, the dimensions of the detecting device are to be minimized in order to reduce the parasitic losses. This postulate was formulated already

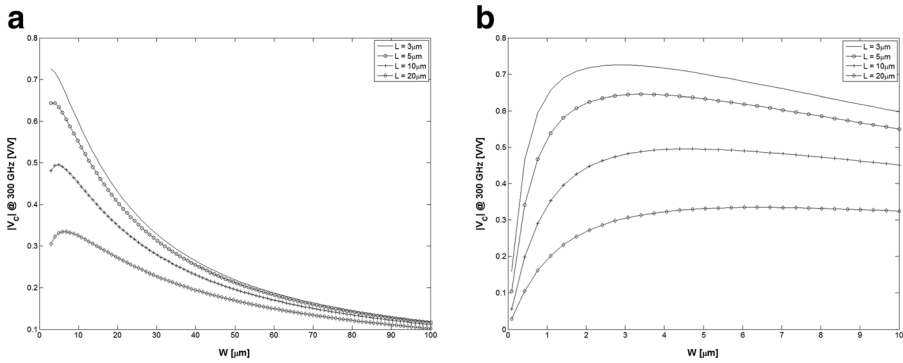


Fig. 6 Dependence of the channel voltage amplitude on the width W and length L of the device in broad range of W (a) and for a narrower range where maximum responsivities are expected (b)

in [9], where the use of small devices was suggested in order to decrease “substrate losses,” although no detailed analysis of their influence was given.

1.4 Responsivity Calculations of a MOSFET Integrated with a Patch Antenna

The results presented in Section IV confirm the predictions published in the conclusions of [12], where it was suggested that the parasitic elements present in the vicinity of the MOSFET’s channel significantly modify the input impedance as seen by the feed. The model introduced there can be employed to calculate the responsivity of a detector built of silicon-based MOSFETs of various sizes, in a procedure which to some extent resembles the approach in [13]. However, instead of the channel impedance Z_0 (as done in [12]), the $Z_{gs}(f, W, L)$ impedance calculated in Section IV should be used in order to obtain a more realistic prediction of the responsivity. Employing Eq. (3), the photo-detection voltage $\Delta U(f, W, L)$ can be found as follows:

$$\Delta U(f, W, L) = \frac{e}{4k_B T} a(f, W, L) P_R(f, W, L) \tag{4a}$$

$$a(f, W, L) = \frac{|v_c(f, W, L)|^2}{v_{gs}(f, W, L) i_g^*(f, W, L)} \tag{4b}$$

$$P_R(f, W, L) = p_{inc} A_e(f) (1 - |\Gamma(f)|^2) = p_{inc} \frac{D(f)^2 \eta \lambda^2}{4\pi} \left(1 - \left| \frac{Z_{gs}(f, W, L) - Z_A^*(f)}{Z_{gs}(f, W, L) + Z_A(f)} \right|^2 \right) \tag{4c}$$

which combined into one formula gives:

$$\Delta U(f, W, L) = \frac{e}{4k_B T} p_{inc} \frac{D(f) \eta \lambda^2}{4\pi} \left(1 - \left| \frac{Z_{gs}(f, W, L) - Z_A^*(f)}{Z_{gs}(f, W, L) + Z_A(f)} \right|^2 \right) a(f, W, L) \tag{4d}$$

where p_{inc} is the incident power density given in $[\text{W}/\text{m}^2]$, a is a proportionality factor relating the power P_{R} transferred into the Z_{gs} impedance and the squared amplitude of the channel voltage v_{c} , Z_{A} is the input impedance of the antenna as seen through the pads where the MOSFET is connected (Z^* denominates complex conjugate of Z), A_{e} is the effective aperture of the antenna defined using the D which is the power directivity of the antenna in the direction of interest (typically in the direction normal to the surface of the substrate), η —the radiation efficiency of the radiator—and λ , which is the wavelength, which depends not only on the properties of free space but also on the substrate.

To this end, a patch antenna described previously in [11] was employed. The structure was designed on a silicon-on-insulator (SOI) substrate, but a relatively thick device layer makes the technology bulk-like. A thin substrate beneath the antenna and the transistor was created in a form of a membrane by means of chemical etching with potassium hydroxide (KOH) of its back-side, which was later covered with metal. Based on analytical and numerical predictions presented in detail in [12], the substrate thickness was chosen as a compromise between suppressing substrate modes and maximizing the mechanical robustness of the structure. On a resulting 40- μm -thick sheet of dielectric, a 2-element array of rectangular patch antennas of dimensions $188.25 \times 106.45 \mu\text{m}$ was developed. The antenna top metallization is shown in Fig. 7a while the vertical cross-section of the thinned-down substrate is presented in Fig. 7b. The spacing of the radiators (equal to $203.55 \mu\text{m}$) allows exciting the MOSFET structure located between the patches with a strong out-of-phase signal coming from the opposite radiating edges. The complete structure was fabricated on a chip of dimensions $2700 \times 2550 \times 450 \mu\text{m}$. It was designed to provide maximum responsivity in a band centered on the frequency of cir. 340 GHz.

The numerical characteristics of the designed antenna were extracted by means of numerical simulation using the QuickWave 3D electromagnetic (EM) solver [20] based on the finite-difference time-domain (FDTD) algorithm applied to a complete structure including the chip. In the numerical simulation, all the dielectric media were assumed lossless, with the relative

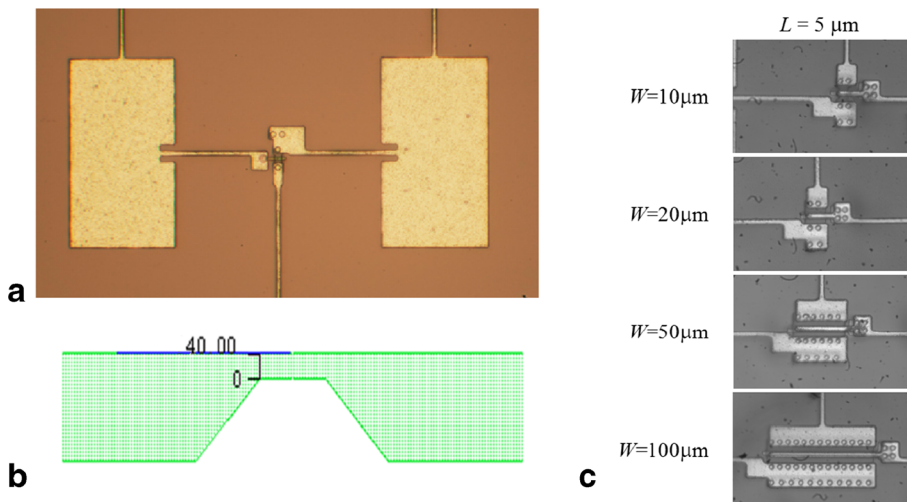


Fig. 7 A top view on the array of two patch antennae integrated with a MOSFET (a), a vertical cross-section through the locally thinned-down SOI substrate (b), and microphotographs of the MOSFETs with varying channel dimensions (c)

permittivity of silicon $\epsilon_r(Si)$ assumed to be equal to 11.65. Ideal metallization plates of zero thickness were employed, which seems to be justified since the metallization layers in the fabricated structures are made with aluminum of thickness of approx. 1 μm . The Drude model of such a conductor exhibits a rapid decrease of conductivity only well above 1 THz, which is much higher than the frequency range of interest. Figure 8a shows results obtained for the antenna array coupled to MOSFET of various sizes using Eq. (4) with incident power density p_{inc} adjusted in order to provide photo-response voltage of the order of the measurement data. A comparison between the expectations and the measurements done in a wide frequency band is shown in Fig. 8b. Three different measurement set-ups described further in this Section were employed in order to cover wider frequency range. The presented curves were all scaled linearly using the simulation data as a reference. The peak of responsivity occurs at the frequency that depends on the antenna design, which agrees quite well with expectations. The performance of the detector degrades as the frequency of the illuminating signal shifts from the operating frequency of the antenna. The undesired peaks in responsivity that are particularly well visible in data obtained with the measurement set-up 3 for frequencies above 350 GHz seem to be caused by low power level offered by the source in this range, resulting in rather poor signal to noise ratio. The unit adopted in Fig. 8 is not [V]. Instead, arbitrary unit [a.U] was used in order to stress out that the curves shown in Fig. 8b were scaled so that they can be stitched together at the boundaries of frequency ranges of respective measurement set-ups. In order to keep scaling consistent, the same scale was used also in Fig. 8a.

The maximum photo-detection voltage ΔU of a detector built of the same antenna integrated with MOSFET of channel whose dimensions vary in wide range is shown in Fig. 9a. The calculations were done for the center frequency of the structure $f=340$ GHz, which is the frequency where the peak responsivity is to be expected. The responsivity curve follows predictions made previously using the v_c voltage. Slight differences are caused by the reflection coefficient included in the calculations. Again, it confirms the intuitive expectation that the detecting device should be kept as small as possible. However, as explained previously, the decrease of the responsivity shown for small values of W results from non-optimal shape of the device where channel length exceeds its width, unnecessarily increasing the access resistances. This effect should not be mistaken for the phenomena associated with the behavior of short channel devices reported in [14] and which is correctly predicted by the

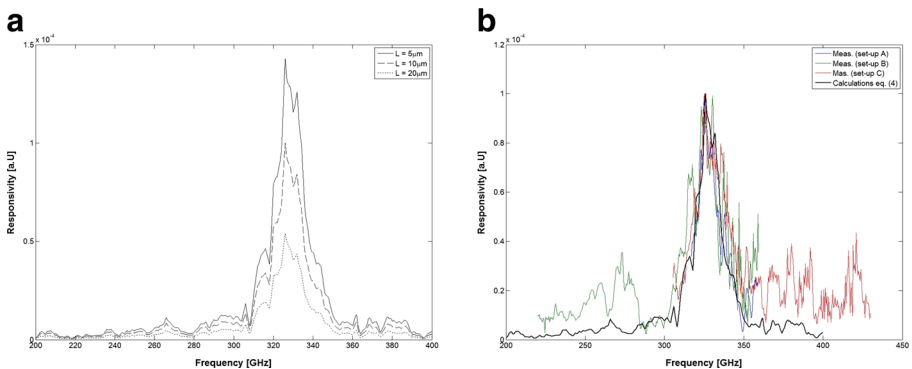


Fig. 8 Estimated responsivity of a detector built of the array antenna coupled to a MOSFET with channel width $W=10 \mu\text{m}$ (a) and comparison of data calculated for an $10 \mu\text{m} \times 10 \mu\text{m}$ exemplary structure with results obtained using three different measurement set-ups (b)

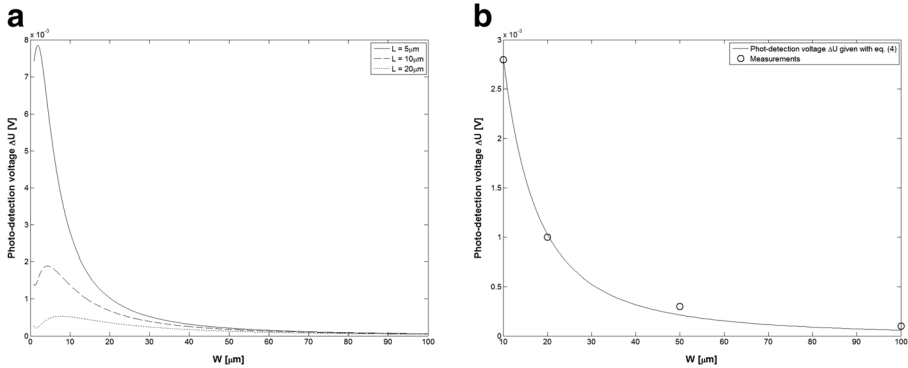


Fig. 9 Responsivity of a detector built of an antenna array integrated with MOSFETs of different dimensions calculated with Eq. (3) (a) and comparison between measurements and calculated data for a device of $L=5 \mu\text{m}$ (b)

Dyakonov-Shur theory. The effect presented here is expected to occur simultaneously to the phenomena reported in [14] if the layout of the transistor and the process parameters allow for this.

Additionally, the predictions shown in Fig. 9a were verified experimentally by obtaining responsivity estimation of four detectors built with the antenna as simulated previously, which was integrated with MOSFET of $L=5 \mu\text{m}$ and W equal to 10, 20, 50, and $100 \mu\text{m}$. The measurement set-up, shown in Fig. 10, consisted of a solid-state source (Z) from VDI, Inc., delivering a continuous signal of frequency equal to 340 GHz and the output power of approx. 1 mW to a dedicated diagonal horn antenna and into space. With a system of two mirrors (L1, L2), the beam was concentrated on a detector (T), whose photo-response voltage ΔU was measured by means of a mechanical chopper (C) and a lock-in amplifier (not shown). In order to ensure optimal positioning of the detector, it was located on a motorized XYZ stage, which allowed adjusting the location of the chip automatically. The distance between the aperture of the horn and the detector-under-test (DUT) was kept constant as well as the output power of the source, which was constantly monitored using an external pyroelectric detector (D). For each new sample, the bias voltage V_{GS} was adjusted in order to maximize the detection voltage ΔU , while the V_{DS} bias voltage was not applied. Figure 9b presents the measurement results compared with the predictions based on Eq. (4). The measurements can be fitted using a hyperbola defined as $0.1087W^{-1.563}$. The measurement data shown were obtained without applying any normalization of the DUT detection voltage ΔU . Since the aim of the experiment was not to obtain absolute responsivity of the structure in $[\text{V}/\text{W}]$ but rather to compare in the same operating conditions the performance of similar detectors differing only with the MOSFET's channel dimensions, such an approach seems justifiable. A trend that can be observed in the data shown in Fig. 9b remains independent of any scaling resulting from the procedure employed to measure the incident power. A series of measurements of several copies of each detector was performed, and the presented results are an average of the results obtained. Based on the comparison, it seems that the relatively simple model described in this section explains the results of the performed experiment reasonably well.

The procedure of adjusting the V_{GS} bias voltage to ensure maximum photo-detection voltage was required because the devices of different dimensions had slightly different threshold voltages V_t (although always close to 1 V as measured with V_{DS} kept at 0.1 V).

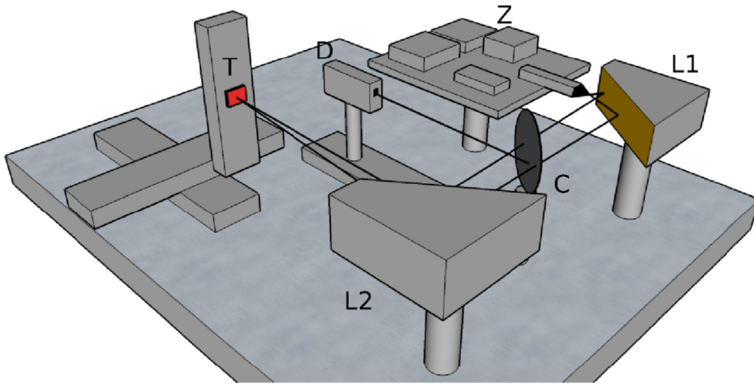


Fig. 10 The measurement set-up employed for measurements of responsivity of detectors built of an antenna array integrated with MOSFETs of various dimensions

This effect is shown in Fig. 11, where the amplitude of the detection voltage ΔU is shown for several DUTs illuminated with the THz signal using the set-up introduced in Fig. 10. As shown, the variation of the V_t voltages is not large, although adjusting the bias voltage allowed increasing the detection voltage ΔU significantly. Each channel dimension was represented by two different samples. The obtained results suggest that the different DUTs of the same channel dimensions are very similar, and the visible discrepancies can be attributed to slight differences in wirebond lengths or the non-ideal mounting of the chips in their packages.

2 Conclusions

In this paper, an analysis of parasitic elements that are found in all typical n-MOSFET devices has been performed from a viewpoint of a designer of sub-THz radiation detectors. To this end, a simplified model of the extrinsic MOSFET device has been proposed. Typical values of its

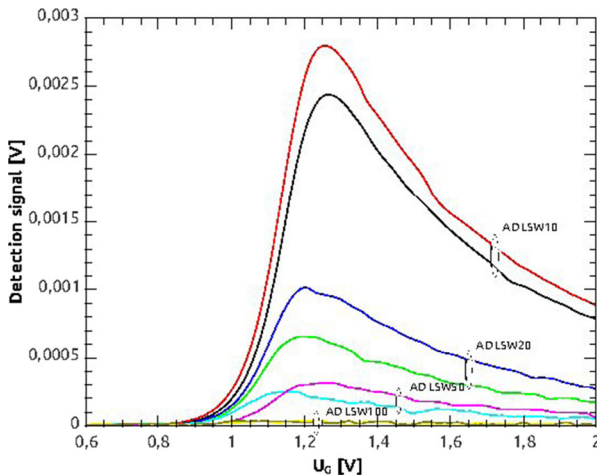


Fig. 11 The photo-detection voltage ΔU measured at the Drain-side of the DUTs of varying channel width W and $L=5 \mu\text{m}$ biased with various V_{GS} voltages

parameters have been assumed. The authors have also built a model of the MOSFET's channel (intrinsic device) employing the standard transmission line approach and defining a Z-matrix of the circuit in order to facilitate its integration with the parasitic elements. The full effective circuit model of the MOSFET has been employed to analyze the behavior of the detector when subjected to sub-THz radiation delivered through the Gate and Source pads. Finally, predictions of the responsivity of an example detector built of a typical MOSFET integrated with a patch antenna fabricated on a locally thinned SOI substrate have been compared with measurements of several structures employing MOSFETs of various channel widths. Good agreement between the predictions and the measurements has been demonstrated, which indicates that despite its simplicity, the presented model can significantly help to better understand operation of MOSFET-based detectors and also use the existing silicon-based manufacturing processes.

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