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EDITORIAL

# Semiconductor manufacturing

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Integrated circuit chip (IC) technology has changed our way of life. Computer, communication, industrial and consumer markets are all drivers of the semiconductor industry. The basic operations involved in the manufacture of semiconductors include: Crystal Production and Wafer Preparation, Mask Manufacturing, Wafer Fabrication, Packaging/Assembly, and Testing. Due to vertical disintegration of semiconductor supply chains, these operations are usually performed by separate and distinct companies. The heart of the semiconductor industry, the most capital-intensive operation, and the greatest challenge from an underwriting standpoint, is wafer fabrication. Fabrication of wafers must undergo hundreds of processes using expensive equipment with relatively short lifetime due to rapid evolution of manufacturing technologies, in which making the best use of those expensive equipments within their short lifetime to minimize the production costs has become a crucial and challenging issue. This special issue is a collection of highly selective papers addressing important issues including demand fulfillment planning, cross-company short-term capacity backup, scheduling of unrelated parallel machines, and fault detection and classification in semiconductor manufacturing.

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*Demand Fulfillment Planning in Semiconductor Manufacturing*—companies strive to enhance their capital effectiveness via managing demand fulfillment and capacity utilization to maintain their competitive advantage. This paper presents a demand fulfillment planning framework to facilitate the decision-making process regarding allocations of new tape-outs (NTOs) of forthcoming products, considering capacity backup and product reallocation to alter short-term capacity configuration, to fulfill the demands and minimize the costs. A two-stage stochastic programming demand fulfillment model was built to allocate NTOs to a number of qualified wafer fabrication facilities before the corresponding demand volume is realized and then matches fabrication facility capacity with various demands, while employing various capacity reconfiguration options. Computational results from using real data have shown viability and decision quality of this approach under different scenarios. Adopting models of the proposed two-stage stochastic programming approach in a high demand variation environment is beneficial because this approach can provide solution patterns similar to the optimal solutions of deterministic models with perfect information.

*Cross-Company Short-Term Capacity Backup in Semiconductor Industry Ecosystem*—this paper proposes a novel approach for short-term cross-company equipment backup among the semiconductor manufacturing companies that have complementary capacity configuration, while most studies focused on long-term capacity planning through optimizing the capacity investment plan or medium-term capacity allocation for demands fulfillment and loading balancing. A systematic decision approach integrating signaling game and decision tree analysis model was developed to evaluate the short-term capacity backup strategies among the fabrication facilities of different companies in semiconductor industry cluster. This approach has demonstrated its practical viability and is thus implemented in practice.

*Scheduling of Unrelated Parallel Machines in Semiconductor Manufacturing*—this paper investigates a difficult scheduling problem in a semiconductor manufacturing process that seeks to minimize the number of tardy jobs and makespan with sequence-dependent setup time, release time, due dates and tool constraints. A mixed integer programming (MIP) formulation is proposed that treats tardy jobs as soft constraints so that the minimum weighted sum of makespan and heavily penalized tardy jobs is calculated. In order to effectively reduce the size of the MIP formulation, this paper proposes a novel technique that estimates the upper bound for the number of jobs processed by a machine. For solving the real-world large scale scheduling problems, this paper gives an efficient dispatching rule that assigns the job of earliest due date to the machine with least recipe changeover (EDDLC) and try to re-optimize the solution by local search heuristics which involves interchange, translocation and transposition between assigned jobs. The computational experiments indicate that EDDLC and the proposed reoptimization techniques are very efficient and effective. In particular, EDDLC usually gives solutions very close to the exact optimum for smaller scheduling problems, and provides good solutions for scheduling up to 200 jobs on 40 machines within 10 min.

*Fault Detection and Classification in Semiconductor Manufacturing*—as the feature size and critical dimension of IC are continuously shrinking to a nano-scale

generation, it is increasingly difficult to maintain the process specification and control of the quality in wafer fabrication that consists of highly complex, interrelated, and lengthy processes. It is critical to efficiently monitor the process in real time to detect potential faults, classify them, and thus remove assignable causes effectively. This study developed a framework for semiconductor fault detection and classification to monitor and analyze the profile data of wafer fabrication from a large number of correlated process variables to eliminate the cause of the faults and thus reduce abnormal yield loss. The proposed approach integrated multi-way principal component analysis and data mining to construct the fault detection model, in which the monitoring process is based on the reduced number of key variables and the corresponding control limits, and then the derived rules were employed for fault classification. This approach is validated and implemented in real settings.

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