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Special issue with selected papers from 2018 Brazilian Symposium on Computer Engineering (SBESC 2018)

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In 2018, the Embedded Systems track of the Brazilian Symposium on Computing Systems Engineering (SBESC) received many high-quality submissions. According to the ranking produced by the Program Committee, authors of five best-ranked evaluated submissions have been invited to submit revised and extended versions of their works for consideration by this journal. After a strict review process, we selected three articles for inclusion in this special issue.

The first article is entitled "Data Clustering for Efficient Approximate Computing" by Michael Guilherme Jordan, Marcelo Brandalero, Guilherme Meneguzzi Malfatti, Geraldo Oliveira, Arthur Lorenzon, Bruno da Silva, Luigi Carro, Mateus Beck Rutzig and Antonio Carlos Schneider Beck Filho. The authors present a novel architectural technique for approximate algorithms, replacing function execution by using look-up accesses in dedicated memories. The results showed better performance compared to neural acceleration solution in terms of performance, as well as energy consumption reductions and area saving.

The second article is entitled "An Embedded Automatic License Plate Recognition System using Deep Learning" by Diogo Moury Fernandes Izidio, Antonyus Pyetro do Amaral Ferreira, Heitor Rapaela Medeiros, and Edna Natividade da Silva Barros. The authors presented a methodology to detect and recognize Brazilian license plates using conventional neural networks tailored for execution on an embedded system. The proposed method was evaluated using real case studies and presented sound results.

The third article is entitled "A Simultaneous Multithreading Processor Architecture with Predictable Timing Behavior" by Hadley Magno Siqueira and Marcio Kreutz. The authors presented Hivek-RT hardware architecture. It is a precision timed machine to enable the execution of hard-real-time and non-real-time threads in parallel. Hivek-RT is based on a customized pipeline and exposed memory hierarchy composed of scratchpads, caches, and a predictable SDRAM memory controller. Experiments were conducted to compare

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the results with other architectures in terms of overhead, performance, and footprint. The achieved values highlight the benefits of the proposed architecture.

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