Introductions to special issue on ESWEEK 2011

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1 ESWEEK 2011 special issue introduction

The Embedded Systems Week (ESWEEK) is the premier scientific event in research, design and implementation of embedded systems hardware, software and tools. ESWEEK brings together three major conferences in the embedded systems area, namely:

- CODES+ISSS (International Conference on Hardware/Software Codesign and System Synthesis, www.codes-isss.org).

R.A. Bergamaschi is Co-Editor-in-Chief.
S. Baruah and S. Fischmeister are Guest Editors and Technical Program Chairs,
EMSOFT/ESWEEK 2011.
R. Dick and J. Madsen are Guest Editors and Technical Program Chairs, CODES+ISSS/ESWEEK 2011.
R. Gupta and V. Mooney are Guest Editors and Technical Program Chairs, CASES/ESWEEK 2011.

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- CASES (International Conference on Compilers, Architecture, and Synthesis for Embedded Systems, www.casesconference.org).
- EMSOFT (International Conference on Embedded Software, www.emsoft.org).

ESWEEK 2011 was held in Taipei, Taiwan, with the sponsorship of several professional societies from the ACM (SIGBED, SIGDA, and SIGMICRO) and the IEEE (IEEE Computer Society, IEEE Circuits and Systems Society, and IEEE Council on Electronic Design Automation).

The Program Chairs from the conferences above were invited as Guest Editors and asked to select among the best papers from each conference to form this special issue. Short descriptions of their selected papers are given by the Guest Editors. The Editors-in-Chief of the Journal of Design Automation for Embedded Systems are proud to bring this special issue with some of the best papers from ESWEEK 2011.

2 EMSOFT 2011 Guest Editors' introduction (Sanjoy Baruah, Sebastian Fischmeister)

We are pleased to include in this special issue extended versions of three EMSOFT 2011 papers that really demonstrate the quality and variety of the papers accepted for the conference, ranging from real-time scheduling to model-driven development to locking protocols for embedded applications.

In the first paper, entitled "On the Hard-Real-Time Scheduling of Embedded Streaming Applications", M. Bamakhrama and T. Stefanov investigate schedulability of actor-oriented streaming applications on multiprocessor applications. The authors provide a framework for analyzing such applications and furthermore characterize two sub-classes of streaming applications that use the Cyclo-Static Dataflow model.

In the second paper, entitled "Model-based Implementation of Distributed Systems with Priorities", B. Bonakdarpour, M. Bozga, and J. Quilbeuf propose construction mechanisms for correct implementations from component-based models. The authors describe transformation techniques to implementations when using priorities in component-based models with broadcast and rendezvous interactions.

In the third paper, entitled "The OMLP Family of Optimal Multiprocessor Real-Time Locking Protocols", B. Brandenburg and J. Anderson explore efficient locking protocols especially tailored to multiprocessor systems. They specifically characterize timing aspects involved in locking protocols, propose a family of locking protocols, and empirically evaluate the proposed protocols.

3 CODES+ISSS 2011 Guest Editors' introduction (Robert Dick, Jan Madsen)

In 2011, the International Conference on Hardware/Software Codesign and System Synthesis (CODES-ISSS) received 117 technical paper submissions. We invited a selection of papers to be submitted to this special issue and two papers were ultimately accepted for publication.

The first, "Symbolic System-level Design Methodology for Multi-Mode Reconfigurable Systems" by Stefan Wildermann, Felix Reimann, Daniel Ziener, and Jürgen Teich describes a system-level design methodology that optimizes allocation, binding, and placement in systems containing partially reconfigurable field programmable gate arrays.

The second, "Virtualizing On-Chip Distributed ScratchPad Memories for Low Power and Trusted Application Execution" by Luis Angel D. Bathen, Dongyun Shin, Sung-Soo Lim, and Nikil D. Dutt describe a virtualization layer for scratchpad memories that supports priority-driven allocation, thereby enabling improvements in performance and power consumption.

We would like to thank the authors and reviewers for their efforts in making this special issue possible.

4 CASES 2011 Guest Editor's introduction (Rajesh Gupta, Vincent Mooney)

In 2011, CASES received 61 full submissions. From those submissions, four were identified as Best Paper Candidates by the program committee and thus also were invited to appear in this special issue of DAEM. We invited the authors of all four papers to submit a revised paper for consideration in this journal, and three chose to do so. After a strict review process we selected two papers for inclusion in the special issue. The excellent result is now available to the readers of DAEM!

The first paper is "Fault Buffers Enabling Near-True Voltage Scaling in Variation-Sensitive L1 Caches" by Teyyeb Mahmood and Soontae Kim. In this paper the authors propose a specialized buffer scheme to dynamically handle faults at a word-level granularity. They target voltage scaled memories and aim to mitigate the effect of parametric variations. In conclusion, the proposed Fault Buffer Array (FBA) technique of the authors provides a novel way to dynamically handle memory faults which may be more costly to eliminate using static techniques.

The second paper is "Instruction Scheduling with k-Successor Tree for Clustered VLIW Processors" by Xuemeng Zhang, Hui Wu and Jingling Xue. This paper focuses on compilation for VLIW processors using clustering. A novel approach to a priority-based, phase coupled heuristic is shown to improve basic block instruction scheduling. The approach takes into account inter-cluster communication overhead and shows results on a variety of benchmarks. The approach and associated algorithms are explained clearly and in detail.

We would like to thank the Program Committee of CASES for their hard work reviewing the papers and participating in two days of meetings to select both the papers for the conference as well as the specific best paper candidates. We also want to thank the additional reviewers who helped and the authors themselves for their contributions.

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