



An 18–28 GHz dual-mode down-converter IC for 5G applications

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Abstract

Emerging spectrum trends require a higher integration of 5G New Radio Frequency Range 1 (FR1) and Frequency Range 2 (FR2) bands to enhance the availability of spectrum and spectrum-sharing opportunities. To enable the reception of both FR1 and FR2 bands in a seamless hardware entity, we propose combining homodyne and heterodyne architectures. This necessitates the incorporation of a down-converter module that transfers the incoming signals from FR2 bands down to FR1, ensuring compatibility with an FR1 direct-conversion receiver (DCR) for the final signal reception. The primary focus of this paper is the design and implementation of the required integrated down-converter. The module includes an integrated balun, a low-noise amplifier (LNA) with a bypass mode, a dual-mode mixer, and an intermediate frequency (IF) amplifier. The introduced bypass mode helps to further elevate the linearity performance compared to the nominal mode. The bypass mode is designed for joint communication and sensing operation to avoid the compression of the receiver. This work also incorporates a local oscillator (LO) signal distribution network with phase tuning elements using a mixed-signal approach. The circuit is implemented in a 22-nm CMOS process, and the active die area is 0.6 mm². The measurements demonstrate that the implemented chip can efficiently perform the required frequency conversion over a wide frequency range of 18–28 GHz. Conversion gain of 4.5–7.5 dB, noise figure of 15–19.7 dB, 1 dB compression point (IP1dB) of –16 to –10 dBm, and input third-order intercept point (IIP3) of –5 to 0 dBm are achieved. The measured IP1 dB and IIP3 for the bypass mode are +0.5 to +4.5 dBm and +8.5 to +10 dBm, respectively.

Keywords 5G · Down-converter · Frequency converter · Heterodyne · Joint communication and sensing · Millimeter wave · Modular receiver · New radio (NR)

1 Introduction

5 G communication brings new features and applications to the users, such as high data-rate communication, sensing and security, industrial 5G, health and medical, and transceivers requiring ultra-low latency and high reliability. Millimeter wave frequency operation together with array transceivers will be widely utilized in future products. Within 3GPP standardization, first step is to shift to the FR2 band at 24.2–52.6 GHz [1]. Although several receiver front-ends have been published in the literature for either FR1 [2–4]

or FR2 [5–16], none of them can cover both FR1 and FR2 bands in one system. In the context of emerging spectrum trends, the combination of FR1 and FR2 bands increases the availability of spectrum and spectrum-sharing opportunities. This provides deployment flexibility, enhanced coverage (through the low frequency band FR1), and higher data rates (through the mmWave band FR2) for a 5G communication system. Therefore, developing hardware-efficient methods to enable communication over both FR1 and FR2 bands within a seamless hardware entity is a valid research direction for future 5G systems.

Our solution to cover both FR1 and FR2 bands is illustrated in Fig. 1. In this approach, the down-converter module converts the signal from FR2 bands down to the FR1 band in such a way that an FR1-compatible direct-conversion receiver (DCR) will follow for the final signal reception. In our approach, we convert the FR2 band signal down to 1–7 GHz which enables wideband signal

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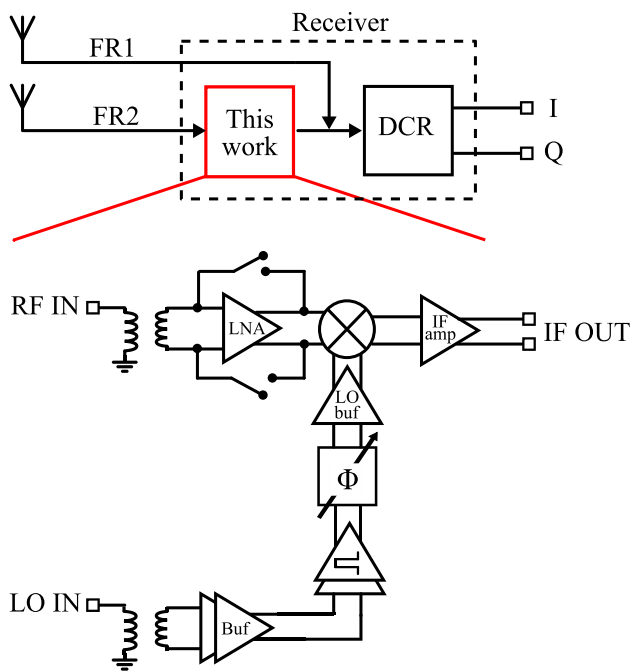


Fig. 1 Concept of a 5G receiver for both FR1 and FR2 bands, and the structure of the implemented FR2 down-converter module

feed to the output. The module is a frequency converter consisting of an integrated balun, an LNA with a bypass mode, a dual-mode mixer, an IF amplifier, and an LO signal chain. The module has intentionally low gain and thus high linearity, to enable operation with a lower probability of compression in a hostile radio environment. Furthermore, it incorporates a bypass mode, as depicted in Fig. 1, in which the LNA is bypassed to further elevate linearity, and the dual-mode mixer is configured for passive operation. The bypass mode is used to avoid the compression of the receiver due to strong transmitter leakage during radar full-duplex operation for joint communication and sensing systems [17, 18].

We have designed a proof-of-concept IC for the down-converter module, fabricated on a 22-nm CMOS process. The circuit occupies an active die area of 0.6 mm² and operates over a frequency range of 18–28 GHz. Conversion gain of 4.5–7.5 dB, noise figure of 15–19.7 dB, 1-dB compression point (IP1dB) of –16 to –10 dBm, and input third-order intercept point (IIP3) of –5 to 0 dBm are achieved. The measured IP1 dB and IIP3 for the bypass mode are +0.5 to +4.5 and +8.5 to +10, respectively. In Chapter II we describe the down-converter architecture in detail and Chapter III covers the circuit implementation. Chapter IV represents the measurement results and finally, Chapter V concludes the paper.

2 Architecture

Figure 1 presents the overall system-level concept as well as the structure of the implemented down-converter module including the RF, LO, and IF blocks. The module is designed to work at 5G NR FR2 bands with a heterodyne operation, where the down-converted FR2 signals along with the received FR1 signals will be processed through a direct conversion receiver. The single-to-differential transformer and LNA are the first two stages of the implemented structure. The intention for employing an integrated transformer is to decouple the bonding pads from the gate terminals of the input transistors without using any electrostatic discharge (ESD) diodes. The LNA is followed by a double-balanced Gilbert-cell based mixer for down-converting the RF input signal to the desired IF. Finally, the last stage of the designed structure is a super-source-follower type IF-amplifier that provides a matched impedance for the IF output of the down-converter. This work also represents an inverter-based LO chain. Such a circuitry is usually designed by analog techniques for operation above 10 GHz, see e.g. [12, 19]. However, the deep submicron CMOS technology offers transit frequencies and maximum oscillation frequency of several hundreds of gigahertz [20], promoting the operation of the digital circuits above 10 GHz. The presented LO signal chain is designed by applying the mixed-signal techniques to explore this opportunity.

While operating at the highly occupied radio spectrum of modern urban environment, a radio receiver can potentially be affected by hostile signals from the nearby transmitters that can compress the signal path [21]. Furthermore, during radar-mode operation in joint sensing and communications scheme, strong signal may enter the receiver and the receiver needs to avoid compression. On the other hand, in this scenario sensitivity is not a major issue and we can tolerate high noise figure. As a counter-action for this issue an additional operating mode is implemented that can bypass the amplification stages and improve the linearity of the receiver. The mode control functionality of the proposed mixer is accomplished by switching between the resistive and capacitive loads in the IF outputs as well as whether or not to bypass the input transconductance stage of the mixer. In the nominal mode, the bypass switches around the LNA shown in Fig. 1 are open and the LNA can provide its nominal amplification. The next stage mixer is also configured to operate as an active mixer. In the bypass mode of operation, on the other hand, the bypass switches around the LNA are enabled and the input signal is directly applied to the common source nodes of the mixer's switching quad and in this way, the preceding gain stages including the LNA and the

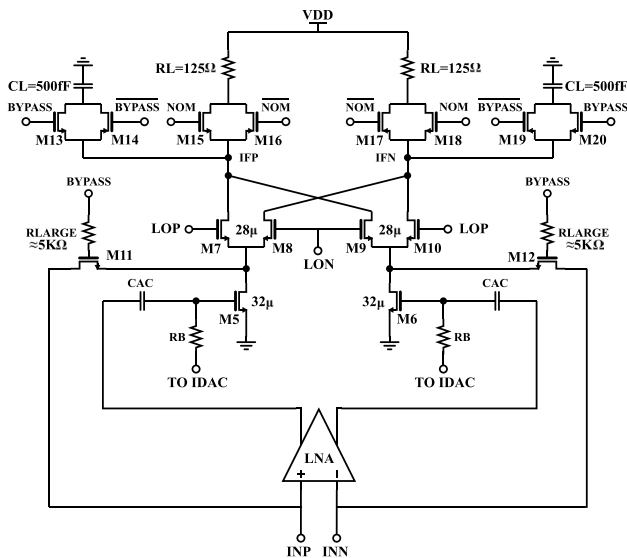


Fig. 3 Overall structure of the dual mode mixer

Table 1 Configuration of the switches

Switch	Nominal mode	Bypass mode
NOM	ON	OFF
$\overline{\text{NOM}}$	OFF	ON
BYPASS	OFF	ON
$\overline{\text{BYPASS}}$	ON	OFF

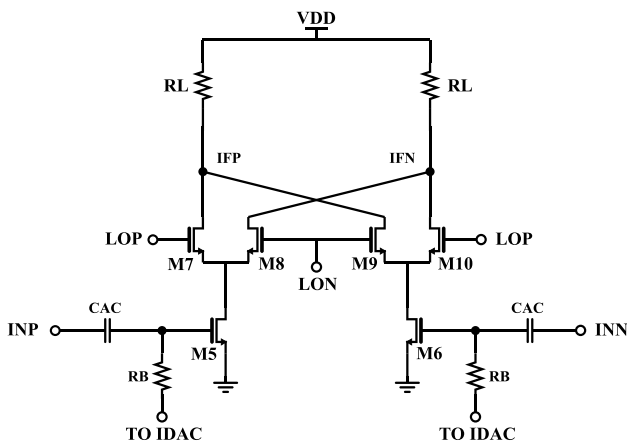


Fig. 4 Down-conversion mixer: nominal mode

and consequently, the mixer operates as an active mixer. The implemented mixer in the nominal mode involves three main stages: input transconductance stage (M5, M6), switching stage (M7, M8, M9, M10), and load stage (RL). Resistive loads are preferred over the active load counterparts to provide a wider bandwidth for the mixer in the nominal mode. Transistors M5 and M6 are biased in

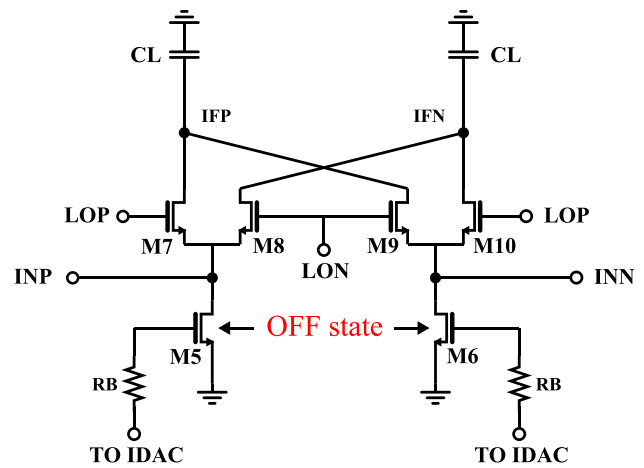


Fig. 5 Down-conversion mixer: bypass mode

the saturation region to provide enough gain for the input signal. On the other hand, the switch transistors, M7–M10, are all biased to conduct but near the pinch-off region to act as switches [27].

3.2.2 Bypass mode

By enabling the bypass mode according to the requirements mentioned in Table 1, the structure of the mixer can be redrawn as shown in Fig. 5. In the bypass mode, the input signal is directly applied from the output of the integrated transformer to the common-source nodes of the switching quad and in this way, the preceding gain stages are all bypassed. This will relax the saturation challenge of the down-converter in the presence of strong interferer. The mixer will also have capacitor loads enabled in this mode and since the transconductance has already been bypassed, there is no DC current flowing through the mixing quad. As a result, the mixer will operate in the passive mode with a good linearity performance as required in the bypass mode.

Passive mixers can operate in either ON or OFF overlap region depending on the dc gate bias of the switching quad. The ON overlap operation is preferred in the proposed structure since it is the desirable region from a linearity perspective [28]. In addition to the linearity performance, the input matching is another important parameter that should be taken into account since with the LNA bypassed the mixer is the first stage of the down-converter in the bypass mode. The required input matching is provided by a series combination of ON resistance of the switch transistors and scaled version of IF impedance formed by the implemented load capacitors (CL). These IF capacitors will also improve the linearity performance of the mixer by attenuating the out-of-band blockers [29, 30].

3.3 IF amplifier

The last circuit block of the implemented down-converter is the IF amplifier stage, which is shown in Fig. 6. This stage provides the required output matching for the implemented module. It also provides IF gain for the desired IF band as well as a sufficient suppression for the out-of-band interferences by the low-pass behavior. The proposed IF amplifier has a two-stage configuration composed of a super source follower followed by a self-biased inverter stage. The super-source follower is selected as the input stage because it provides wider bandwidth compared to the conventional common drain structure. The high input impedance of the super-source follower stage also prevents any loading effect and signal degradation on the mixer’s output side. The output stage of the proposed IF amplifier is a self-biased inverter that provides few dB IF-signal amplification and a driving capability to external load. During the design phase the high-frequency non-ideal effects imposed by the chip pads, bonding wires, PCB pads, and PCB traces were taken into account while designing the proposed IF amplifier stage to be matched to a 50Ω load.

3.4 LO chain

Figure 7 illustrates the block diagram for the LO signal chain. It was designed by applying mixed-signal techniques, and it serves as a step to analyze the feasibility of digital circuits operating above 10 GHz. The LO chain targets to provide

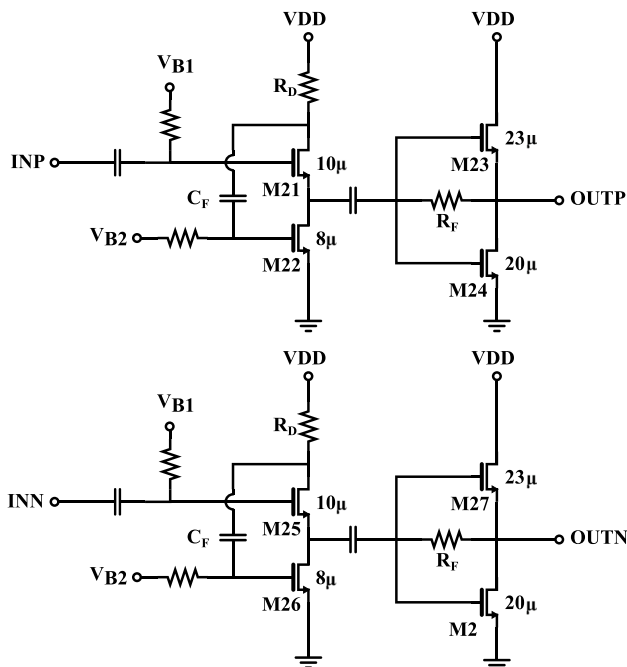


Fig. 6 Overall structure of the IF amplifier

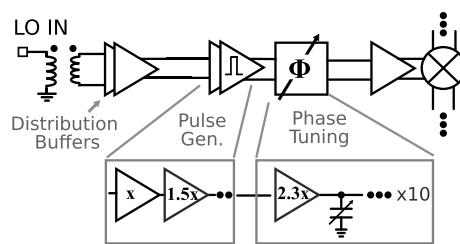


Fig. 7 LO-signal chain

rail-to-rail signals for switching of mixers operating between 12 and 25 GHz LO frequency. It also incorporates varactor-based phase-tuning, to calibrate phase mismatches and study the possibility of LO phase-tuning for phased arrays.

The reference LO signal is fed in through a single-to-differential transformer and distributed across the chip with buffers. Located close to the mixers, pulse generation is the first block in the LO chain. At frequencies above 10 GHz, rail-to-rail signal generation and propagation requires special design considerations. The RC time-constant contributed by the load, interconnect and transistor parasitics limits the driving capability of CMOS circuits. Inverters are chosen as the building block for the LO signal chain as they present the smallest possible load. Pulse generation consists of a chain of inverters, and each inverter drives a load of 1.5 times its size. The inverter loading has been limited to allow amplification of the LO signal to create required waveforms.

The pulse generator is followed by a phase-tuning element, which is composed of a series of 10 inverter-varactor pairs. The varactors are driven by 2.3 times the minimum-sized inverter to maintain signal integrity at the highest frequency of the range, as well as drive the mixers. Digital controls (0,1) enable 1-bit of tuning control in each pair. The varactor-tuning block can calibrate phase mismatches between LO_p and LO_n signals or can serve phase-tuning for possible beamforming application. Figure 8 shows the post-layout simulation results at for the presented LO chain to demonstrate its phase-tuning capability. Here, one of the differential input signal LO_p is phase-tuned by progressively changing varactor controls from V_{DD} to ground. Overall delay tuning is 13 ps. This would correspond to a 30° beamsteering angle in a typical 2×2 sub-array antenna at 28 GHz. These results indicate that the mixed-mode design methodology is feasible, yet the performance of this demonstration calls for improvements.

4 Measurements

Figure 9 presents layout and microphotograph of the chip fabricated on a 22-nm CMOS process with a size of 1.25 mm \times 1.25 mm including pads. RF transformer, LNA, mixer, IF

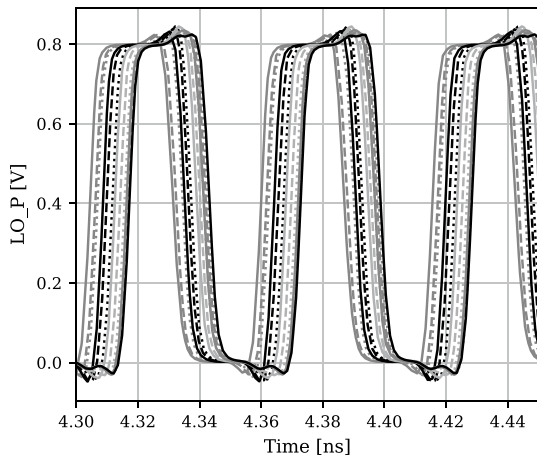


Fig. 8 Simulated time-domain waveforms for phase-tuning at 18 GHz

amplifier, and LO related blocks are the main elements of the receive path and are specified using red colored rectangles on the die microphotograph. Active die area is 0.6 mm². The implemented IC also includes two TX up-converting elements that are not the subject of this paper. The simplified measurement setup of the implemented down-converter is depicted in Fig. 10. The RF and LO inputs are provided using ground-signal-ground (GSG) probes through the custom designed low-parasitic pads. The EM-simulated parasitic capacitance of these mmw pads are only 20 fF. The IF outputs, on the other hand, are wire-bonded to the PCB and a micro-strip transmission line pair is employed to route them to the edge SMA connectors. Other lower frequency signals, including reference current, DC power supplies and SPIs are also provided through the PCB traces.

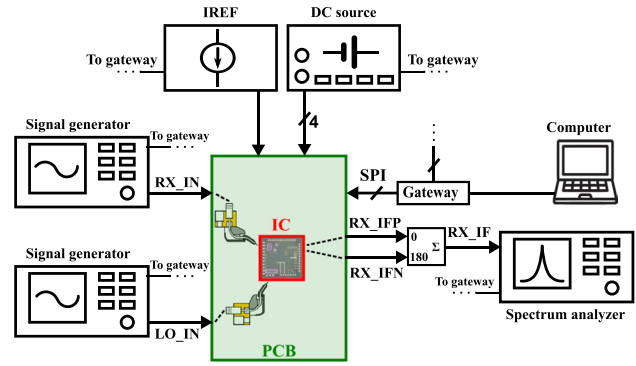


Fig. 10 Simplified measurement setup (CG)

The functionality of the implemented down-converter module in both nominal and bypass modes was investigated through various measurements. Figure 11 shows the measured return loss at the RF input. The implemented on-chip transformer along with the input matching network of the nominal mode can preserve $S_{11} < -10$ dB in a wide range of frequencies starting from 20 GHz up to 30 GHz. On the other hand, the input matching in the bypass mode is mostly defined by the on-chip transformer and the input impedance of the passive mixer. The measured S_{11} of the bypass mode verifies that the input power in this mode can also be efficiently transferred into the chip in a wide range of frequencies as nominal mode.

The measured conversion gain and noise figure of the module with an IF frequency of 7 GHz are shown in Fig. 12. The receive path can provide a conversion gain of 2.5–7.5

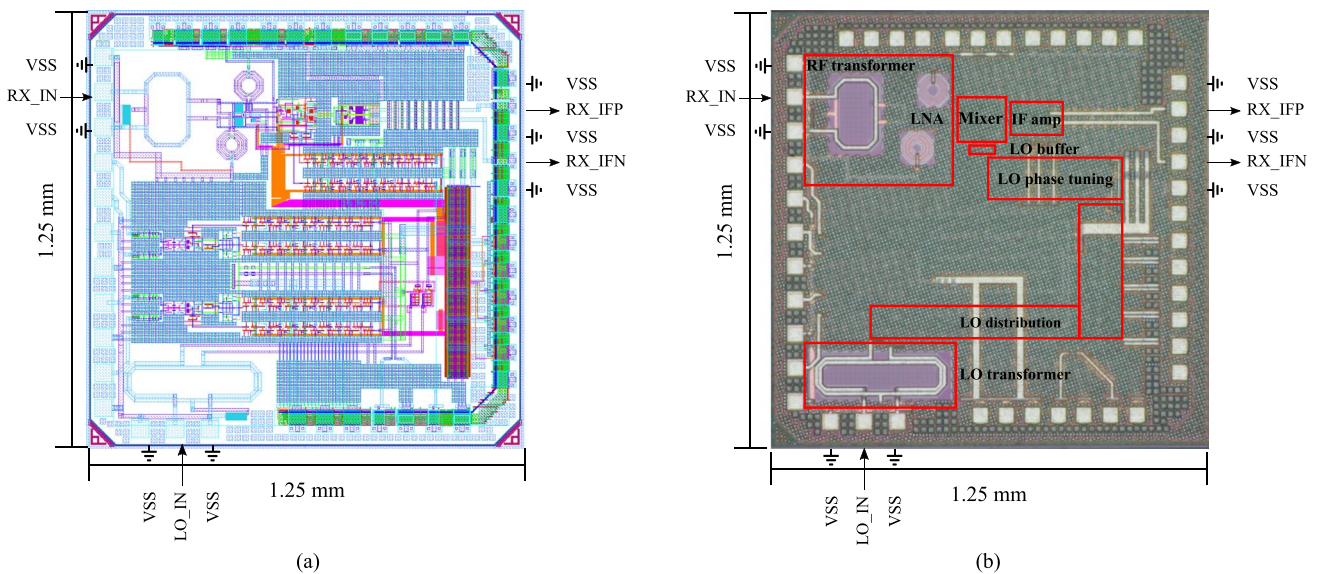


Fig. 9 Layout of the implemented down-converter IC (a), microphotograph of the implemented down-converter IC (b)

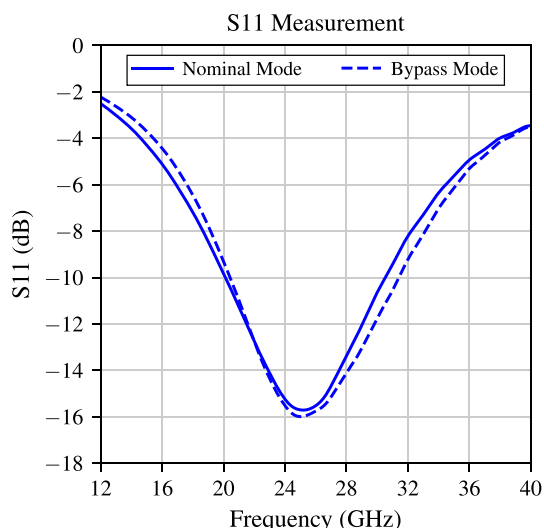


Fig. 11 Measured S11 in both modes of operations

dB and a noise figure of 15–20 dB over the frequency range in the nominal mode of operation. By enabling the bypass mode, the LNA and transconductance stage of the mixer are disabled and in this way, a good linearity performance at the cost of lower gain and higher noise figure is achieved from the bypass mode. As can be seen from Fig. 12, the bypass mode reduces the nominal conversion gain of the down-converter by about 18dB over the frequency range.

Finally, Fig. 13 presents the measured linearity performance of the implemented module, where the IIP3 is

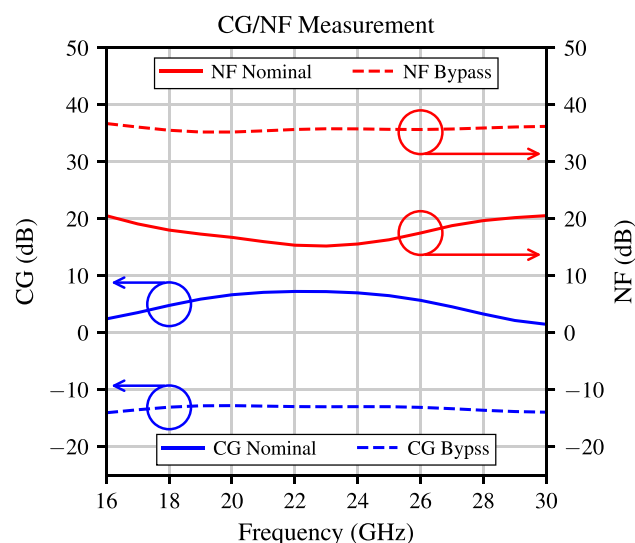


Fig. 12 Measured conversion gain and noise figure in both modes of operations

measured using a two-tone separation of 100 MHz. The input P1dB is -16 to -10 dBm and the in-band IIP3 is -5 to 0 dBm at 18–28 GHz for the nominal mode of operation. For the bypass mode of operation, the input P1dB is $+0.5$ to $+4.5$ dBm and the in-band IIP3 is $+8.5$ to $+10$ dBm at 18–28 GHz. Performance summary and comparison with other down-converters in the same frequency range are provided in Table 2. As it can be seen, the implemented chip can achieve state of the art level performance metrics while providing a dual-mode operation at millimeter wave ranges.

5 Conclusions

In this paper, a modular receiver architecture to enable the reception of input signals from both FR1 and FR2 bands using an hardware-efficient approach is presented. As the main requirement to achieve this goal, we have designed and implemented a proof-of-concept down-converter module that converts the signal from FR2 bands down to FR1. The measurement results show that the required frequency conversion is successfully implemented and a CG of 4.5–7.5 dB, NF of 15–19.7 dB, IP1dB of -16 to -10 dBm, and IIP3 of -5 to 0 dBm were achieved for the proposed down-converter module over a wide frequency range of 18–28 GHz. The module also offers a bypass mode in addition to the nominal mode where even a higher linearity is achieved by bypassing the gain stages of the structure. The measured IP1dB and IIP3 for the bypass mode are $+0.5$ to $+4.5$ and $+8.5$ to $+10$, respectively.

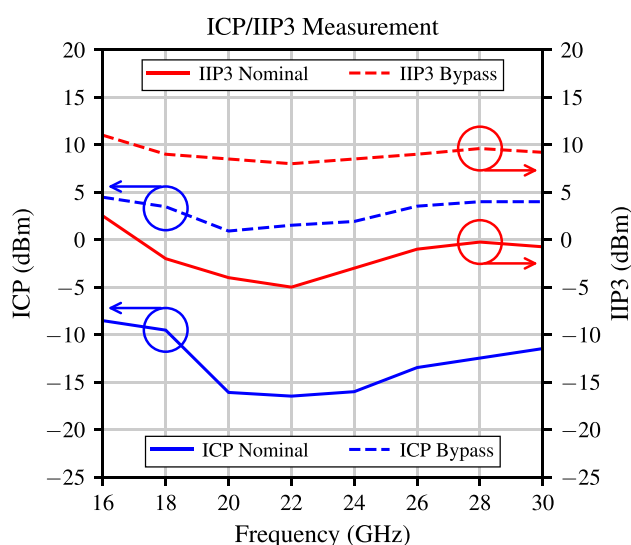


Fig. 13 Measured 1-dB compression point and IIP3 in both modes of operations

Table 2 Performance summary and comparison with millimeter wave down-converters

	This work	[31] ICMMT 2022	[32] AICSP 2022	[33] EuMIC 2022	[34] IMS 2021	[35] RFIC 2021	[36] TCAS-II 2021	[37] TVLSI 2017
Process (CMOS)	22 nm	65 nm	180 nm	65 nm	130 nm	130 nm	65 nm	65 nm
Supply (V)	0.9	1.1	1.8	1	1.5	2.7	1	1.2
RF Freq (GHz)	18–28	20–55	5	30–38	23–25	24–30	24–40	21.5–32.5
IF Freq (GHz)	1–7	2	0–0.1	1	0.1	2–5	N/A	0.001
CG (dB)	4.5–7.5	2.41	6 ²	4.3	1.3–3	– 1	7.2 ³	15.5
NF (dB)	15–20	12.6–14.7 ²	21 ²	21	15.2–19.3	< 15	12.3 ³	11–20.5
S11 (dB)	< – 8	N/A	N/A	N/A	< – 10	< – 10	N/A	< – 10
IP1dB (dBm)	– 11 ± 4 ¹	–11.3	+1.9 ²	– 1	–0.6–0	N/A	–6.1 ³	N/A
IIP3 (dBm)	– 1 ± 10 ¹	N/A	+10.6 ²	+ 4	N/A	> + 14.5	–2.5 ³	(– 1.9)–(+8.8)
Integration	LNA + Mixer + IF buf + LO	Mixer + IF buf + LO	Mixer	Mixer + IF buf + LO	Mixer + IF buf + LO	T/R SW + Mixer +IF buf+LO	Mixer + IF buf	LNA + Mixer + IF buf
Power (mW)	RX = 14.8/6.5 ¹	7.48	6.64 ²	10.4	10.5	210	10.3	7.1
Area (mm ²)	0.6	0.25	N/A	0.44	0.6	N/A	0.4	0.88

¹Nominal mode result/Bypass mode result²Simulation result³Measured at 28 GHz RF frequency

Author Contributions SN: Mixer Design, Top-level arrangements, Tape-out activities, IC measurements kaisa ryynanen: LNA design, Transformer design, Tape-out activities MZ: LO design, Tape-out activities AK: IF amp design, Tape-out activities KS: Senior designer for microwave support, System design, Top-level arrangements, Tape-out activities MK: Senior designer for digital support (SPI, IO ring), System design, Top-level arrangements, Tape-out activities vishnu unnikrishnan: System design, Top-level arrangements. LA: System design (communication aspects) MV: System design (communication aspects) JR: Main supervisor of the project

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Declarations

Conflict of interest The authors declare no competing interests.

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References

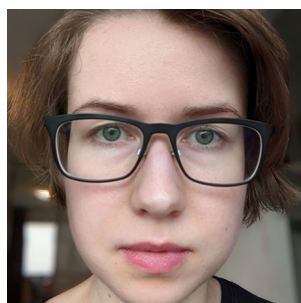
- 3GPP. (2019). User Equipment (UE) radio transmission and reception; Part 3: Range 1 and Range 2 Interworking operation with other radios (Release 16). 3GPP TS 38.101-3.
- Lee, J., Han, S., Lee, J., Kang, B., Bae, J., Jang, J., et al. (2019). A Sub-6-GHz 5G new radio RF Transceiver Supporting EN-DC With 3.15-Gb/s DL and 1.27-Gb/s UL in 14-nm FinFET CMOS. *IEEE Journal of Solid-State Circuits*, 54(12), 3541–3552. <https://doi.org/10.1109/JSSC.2019.2938132>
- Zahra, M., Kempf, I., Haarla, J., Antonov, Y., Khonsari, Z., Mii-lunpalo, T., et al. (2020). A 2-5.5 GHz beamsteering receiver IC with 4-element vivaldi antenna array. *IEEE Transactions on Microwave Theory and Techniques*, 68(9), 3852–3860. <https://doi.org/10.1109/TMTT.2020.2986754>
- Lee, J., Kang, B., Joo, S., Lee, S., Lee, J., Kang, S., Jo, I., Ahn, S., Lee, J., Bae, J. & Ko, W., (2021). A low-power and low-cost 14nm FinFET RFIC supporting legacy cellular and 5G FR1. In *Proceeding IEEE international solid-state circuits conference*; p. 90–92.
- Kodak, U., & Rebeiz, GM. (2016). A 42mW 26-28 GHz phased-array receive channel with 12 dB gain, 4 dB NF and 0 dBm IIP3 in 45nm CMOS SOI. In *Proceeding IEEE radio frequency integrated circuits symposium (RFIC)*; p. 348–351.
- Yeh, Y. S., Walker, B., Balboni, E., & Floyd, B. (2017). A 28-GHz phased-array receiver front end with dual-vector distributed beamforming. *IEEE Journal of Solid-State Circuits*, 52(5), 1230–1244. <https://doi.org/10.1109/JSSC.2016.2635664>
- Garg, R., & Natarajan, A. S. (2017). A 28-GHz low-power phased-array receiver front-end with 360° rtps phase shift range. *IEEE Transactions on Microwave Theory and Techniques*,

- 65(11), 4703–4714. <https://doi.org/10.1109/TMTT.2017.2707414>
8. Ding, Y., Vehring, S., Maurath, D., Gerfers, F., & Boeck, G. (2017). IEEE transactions on microwave theory and techniques. In *Proc. Asia-Pacific Microw. Conf.*, p. 1226–1229.
 9. Kim, H. T., Park, B. S., Song, S. S., Moon, T. S., Kim, S. H., Kim, J. M., et al. (2018). A 28-GHz CMOS direct conversion transceiver with packaged 2×4 antenna array for 5G cellular system. *IEEE Journal of Solid-State Circuits*, 53(5), 1245–1259. <https://doi.org/10.1109/JSSC.2018.2817606>
 10. Mondal, S., Singh, R., Hussein, A. I., & Paramesh, J. (2018). A 25–30 GHz fully-connected hybrid beamforming receiver for MIMO communication. *IEEE Journal of Solid-State Circuits*, 53(5), 1275–1287. <https://doi.org/10.1109/JSSC.2018.2789402>
 11. Kim, S., Kim, B., Lee, Y., Kim, S., & Shin, H. (2019). A 28GHz Direct Conversion Receiver in 65nm CMOS for 5G mmWave Radio. In *Proceeding 2019 international Soc design conference* p. 29–30.
 12. Pang, J., Wu, R., Wang, Y., Dome, M., Kato, H., Huang, H., et al. (2019). A 28-GHz CMOS phased-array transceiver based on LO phase-shifting architecture with gain invariant phase tuning for 5G new radio. *IEEE Journal of Solid-State Circuits*, 54(5), 1228–1242. <https://doi.org/10.1109/JSSC.2019.2899734>
 13. Shakib, S., Elkholy, M., Dunworth, J., Aparin, V., & Entesari, K. (2019). A wideband 28-GHz transmit-receive front-end for 5G handset phased arrays in 40-nm CMOS. *IEEE Transactions on Microwave Theory and Techniques*, 67(7), 2946–2963. <https://doi.org/10.1109/TMTT.2019.2913645>
 14. Shimura, T., Ohshima, T., & Ohashi, Y. (2019). A 28-GHz Phased-array Receiver with an On-chip BIST Function by using a Shielded Symmetrical Signal Distributor. In *2019 49th European Microwave Conference (EuMC)*, p. 618–621.
 15. Krishnamurthy, S., & Niknejad, AM. (2020). 10-35GHz passive mixer-first receiver achieving +14dBm in-band IIP3 for digital beam-forming arrays. In *2020 IEEE radio frequency integrated circuits symposium (RFIC)* p. 275–278.
 16. Singh, R., Mondal, S., & Paramesh, J. (2020). A millimeter-wave receiver using a wideband low-noise amplifier with one-port coupled resonator loads. *IEEE Transactions on Microwave Theory and Techniques*, 68(9), 3794–3803. <https://doi.org/10.1109/TMTT.2020.2985676>
 17. Barneto, C. B., Riihonen, T., Turunen, M., Anttila, L., Fleischer, M., Stadius, K., et al. (2019). Full-duplex OFDM radar with LTE and 5G NR waveforms: challenges, solutions, and measurements. *IEEE Transactions on Microwave Theory and Techniques*, 67(10), 4042–4054. <https://doi.org/10.1109/TMTT.2019.2930510>
 18. Barneto, C. B., Liyanaarachchi, S. D., Heino, M., Riihonen, T., & Valkama, M. (2021). Full duplex radio/radar technology: The enabler for advanced joint communication and sensing. *IEEE Wireless Communications*, 28(1), 82–88. <https://doi.org/10.1109/MWC.001.2000220>
 19. Wu, L., Leung, H. F., Li, A., & Luong, H. C. (2017). A 4-element 60-GHz CMOS phased-array receiver with beamforming calibration. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 64(3), 642–652. <https://doi.org/10.1109/TCSI.2016.2612232>
 20. Jan, CH., Agostinelli, M., Deshpande, H., El-Tanani, MA., Hafez, W., Jalan, U., et al. (2010). RF CMOS technology scaling in High-k/metal gate era for RF SoC (system-on-chip) applications. In *2010 international electron devices meeting*, p. 27.2.1–27.2.4.
 21. Goel, A., Analui, B., & Hashemi, H. (2012). A 130-nm CMOS 100-Hz-6-GHz reconfigurable vector signal analyzer and software-defined receiver. *IEEE Transactions on Microwave Theory and Techniques*, 60(5), 1375–1389. <https://doi.org/10.1109/TMTT.2012.2190091>
 22. Zhuo, W., Embabi, S., de Gyvez, JP., & Sanchez-Sinencio, E. (2000). Using capacitive cross-coupling technique in RF low noise amplifiers and down-conversion mixer design. In *Proceedings of the 26th European solid-state circuits conference*, p. 77–80.
 23. Zhuo, W., Li, X., Shekhar, S., Embabi, S. H. K., Pineda de Gyvez, J., Allstot, D. J., et al. (2005). A capacitor cross-coupled common-gate low-noise amplifier. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 52(12), 875–879.
 24. Shekhar, S., Walling, J. S., & Allstot, D. J. (2006). Bandwidth extension techniques for CMOS amplifiers. *IEEE Journal of Solid-State Circuits*, 41(11), 2424–2439. <https://doi.org/10.1109/JSSC.2006.8833336>
 25. Li, X. J., & Zhang, Y. P. (2010). Flipping the CMOS switch. *IEEE Microwave Magazine*, 11(1), 86–96. <https://doi.org/10.1109/MMM.2009.935203>
 26. Balasubramanian, A., & Bellaouar, A. (2018). RF/mmWave Front-End Module Switch in 22nm FDSOI Process. In *2018 IEEE SOI-3D-subthreshold microelectronics technology unified conference*, p. 1–2.
 27. Lin, C., Wu, P., Chang, H., & Wang, H. (2006). A 9–50-GHz Gilbert-cell down-conversion mixer in 0.13- μ m CMOS technology. *IEEE Microwave and Wireless Components Letters*, 16(5), 293–295. <https://doi.org/10.1109/LMWC.2006.873492>
 28. Kim, J., & Silva-Martinez, J. (2013). Low-power, low-cost CMOS direct-conversion receiver front-end for multistandard applications. *IEEE Journal of Solid-State Circuits*, 48(9), 2090–2103. <https://doi.org/10.1109/JSSC.2013.2265781>
 29. Andrews, C., & Molnar, A. C. (2010). A passive mixer-first receiver with digitally controlled and widely tunable RF interface. *IEEE Journal of Solid-State Circuits*, 45(12), 2696–2708. <https://doi.org/10.1109/JSSC.2010.2077151>
 30. Mirzaei, A., & Darabi, H. (2011). Analysis of imperfections on performance of 4-phase passive-mixer-based high-Q bandpass filters in SAW-less Receivers. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 58(5), 879–892. <https://doi.org/10.1109/TCSI.2010.2089555>
 31. Dai, Y., Wen, J., & Jin, N. (2022). A 20–55 GHz broadband low-power down-conversion mixer using 65-nm CMOS technology. In *2022 international conference on microwave and millimeter wave technology (ICMMT)*, IEEE. p. 1–3.
 32. Altuner, E., Özoğuz, I. S., & Yelten, M. B. (2022). High-linearity Gilbert-cell mixer design for cryogenic applications. *Analog Integrated Circuits and Signal Processing*, 113(2), 249–256.
 33. Li, M. H., Chen, C. N., Wang, Y., & Wang, H. A. (2021). 30-to-38 GHz active and passive combined down-conversion variable gain mixer with low OP 1dB variation in 65-nm CMOS. In *16th European microwave integrated circuits conference (EuMIC)*. IEEE, 2022, 55–58.
 34. Pan, J., He, J., Peng, Y., Wang, H., Chang, S., Huang, Q., & Li, J. (2021). A K-band active up/down bidirectional mixer in 130-nm CMOS. In *2021 IEEE MTT-S international microwave symposium (IMS)*, (pp. 294–296). IEEE
 35. Paidimarri, A., Yoshiyama, M., Plouchart, J. O., Valdes-Garcia, A., Lee, W., Okuyama, Y., et al. (2021). A High-Linearity, 24–30 GHz RF, Beamforming and Frequency-Conversion IC for Scalable 5G Phased Arrays. In *2021 IEEE radio frequency integrated circuits symposium (RFIC)* p. 103–106.
 36. Bae, B., & Han, J. (2021). 24–40 GHz gain-boosted wideband CMOS down-conversion mixer employing body-effect control for 5G NR applications. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 69(3), 1034–1038.
 37. Li, C. H., Ko, C. L., Kuo, M. C., & Chang, D. C. (2017). A 7.1-mW K/K_a -band mixer with configurable bondwire resonators in 65-nm CMOS. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 25(9), 2635–2648. <https://doi.org/10.1109/TVLSI.2017.2703807>

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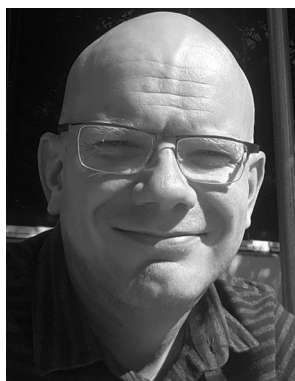


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