An LO phase shifter with frequency tripling and phase detection in 28 nm FD-SOI CMOS for mm-wave 5G transceivers

Rikard Gannedahl[1] · Henrik Sjöland[1]

Abstract

This paper presents an LO phase shifter with frequency tripling for 28-GHz 5G transceivers. The phase shifting and frequency tripling are achieved using an injection-locked oscillator and injection-locked frequency tripler, respectively. A phase detector based on third harmonic mixing is also implemented and is used to detect the applied phase shift, supporting automatic calibration of the phase shifter. Additionally, an algorithm to automatically tune the oscillators to their respective locking frequency is presented. To test the phase shifter, a 24–30-GHz sliding-IF receiver is implemented. Simulations show that a > 360° tuning range over the full 24–30 GHz span is achieved, with a gain variation of 0.11 dB or less, and that the phase detector has an rms phase error of < 2.5°. The circuit is implemented in a 28nm FD-SOI CMOS process and the entire chip measures 1080 μm × 1080 μm, including pads, and consumes 27–29 mW from a 1 V supply.

Keywords Beamforming · mmWave · Phase shifter · Frequency multiplier · Injection locking

1 Introduction

To account for the ever-increasing needs for mobile data, the fifth generation of cellular network technology (5G) has enabled the use of mm-wave frequencies for mobile communication, i.e., frequencies between 30 and 300 GHz. Since the mm-wave spectrum is mostly unoccupied, very large bandwidths can be allocated to each user [1]. For instance, the first commercial bands operating at 24–30 GHz and 37–43.5 GHz offer up to 400 MHz of bandwidth per user, enabling unprecedented data rates in mobile communication [2]. However, the mm-wave communication suffers from significantly higher path loss than its sub-6GHz counterpart [3].

This necessitates the use of antenna arrays, see Fig. 1, in which tens to hundreds of antenna elements are used to focus the transmitted or received power in a certain direction, in a process called beamforming, thus greatly improving the achievable communication distance [4]. The direction of the main beam, or lobe, can be controlled by applying an appropriate phase shift to each antenna element signal. In addition to the main lobe, there will be nulls, where the signal is completely canceled, and sidelobes, see Fig. 1.

The phase shift can either be implemented in the digital domain, referred to as digital beamforming, in the analog domain, referred to as analog beamforming, or in both domains, referred to as hybrid beamforming [5]. Digital beamforming results in the highest system capacity, since all degrees of freedom can be utilized in the channel, but it also requires a full RF chain and a data converter for each antenna element, causing high power consumption [1]. On top of this, it requires extremely fast digital signal processing due to the huge amount of data generated, further increasing the power consumption.

Analog beamforming, on the other hand, only requires a single data converter, significantly reducing the power consumption. However, this means that only a single beam can be created at the time, resulting in a poor utilization of the frequency spectrum resources [5].

Hybrid beamforming has proven to be an efficient middle ground for mm-wave communication, almost reaching the system capacity of digital beamforming, while consuming less power [5, 6]. Thus, analog phase shifters are typically required for mm-wave communication. For simplicity of discussion, the rest of this paper will focus on phase shifting

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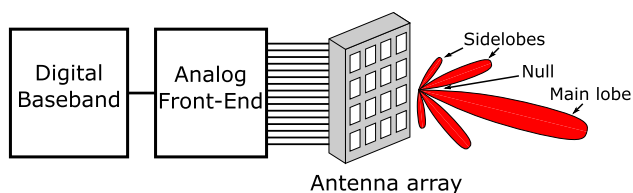
Fig. 1 A beamforming antenna array

in receivers. However, in general, the same concepts apply equally well to transmitters.

The analog phase shift can be applied to the received signal at baseband (BB), at mm-wave frequencies, or to the local oscillator (LO) signal of the mixers [7]. The major benefit of mm-wave phase shifting is that the signals are combined before they are down-converted. This means that only a single mixer is required, making the LO signal routing very simple. However, the phase shifter and combiner must operate at mm-wave frequencies, resulting in high power consumption and/or losses, and any amplitude-variation with phase setting will directly affect the signal. IF/BB phase shifting also suffers from this direct relation between phase-shifter gain and signal amplitude, but is typically easier to implement due to the lower operating frequency. LO phase shifting has, due to the weak relation between mixer gain and LO amplitude, a much lower sensitivity to amplitude-variations of the phase shifter. Both IF/BB and LO phase shifting require one mixer per antenna element, complicating the LO distribution, especially for very large arrays. However, much research has recently focused on combining a large number of smaller integrated circuits (ICs), each with a limited number of antenna elements, in a so-called tiled approach, thereby improving yield and modularity while reducing cost [4]. This means that the penalty of using LO or IF/BB phase shifting in terms of LO distribution becomes less significant compared to mm-wave phase shifting and combining.

An important aspect of an analog phase shifter is phase-amplitude control orthogonality, that is, it should be possible to control the amplitude and phase of each antenna element independently [8]. If the amplitude of each antenna element can be controlled prior to combining the signals, tapering can be used to reduce the amplitude of the sidelobes, at the cost of widening the main beam [9]. However, the sidelobe suppression will be limited by the phase resolution of each phase shifter. In [8], it is shown that for an 8x8 antenna array, the sidelobe suppression will degrade by about 5 dB if the phase shifters have a resolution of 22.5°, compared to using phase shifters with infinite resolution. Phase shifters with 5° resolution, on the other hand, only degrade the sidelobe suppression by about 1 dB. Interestingly, in both cases, the beam direction resolution is less than 1° when non-uniform phase settings are used.

Phase-amplitude control orthogonality is also important for the achievable peak-to-null ratio. If the amplitude varies with varying phase setting, or vice versa, the signals will not perfectly cancel in the null direction. The same is true if the actual phase shift deviates from the desired phase setting. In [10], it is shown that to achieve a 30 dB peak-to-null ratio in a four-element array, the rms phase error and amplitude variation must be less than 2° and ±1.5 dB, respectively.

Due to process, voltage, and temperature variations, this kind of performance is typically only achieved with a time-consuming and costly manual calibration. To speed up that process or even completely circumvent it, several designs with with either built-in self-tests (BIST), automatic calibration schemes or very robust design, requiring little to no calibration, have been proposed [10–15]. Wu et al. [10, 11] achieve excellent phase accuracy and amplitude stability with automatic calibration, but the phase resolution is limited to 22.5°. On the other hand, Inac et al. [12] uses a BIST and achieves a phase resolution of 11.25°, but the rms phase error is about 4°. Yin et al. [13] implements phase shifters with a resolution of 5.6° that only requires calibration at one frequency to cover all of its intended frequencies (23.5–29.5 GHz), but the amplitude variation and phase error is still 1.1 dB and 4.8°, respectively. [14] claims a design robust enough to not require any calibration. However, while the design does achieve an uncalibrated phase resolution and amplitude variation of less than 6.1° and ± 0.8 dB, respectively, the phase error is significant. While not explicitly stated, based on the presented plots it appears to be several degrees. Lastly, [15] achieves an extraordinary rms phase error of 0.08° and rms amplitude error of 0.01 dB after automatic calibration, with a phase resolution of 0.05°. However, their calibration is based on connecting each transmitter output to each receiver input through switches, degrading noise performance and potentially causing cross-talk. For some frequencies, their noise figure (NF) is as high as 11 dB with a gain of − 3 dB, meaning that any circuitry added at the baseband will severely degrade the NF. Additionally, it severely complicates the layout.

In this work, a 24–30 GHz LO phase shifter intended for a hybrid beamforming array is presented, see Fig. 2. The phase shift is accomplished using an injection-locked oscillator (ILO) followed by an injection-locked frequency tripler (ILFT), similar to the work in [10, 11]. A phase detector (PD) is added for built-in measurements of the phase shift and to automatically find the frequency control settings to lock the ILO and ILFT. Additionally, a 28-GHz receiver is implemented to verify the performance of the phase shifter. This paper is an extended version of the work presented in [16].
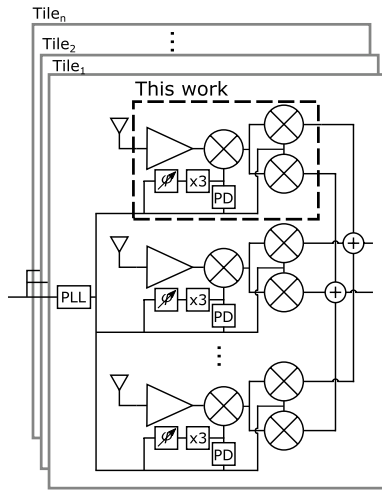
Fig. 2 LO beamforming receiver architecture

2 Injection-locked phase shifter and phase detector

If an oscillator with a free-running oscillation frequency f_0 is injected with a signal at frequency f_{inj}, the oscillator can be forced to oscillate at frequency f_{inj} [17]. The oscillator is then said to be injection-locked. Injection-locking will occur if the difference between f_0 and f_{inj} is smaller than the one-sided locking range f_L, given by [18]:

$$f_L = \frac{f_0}{2Q} \cdot \frac{I_{inj}}{I_{osc}} \cdot \frac{1}{\sqrt{1 - \frac{I_{inj}^2}{I_{osc}^2}}}, \tag{1}$$

where Q is the quality factor of the resonator in the oscillator, and I_{inj} and I_{osc} are the magnitudes of the injected and free-running oscillation currents, respectively.

Since the injection-locked oscillator (ILO) will not oscillate at the resonance frequency of its tank, the ILO output must be phase-shifted relative to the injected signal in order to sustain a 360° phase shift when going through the oscillator loop [18]. This phase shift can be approximated by [18]:

$$\Delta\phi \approx \arcsin\left(\frac{f_0 - f_{inj}}{f_L}\right) \tag{2}$$

Thus, by changing the free-running frequency of the ILO, for instance by using a varactor, this phase shift can electronically be controlled. An issue with this approach is that Eq. 2 is limited to phase shifts of up to ± 90°, while for a phased array, phase shifts of up to ± 180° are required. This can be solved by using a frequency tripler [10, 19], which also triples the phase shift, extending the achievable phase shift to ± 270°. The frequency tripler can also be implemented as an
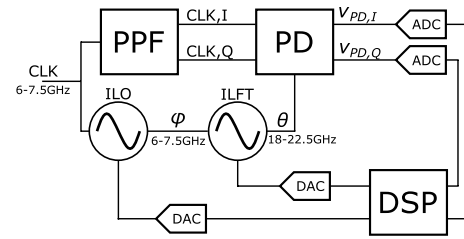

Fig. 3 Architecture of the proposed LO phase shifter

injection-locked oscillator, but with a resonance frequency three times that of the phase-shifting ILO, so that it locks to the third harmonic of the injected signal.

In addition to improving the phase shifting range, using a tripler has two added benefits, both related to that the central PLL seen in Fig. 2 only needs to operate at 1/3 of the final frequency. Firstly, it makes the frequency distribution more power efficient, since lower frequency means less losses [20], thus requiring less buffering. The buffers themselves will also be more power-efficient at lower frequencies. Secondly, the phase noise will improve. This is because the phase noise of ILO will ideally follow the phase noise of the PLL, while the frequency tripler will follow the phase noise of the ILO, multiplied by a factor 3^2, corresponding to an addition of 9.5 dB [10]. Since VCOs, due to poor varactor quality factor, typically have worse figure-of-merit at higher frequencies, a PLL operating at the final frequency would most likely have worse phase noise performance than a PLL operating at one-third of the frequency followed by a frequency tripler.

If a single PLL is used for multiple ILOs and ILFTs, as in Fig 2, the phase noise in each antenna element path will be correlated inside the injection-locked bandwidth of the oscillators. While correlated noise is typically something to be avoided in circuit design, it may actually be an advantage in multi-user beamforming applications [21]. This is because correlated phase noise will affect the phase of each antenna element signal the same, causing the relative phase difference between antenna elements to be unaffected, thus not impacting the shape of the beams and nulls. On the other hand, uncorrelated phase noise will affect the phase of each antenna element signal differently, thus distorting the shape of the beams and nulls.

Figure 3 shows our proposed architecture for the LO phase shifter with frequency tripling and phase detection. It comprises an ILO, an ILFT, a polyphase filter (PPF), a phase detector, two ADCs, two DACs, and a DSP. Note that the converters and DSP are not implemented in this work. A 6–7.5-GHz external clock is injected into the ILO, which, assuming that injection-locking occurs (more on that later), adds a phase shift ϕ. This signal is then injected into the ILFT, which outputs an 18–22.5-GHz signal with a phase
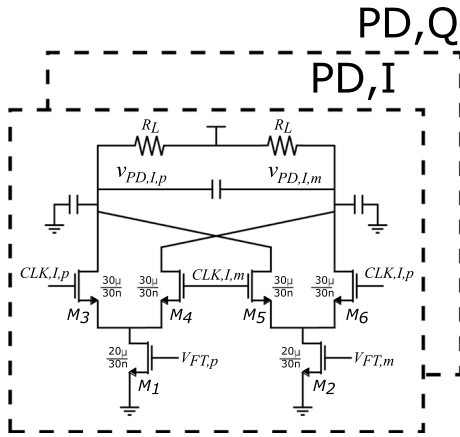
Fig. 4 Schematic of the *I*-part of the phase detector

shift of $\theta = 3\phi + \epsilon$, where ϵ is the phase shift added by the ILFT, relative to the initial clock. The external clock is also injected into a PPF, generating quadrature signals, *CLK, I* and *CLK, Q*. These quadrature clock signals and the ILFT output are then fed to the phase detector.

The phase detector is implemented as two Gilbert mixers, one for the *I*-signal and one for the *Q*-signal, see Fig. 4. The output from the ILFT is fed to the common source transistors M_1 and M_2, while the output from the PPF is fed to the commutating pairs, M_3–M_6. The commutating pairs are sized so that the current is completely steered from one branch to the other, creating a large third harmonic. This third harmonic mixes with ω_{ILFT} and, assuming that the current in each commutating pair is a perfect square wave and only accounting for the third harmonic, results in an output:

$$
\begin{aligned}
v_{PD,I} &= g_{m1}R_L V_{FT} \cos(3\omega_{clk}t + \theta)\frac{4}{3\pi}\cos(3\omega_{clk}) \\
&= \frac{2}{3\pi}g_{m1}R_L V_{FT}(\cos(\theta) + \cos(6\omega_{clk} + \theta)),
\end{aligned}
\tag{3}
$$

$$
\begin{aligned}
v_{PD,Q} &= g_{m1}R_L V_{FT} \cos(3\omega_{clk}t + \theta)\frac{4}{3\pi}\sin(3\omega_{clk}) \\
&= \frac{2}{3\pi}g_{m1}R_L V_{FT}(\sin(\theta) - \sin(6\omega_{clk} + \theta)),
\end{aligned}
\tag{4}
$$

where g_{m1} is the transconductance of M_1 and M_2, R_L is the load resistor, and V_{FT} is the output amplitude of the frequency tripler.

After low-pass filtering the two outputs and converting them to digital signals using the ADCs, the phase can, using simple digital processing, be calculated as:

$$
\theta = \begin{cases} \arctan\left(\frac{v_{PD,Q}}{v_{PD,I}}\right), & \text{if } v_{PD,I} \geq 0 \\ \arctan\left(\frac{v_{PD,Q}}{v_{PD,I}}\right) + 180°, & \text{otherwise} \end{cases}
\tag{5}
$$

Based on this phase measurement, the ILO can then be tuned with a DAC to achieve the desired phase shift without any further calibration, see Fig. 3.

However, this only works if the ILO and ILFT are injection-locked, but the phase detector can also be used to automatically tune the oscillators to achieve lock. The following example, in which the oscillators are tuned to lock to an injected signal with frequency ω_{clk}, illustrates this.

1. Initially, the free-running frequencies of the ILO (ω_{ILO}) and the ILFT (ω_{ILFT}) are tuned to their lowest settings, i.e. the varactor voltages $V_{tune,ILO}$ and $V_{tune,ILFT}$ are set to 0 V.[1] This means that $\omega_{clk} > \omega_{ILO}$ and $3\omega_{clk} > \omega_{ILFT}$, see the top part of Fig. 5(a). This means that in the phase detector, $\omega_{clk,I}$ and $\omega_{clk,Q}$ are mixed with ω_{ILFT}. Since ω_{ILFT} is *not* a harmonic of ω_{clk}, no DC output will be generated in the PD and thus $v_{PD,I} - v_{PD,Q} \approx 0$V, see Fig. 5(a).

2. Next, $V_{tune,ILO}$ is increased, shifting ω_{ILO} up in frequency, see Fig. 5(a). With $V_{tune,ILO} = 0.2$V, locking of ILO has yet to occur, and the PD still outputs close to 0 V.[2] But when $V_{tune,ILO}$ reaches about 0.3V, the ILO locks, see Fig. 5(b). This drastically increases the amplitude of the signal at ω_{clk} that is injected into ILFT, which in turn means that a significant portion of this signal leaks through the ILFT to the PD, creating a DC output when mixed with $\omega_{clk,I}$ and $\omega_{clk,Q}$, see the bottom part of Fig. 5(b). Thus, when $v_{PD,I} - v_{PD,Q}$ starts to diverge significantly from 0V, the ILO is locked.

3. Lastly, the ILFT needs to be tuned. For optimum performance, $3\omega_{clk}$ should be exactly equal to ω_{ILFT}, since this gives the highest amplitude. Combining the low-pass filtered results from (3) and (4) with the Pythagorean identity gives:

$$
\sqrt{v_{PD,I}^2 + v_{PD,Q}^2} = \frac{2}{3\pi}g_{m1}R_D V_{FT}
\tag{6}
$$

That is, $\sqrt{v_{PD,I}^2 + v_{PD,Q}^2}$ will be proportional to V_{FT}, which, as noted above, reaches its peak value when $3\omega_{clk} = \omega_{ILFT}$. Thus, $V_{tune,ILFT}$ is swept until $\sqrt{v_{PD,I}^2 + v_{PD,Q}^2}$ is maximized, see Fig. 5(c).

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[1] The final design also incorporates switched capacitors, but for simplicity, only varactors are included in this example.

[2] $v_{PD,I}$–$v_{PD,Q}$ will not be exactly 0 V due to a small portion of the injected signal's fundamental tone leaking through the ILO and the ILFT and mixing with the PPF output.
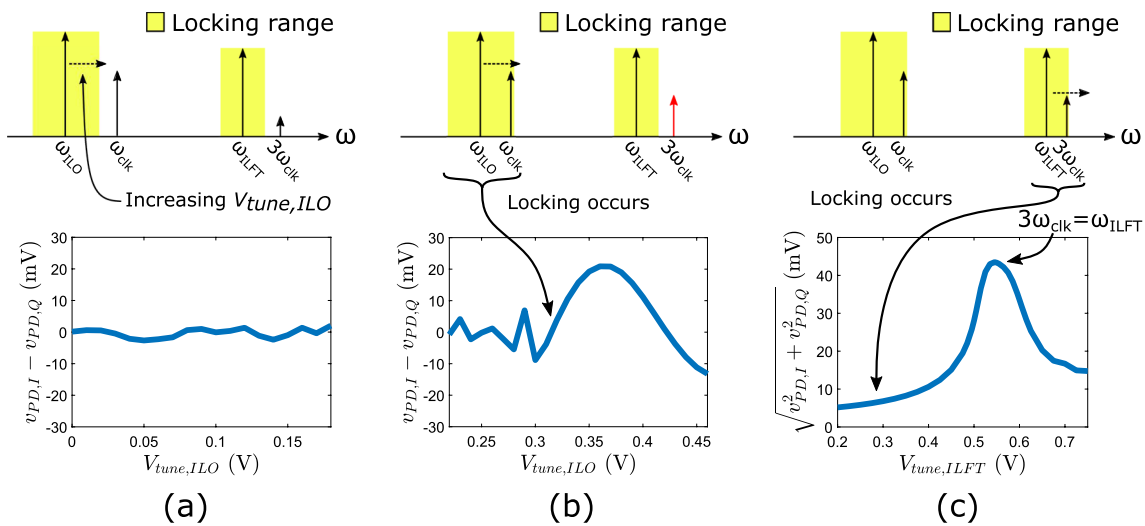
Fig. 5 Scheme for using the PD to detect injection-lock for both the ILO and the ILFT. **a** $V_{tune,ILO}$ starts at 0V and is continuously increased, which increases ω_{ILO}. **b** $V_{tune,ILO}$ reaches a high enough value to achieve lock, causing $v_{PD,I}$ and $v_{PD,Q}$ to diverge. **c** $V_{tune,ILFT}$ is then swept until $\sqrt{v_{PD,I}^2 + v_{PD,Q}^2}$ reaches its peak value

Since the phase can be tuned continuously with a varactor, the phase resolution will only be limited by the resolution of the ILO DAC. The phase detector ADCs will similarly cause a phase error due to the quantization noise. This leads to the question, what are the ADC and DAC resolutions required to make the quantization effects negligible, and what power consumption can be expected for the converters? We start by analyzing the DAC controlling the ILO. Simulations show that the steepest slope for phase vs $V_{tune,ILO}$ is about 1.5°/ mV. Since the phase gets tripled in the ILFT, the resulting slope will be 4.5°/mV. Assuming a full-range voltage of 1V, this corresponds to a minimum DAC resolution of 12 bits to achieve about 1° resolution. Since only a DC voltage is required to control the phase, the sampling rate of the DAC only has to be high enough for the beam to track a moving target, which requires phase update intervals on the order of milliseconds [22]. In [23], a 12-bit DAC with a 112 kS/s sample rate is presented. The DAC consumes 50.8 µW, while occupying an area of only 270 µm^2. Thus, the ILO DAC can be implemented with negligible impact on the total power consumption and area of the LO generation circuit, while achieving a worst-case phase resolution of about 1° and more than sufficient phase update rate.

The ILFT DAC needs a resolution of about 1 mV, or 10 bits, to find the optimal tuning voltage of the tripler. The speed of the ILFT DAC is more relaxed than for the ILO DAC, since this voltage will not change with phase setting, and thus only has to be fast enough to counteract any drift in free-running oscillation frequency. Thus, the power and area consumption will be even smaller than for the ILO DAC.

The ADCs will cause phase errors due to quantization noise, which can easily be investigated using MATLAB or similar software, by simply quantizing the ideal $V_{PD,I}$ and $V_{PD,Q}$ signals for phases varying from 0° to 360°. Then, by comparing $\arctan(V_{PD,Q,quant}/V_{PD,Q,quant})$ to the initial phase, the phase error for various ADC resolutions can be found. Figure 6 shows the rms phase error versus number of bits of the ADC. As seen, for resolutions above 9 bits, the rms error will be less than 0.1°, assuming full-swing input to the ADC. The sampling rate should be on the same order as the DAC. As an example of an ADC that can be used, in [24], a 10 MS/s calibration-free ADC with 11 effective number of bits (ENOB) is presented, consuming 0.41 mW and occupying 0.04mm^2. Reducing the rate to kS/s should provide significant power reductions, making the impact of the ADCs on the total power consumption negligible.

Another source of phase error is mismatch in the PPF and between the *I*- and *Q*-part of the phase detector. To investigate this, a 500-samples Monte Carlo simulation was
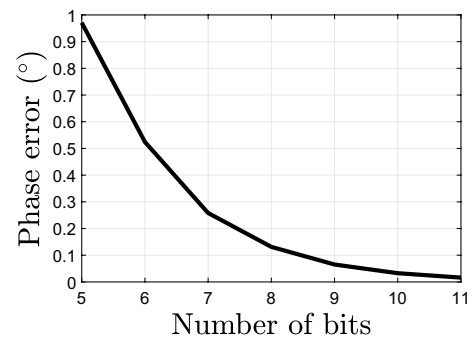

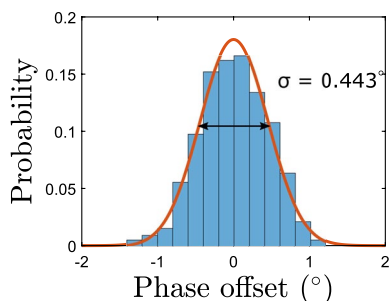**Fig. 6** Rms phase error due to ADC quantization versus number of ADC bits

Fig. 7 Phase detector error due to mismatches

performed. Figure 7 shows the resulting histogram of the phase offset. As seen, the rms phase error is about 0.45°. This error is uncorrelated with the phase error due to the ADCs, and will dominate the total random phase error, which will be about 0.5°. There is, however, also a deterministic phase error due to unwanted mixing that will dominate the total phase error of the circuit, as will be seen in Sect. 4.

3 Circuit implementation

The LO phase shifter is implemented in STMicroelectronics' 28 nm FD-SOI CMOS process and uses a 1 V supply. To properly load the phase shifter and test its capabilities, a 24–30 GHz sliding-IF receiver is also implemented. Figure 8 shows the block schematic of the full circuit.

3.1 LO phase shifter

The implemented LO phase shifter consists of an ILO, a peak detector, an ILFT, a polyphase filter followed by digital logic to generate 25% duty cycle pulses, a PD, and a buffer, as seen in Fig. 8. The ILO is implemented as a regular differential cross-coupled LC oscillator, but with two additional
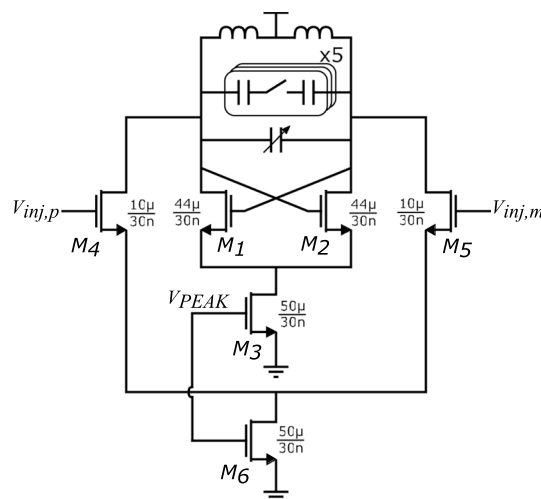

Fig. 9 Schematic of the injection-locked oscillator

injection transistors, see Fig. 9. Using five unary-weighted switched capacitor cells and a varactor, a tuning range between 5.6 and 8.4 GHz is achieved. The varactor is sized so that its tuning capacitance is considerably larger than the capacitance step of one switched capacitor cell. This is done so that a $\pm 60°$ phase shift can be achieved using only the varactor, no matter the frequency. If the gates of the current sources M_3 and M_6 would have been connected to fixed DC voltages, the ILO output amplitude would vary significantly with phase setting, since a large phase shift would correspond to the oscillator operating far from its resonance frequency. This would in turn cause the ILFT amplitude and therefore also the RX gain and noise figure to vary with phase setting. To counteract this, M_3 and M_6 are instead connected to the output of the peak detector, V_{PEAK}, which regulates the ILO amplitude to be almost constant. While it would be enough to only connect M_3 to the peak detector to obtain constant amplitude, the I_{inj}/I_{osc} ratio, and thereby also

Fig. 8 Block diagram of the full circuit. Differential signals drawn as single lines for improved readability
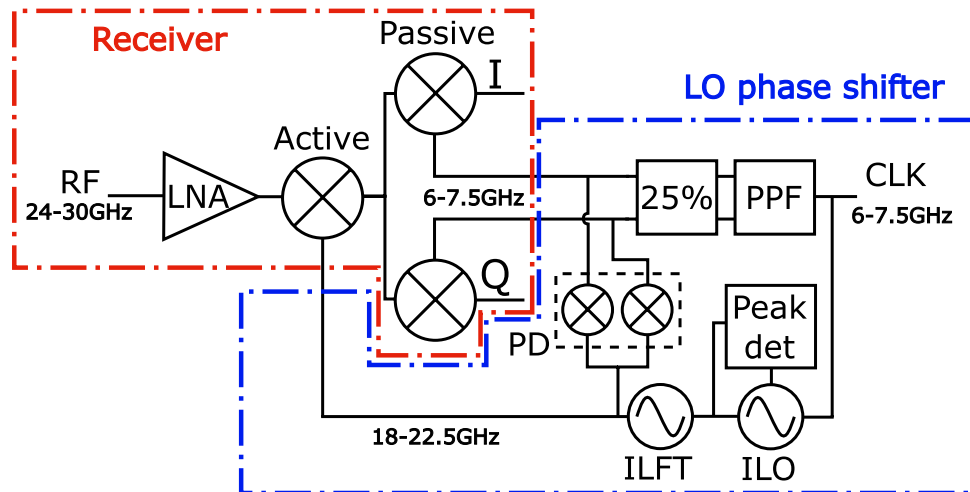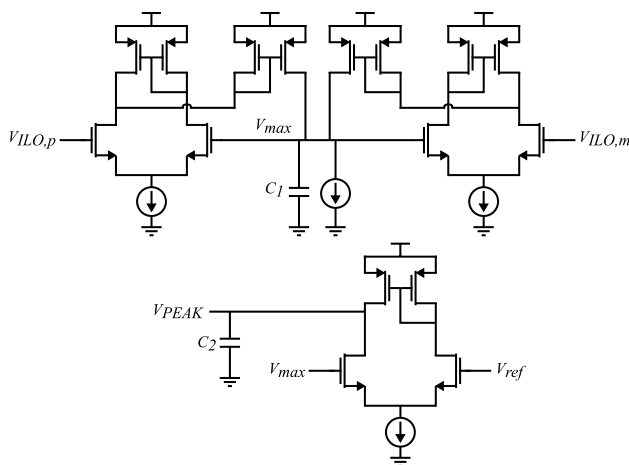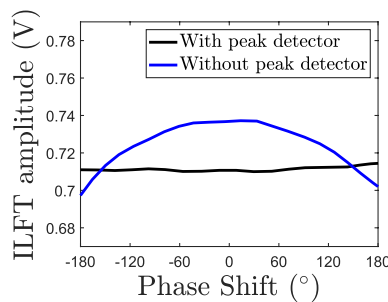
Fig. 10 Schematic of the peak detector

Fig. 11 Impact of peak detector on ILFT amplitude

Fig. 12 Schematic of the PPF and digital logic

reduce frequency pulling of the ILFT when a large interferer is present in the RX. The ILFT and buffer combined consume 6–8 mW, depending on frequency.

The phase detector schematic was shown in Fig. 4. The transistors should be as large as possible to minimize the effect of mismatch and flicker noise, but the size must be limited not to load the ILFT too much and to prevent roll-of before 22.5 GHz, the highest output frequency of the ILFT. The total power consumption of both mixers is 1.2 mW.

Lastly, to generate the quadrature signals, a two-stage PPF is used, see Fig. 12. The resistors used are polysilicon resistors, while the capacitors are metal-oxide-metal capacitors. The PPF is followed by a simple digital circuit to generate pulse waves with 25% duty cycle, which consumes 7 mW.

3.2 Receiver

The full schematic of the receiver is shown in Fig. 13. It comprises an on-chip balun, an LNA, an active mixer and quadrature passive mixers. As can be seen, the LNA is a typical inductively source-degenerated cascode LNA, with the load tuned to 28 GHz. The active mixer is double-balanced, implemented as a Gilbert cell, and is driven by the ILFT, with an LC load tuned to 7 GHz. The image frequency is situated around 14 GHz, far from the desired signal and will be heavily filtered by the antenna, input matching, and LNA output. Thus, no explicit image filter is required. The LNA and Gilbert mixer combined consumes 10 mW.

The two quadrature mixers are implemented with a double-balanced architecture and are driven by the 25% duty-cycle quadrature clock, providing isolation between the the mixer I and Q outputs, providing quadrature baseband signals.

f_L, is kept approximately constant by also connecting M_6 to V_{PEAK}. Otherwise, there would be a risk of losing injection-lock for certain phase settings. The peak detector is based on the design presented in [25] and is shown in Fig. 10. Figure 11 shows the output amplitude of the ILFT versus phase shift at 21 GHz, with and without the peak detector feedback. The variation in amplitude is reduced from 5.7% when not using the peak detector to 0.7% when using the peak detector. The ILO and peak detector consume between 1.2 and 1.7 mW combined, depending on frequency and phase setting.

The ILFT uses the same architecture as the ILO. However, to maximize the third harmonic current, the injection transistors are biased in weak inversion. Additionally, since the ILFT free-running oscillation frequency is not changed once lock is achieved, there is no need for peak detection feedback, so the current-source transistors are biased with fixed DC gate voltages. A tuning range between 17.4 and 23 GHz is achieved with three unary-weighted switched capacitor cells and a varactor. An inverter-based buffer is also implemented between the ILFT and the receiver. This is done to reduce the capacitive load of the ILFT, and to
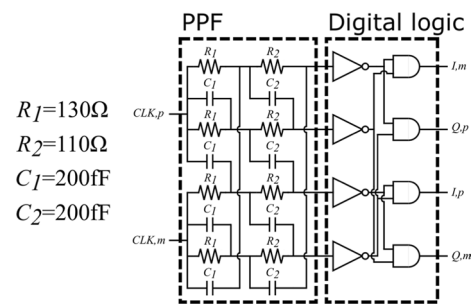
Fig. 13 Schematic of the sliding-IF receiver

Fig. 14 Layout of the full circuit

Fig. 15 Phase noise in the LO generation
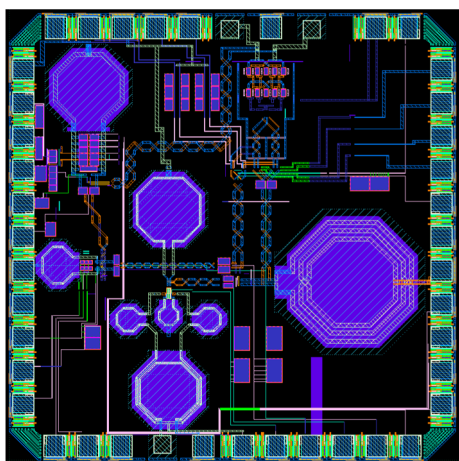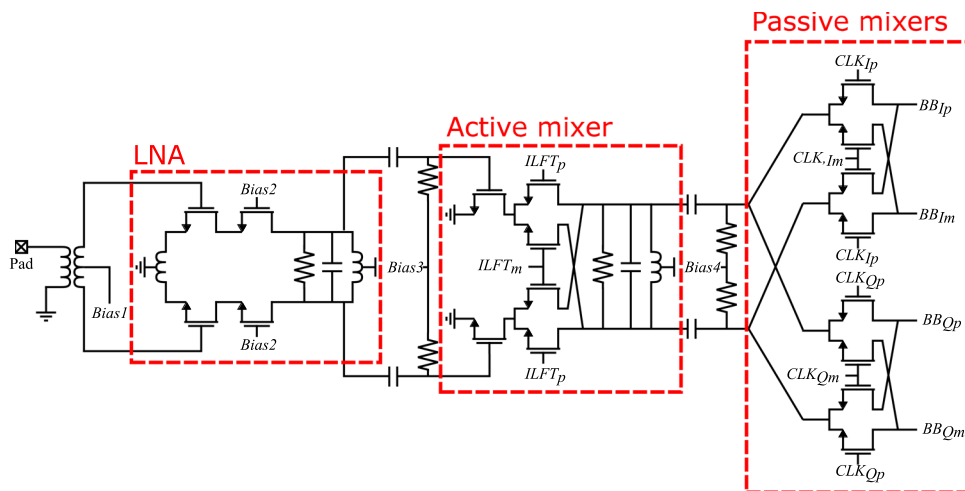
4 Post-layout simulation results

The following simulations were performed after post-layout parasitic extractions using Cadence QRC. Inductors, transformers and longer interconnects were modeled using Keysight Momentum. The full layout is shown in Fig. 14, and measures 1080 µm × 1080 µm, including pads. The entire IC comsumes 27–29 mW, depending on phase setting and frequency.

To simulate the phase noise of the LO chain, a phase noise profile based on the 7GHz integer-N PLL in [26] was added to the external clock signal. Figure 15 plots the phase noise of the external clock, and the outputs of the ILO and ILFT. Also plotted are the phase noise profiles for ILO and ILFT when free-running. As can be seen, the ILO perfectly follows the external clock for low offset frequencies, and the phase noise of the ILFT is about 9.5 dB above
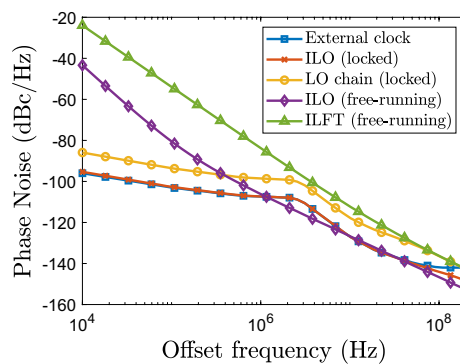
the clock phase noise, matching the theory. However, for large offset frequencies, the ILO and ILFT phase noise profiles start to deviate from the external clock phase noise and instead start to follow the free-running phase noise. This occurs when the frequency offset exceeds the one-sided locking-range. The phase noise at these frequency offsets will then be uncorrelated. However, this should not cause any significant beam distortion due to the low phase noise levels at these offsets. In [18], it is noted that the phase noise performance of an injection-locked oscillator will be worse when operating far from the free-running oscillation frequency due to the change in tank impedance, which is the case when applying a phase shift of $\pm 60°$. However, the simulated phase noise varies by less than 1 dB across all phase settings.

Figure 16(a)–(c) show the phase detector measured phase versus the actual BB output phase, at RF input frequencies 24 GHz, 26.8 GHz and 30 GHz, respectively. Also shown is the phase error, i.e. the difference between the detected and the actual phase. For all three frequencies, the phase shifter achieves more than 360° of phase shift range. The rms phase

Fig. 16 Detected phase shift and phase error versus actual phase shift at **a** 24 GHz, **b** 26.8 GHz and **c** 30 GHz
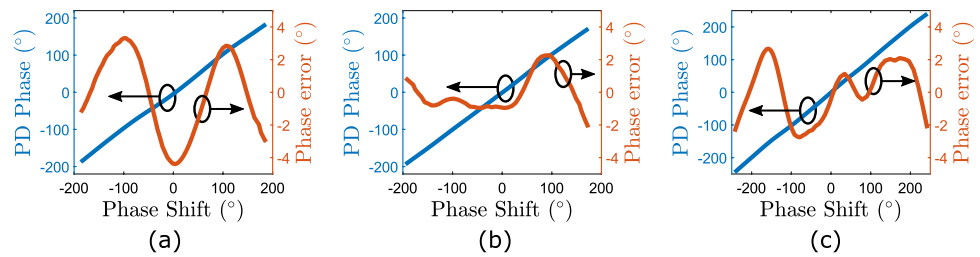
Fig. 17 Receiver gain versus phase shift at **a** 24 GHz, **b** 26.8 GHz and **c** 30 GHz
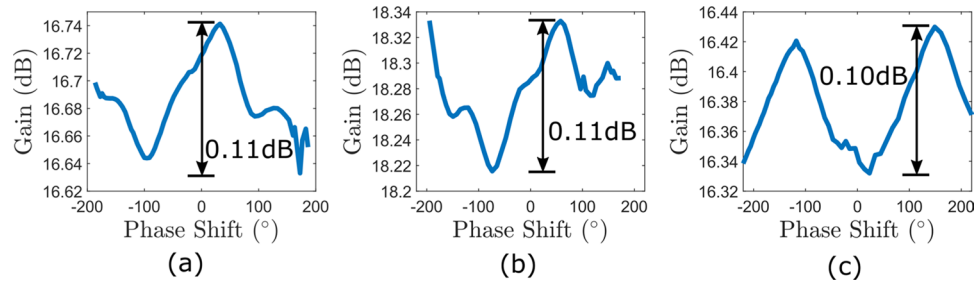
Table 1 Performance comparison of phase-shifting receivers

	This work[a]	[11]	[12]	[15]	[13][b]
Freq (GHz)	24–30	57–66	8.5–11.5	35–42	23.5–29.5
Phase resolution (°)	Cont.[c]	22.5	11.25	0.05	5.6
Rms phase error (°)	2.4	± 0.6[d]	4	0.08	3.6
Gain variation (dB)	0.11	2.2	2	0.08	0.6
Max gain (dB)	16.3–18.3	16.5–21	9–17	− 10 to 2	19
NF (dB)	4.8–6.1	5.8–8.4	3.5	7–11[e]	5.5[e]
Pwr consump./channel (mW)	27–29	60	36	125	156
Technology	28 nm FD-SOI	65 nm CMOS	130 nm CMOS	65 nm CMOS	180 nm BiCMOS

[a] Simulated data only

[b] Only RF part, no down-conversion

[c] Phase tuning is done with varactor and is therefore limited by the voltage control resolution

[d] Rms value not stated, only maximum variation

[e] Including T/R switch

errors are 2.4°, 1.1°, and 1.7°, respectively. This is not random phase error, but rather deterministic due to unwanted mixing in the phase detector. Part of the ILO signal injected into the ILFT will leak through to the PD and mix with the PPF output. Since these signals are at the same frequency, this will generate a DC component, distorting the desired DC component. Figure 17(a)–(c) show the receiver gain versus phase shift for the same simulations. As can be seen in the plots, the receiver gain varies between 16.3 and 18.3 dB versus input frequency, but the maximum gain variation versus phase shift for a given frequency is only 0.11 dB, proving the usefulness of the peak detector feedback. The noise figure at these frequencies are 5.6 dB, 4.8 dB, and 6.1 dB, respectively, with negligible variation with phase setting.

The performance of the circuit is summarized in Table 1, where it is also compared with other receivers with either automatic phase calibration, built-in self test or limited phase calibration. While this work should not be directly compared to the other works presented in Table 1, given that this work is only simulated, the table still gives an indication of the proposed LO phase shifter's ability to drive a mm-wave receiver with competitve performance.

5 Conclusion

An LO phase shifter for 28-GHz 5G transceivers is presented. It features a frequency tripler and a phase detector based on third harmonic mixing to support automatic phase tuning. An algorithm to automatically detect injection-locking using the output of the phase detector is also presented.

The performance of the phase shifter was tested using a 24–30 GHz sliding-IF receiver. The receiver achieves a gain of 16.3–18.3 dB and a noise figure between 4.8 and 6.1 dB, proving the driving capabilities of the LO circuit. Owing to a peak detector-based feedback in the phase shifter, the gain variation of the receiver is only 0.11 dB across all phase settings. The rms difference between the output phase of the receiver and the phase detector, i.e. the phase error, is 2.4°.

Data availability statement The datasets generated during and/or analysed during the current study are available from the corresponding author on reasonable request.

Declaration

References

1. Xiao, M., Mumtaz, S., Huang, Y., Dai, L., Li, Y., Matthaiou, M., Karagiannidis, G. K., Björnson, E., Yang, K., Chih-Lin, I., & Ghosh, A. (2017). Millimeter wave communications for future mobile networks. *IEEE Journal on Selected Areas in Communications, 35*(9), 1909–1935. https://doi.org/10.1109/JSAC.2017.2719924

2. Leveraging the potential of 5G millimeter wave. Technical report, Ericsson (2021). Retrieved May 28, 2022, from https://www.ericsson.com/490025/assets/local/reports-papers/further-insights/doc/leveraging-the-potential-of-5g-millimeter-wave.pdf.

3. Rappaport, T. S., Sun, S., Mayzus, R., Zhao, H., Azar, Y., Wang, K., Wong, G. N., Schulz, J. K., Samimi, M., & Gutierrez, F. (2013). Millimeter wave mobile communications for 5G cellular: It will work! *IEEE Access, 1*, 335–349. https://doi.org/10.1109/ACCESS.2013.2260813

4. Sadhu, B., Gu, X., & Valdes-Garcia, A. (2019). The more (antennas), the merrier: A survey of silicon-based mm-wave phased arrays using multi-IC scaling. *IEEE Microwave Magazine, 20*(12), 32–50. https://doi.org/10.1109/MMM.2019.2941632

5. Molisch, A. F., Ratnam, V. V., Han, S., Li, Z., Nguyen, S. L. H., Li, L., & Haneda, K. (2017). Hybrid beamforming for massive MIMO: A survey. *IEEE Communications Magazine, 55*(9), 134–141. https://doi.org/10.1109/MCOM.2017.1600400

6. Ahmed, I., Khammari, H., Shahid, A., Musa, A., Kim, K. S., De Poorter, E., & Moerman, I. (2018). A survey on hybrid beamforming techniques in 5G: Architecture and system model perspectives. *IEEE Communications Surveys & Tutorials, 20*(4), 3060–3097. https://doi.org/10.1109/COMST.2018.2843719

7. Hashemi, H., Guan, X., Komijani, A., & Hajimiri, A. (2005). A 24-GHz SiGe phased-array receiver-LO phase-shifting approach. *IEEE Transactions on Microwave Theory and Techniques, 53*(2), 614–626. https://doi.org/10.1109/TMTT.2004.841218

8. Sadhu, B., Tousi, Y., Hallin, J., Sahl, S., Reynolds, S. K., Renström, Ö., Sjögren, K., Haapalahti, O., Mazor, N., Bokinge, B., Weibull, G., Bengtsson, H., Carlinger, A., Westesson, E., Thillberg, J.-E., Rexberg, L., Yeck, M., Gu, X., Ferriss, M., … Valdes-Garcia, A. (2017). A 28-GHz 32-element TRX phased-array IC with concurrent dual-polarized operation and orthogonal phase and gain control for 5G communications. *IEEE Journal of Solid-State Circuits, 52*(12), 3373–3391. https://doi.org/10.1109/JSSC.2017.2766211

9. Haupt, R. (1985). Reducing grating lobes due to subarray amplitude tapering. *IEEE Transactions on Antennas and Propagation, 33*(8), 846–850. https://doi.org/10.1109/TAP.1985.1143682

10. Wu, L., Li, A., & Luong, H. C. (2013). A 4-path 42.8-to-49.5 GHz LO generation with automatic phase tuning for 60 GHz phased-array receivers. *IEEE Journal of Solid-State Circuits, 48*(10), 2309–2322. https://doi.org/10.1109/JSSC.2013.2269855

11. Wu, L., Leung, H. F., Li, A., & Luong, H. C. (2017). A 4-element 60-GHz CMOS phased-array receiver with beamforming calibration. *IEEE Transactions on Circuits and Systems I: Regular Papers, 64*(3), 642–652. https://doi.org/10.1109/TCSI.2016.2612232

12. Inac, O., Shin, D., & Rebeiz, G. M. (2012). A phased array RFIC with built-in self-test capabilities. *IEEE Transactions on Microwave Theory and Techniques, 60*(1), 139–148. https://doi.org/10.1109/TMTT.2011.2170704

13. Yin, Y., Ustundag, B., Kibaroglu, K., Sayginer, M., & Rebeiz, G. M. (2021). Wideband 23.5-29.5-GHz phased arrays for multistandard 5G applications and carrier aggregation. *IEEE Transactions on Microwave Theory and Techniques, 69*(1), 235–247. https://doi.org/10.1109/TMTT.2020.3024217

14. Khalaf, K., Vaesen, K., Brebels, S., Mangraviti, G., Libois, M., Soens, C., Van Thillo, W., & Wambacq, P. (2018). A 60-GHz 8-way phased-array front-end with T/R switching and calibration-free beamsteering in 28-nm CMOS. *IEEE Journal of Solid-State Circuits, 53*(7), 2001–2011. https://doi.org/10.1109/JSSC.2018.2822676

15. Wang, Y., Wu, R., Pang, J., You, D., Fadila, A. A., Saengchan, R., Fu, X., Matsumoto, D., Nakamura, T., Kubozoe, R., Kawabuchi, M., Liu, B., Zhang, H., Qiu, J., Liu, H., Oshima, N., Motoi, K., Hori, S., Kunihiro, K., … Okada, K. (2020). A 39-GHz 64-element phased-array transceiver with built-in phase and amplitude calibrations for large-array 5G NR in 65-nm CMOS. *IEEE Journal of Solid-State Circuits, 55*(5), 1249–1269. https://doi.org/10.1109/JSSC.2020.2980509

16. Gannedahl, R., & Sjöland, H. (2021). An LO frequency tripler with phase shifter and detector in 28nm FD-SOI CMOS for 28-GHz transceivers. In *2021 IEEE nordic circuits and systems conference (NorCAS)* (pp. 1–7). https://doi.org/10.1109/NorCAS53631.2021.9599854.

17. Adler, R. (1946). A study of locking phenomena in oscillators. *Proceedings of the IRE, 34*(6), 351–357. https://doi.org/10.1109/JRPROC.1946.229930

18. Razavi, B. (2004). A study of injection locking and pulling in oscillators. *IEEE Journal of Solid-State Circuits, 39*(9), 1415–1424. https://doi.org/10.1109/JSSC.2004.831608

19. Axholt, A., & Sjöland, H. (2010). A 90 nm CMOS 14.5 GHz Injection Locked LO generator with digital phase control. In *2010 IEEE MTT-S international microwave symposium* (pp. 1004–1007). https://doi.org/10.1109/MWSYM.2010.5515588.

20. Vecchi, F., Repossi, M., Eyssa, W., Arcioni, P., & Svelto, F. (2009). Design of low-loss transmission lines in scaled CMOS by accurate electromagnetic simulations. *IEEE Journal of Solid-State Circuits, 44*(9), 2605–2615. https://doi.org/10.1109/JSSC.2009.2023277

21. LaCaille, G., Puglielli, A., Alon, E., Nikolic, B., & Niknejad, A. (2019). Optimizing the LO distribution architecture of mm-wave massive MIMO receivers. arXiv:1911.01339.

22. Cudak, M., Kovarik, T., Thomas, T. A., Ghosh, A., Kishiyama, Y., & Nakamura, T. (2014). Experimental mm wave 5G cellular system. In *2014 IEEE globecom workshops (GC Wkshps)* (pp. 377–381). https://doi.org/10.1109/GLOCOMW.2014.7063460.

23. Aiello, O., Crovetti, P., & Alioto, M. (2019). Standard cell-based ultra-compact DACs in 40-nm CMOS. *IEEE Access, 7*, 126479–126488. https://doi.org/10.1109/ACCESS.2019.2938737

24. Hsu, C.-W., Chang, S.-J., Huang, C.-P., Chang, L.-J., Shyu, Y.-T., Hou, C.-H., Tseng, H.-A., Kung, C.-Y., & Hu, H.-J. (2018). A 12-b 40-MS/s calibration-free SAR ADC. *IEEE Transactions on Circuits and Systems I: Regular Papers, 65*(3), 881–890. https://doi.org/10.1109/TCSI.2017.2771364

25. Sanielevici, S. A., Cioffi, K. R., Ahrari, B., Stephenson, P. S., Skoglund, D. L., & Zargari, M. (1998). A 900-MHz transceiver chipset for two-way paging applications. *IEEE Journal of Solid-State Circuits, 33*(12), 2160–2168. https://doi.org/10.1109/4.735700

26. Lee, C. -H., Kabalican, L., Ge, Y., Kwantono, H., Unruh, G., Chambers, M., & Fujimori, I. (2014). A 2.7GHz to 7GHz fractional-N LCPLL utilizing multimetal layer SoC technology in 28nm CMOS. In *2014 symposium on VLSI circuits digest of technical papers* (pp. 1–2). https://doi.org/10.1109/VLSIC.2014.6858390.

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