A configurable fluorescence sensing front-end for ultra-low power and high sensitivity applications

Maryam Rafati¹ · Seyed Ruhallah Qasemi¹ · Atila Alvandpour¹

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Abstract

This paper presents an ultra-low power, high sensitivity configurable CMOS fluorescence sensing front-end for implantable biosensors at single-cell level measurements. The front-end is configurable by a set of switches and consists of three integrated photodiodes (PD), three transimpedance amplifiers (TIA) for detecting a current range between 1 pA up to 10 nA. Also, an ambient light canceling technique is proposed to make the sensor operate under different environmental conditions. The proposed front-end could be configured for ultra-low light detection or ultra-low power consumption. The circuit is designed and fabricated in a 0.35 μm standard CMOS technology, and the measurement results are presented. The minimum integrated input-referred current noise is measured as 1.07 pA with the total average power consumption of 61.8 μW at an excitation frequency of 80 Hz. For ultra-low-power configuration, the front-end has an average power consumption of 119 nW and input integrated current noise of 210 pA at an excitation frequency of 20 kHz.

Keywords Ultra-low-power · High-sensitivity · Fluorescence detection · Transimpedance amplifier · Ambient light cancelation

1 Introduction

Fluorescence biosensors have gained lots of attention nowadays for their application in biomedical imaging and bio-signals sensing. Fluorescence biosensors include a photosensor and an excitation light source combined with a genetically encoded calcium indicator (GECI), such as GCaMP6, to elicit and collect cellular activities from selected tissue in live animals [1]. A silicon-based integrated optical system on chip (SoC) is a satisfactory solution for having an implantable micrometer-scale fluorescence sensor since CMOS technology has allowed the integration of optical detection devices, e.g., PDs, with analog and digital circuitry. In this regard, a fully implantable wireless micrometer-scale biosensor device is

the next milestone for temporal dynamic functional monitoring of calcium levels in cells in freely moving animals. Many efforts have been taken toward miniaturized fluorescence spectroscopy systems, either for in vivo or in vitro applications.

In [2–4], CMOS head-mountable optoelectronic neural interfaces for fluorescence sensing are presented. In these works, all the CMOS sensors, light-emitting devices (LED), and optical fiber are enclosed within structures that can be mounted on a mouse's head. The bio photometry CMOS sensors in [2–4] consist of a differential CMOS photodetector with a differential capacitive TIA merged with an incremental 2nd order continuous-time delta-sigma modulator. The design in [4] provides a high dynamic range with a minimum detectable current of 2.4 pA, although the sensor cannot be fully implantable and wirelessly powered.

The design of an optoelectronic lock-in amplifier for optical sensing and spectroscopy applications is proposed in [5]. The sensor uses a phototransistor array to convert the incident optical signals into electrical currents followed by TIAs. This optoelectronic sensor consumes low power of 12.97 μW ; however, the minimum detectable current is

✉ Maryam Rafati
maryam.rafati@liu.se

Seyed Ruhallah Qasemi
seyed.ruhallah.qasemi@liu.se

Atila Alvandpour
atila.alvandpour@liu.se

¹ EKS/ISY Linköpings Universitet, Linköping, Sweden

500 nA. A fully integrated image sensor [6] is realized by integrating the nanoplasmonic waveguide-based filters with a CMOS image sensor on a flexible substrate. The work reports the minimum detectable current in the range of 50 fA. Still, the downside is the sensor's high power consumption of 66 mW, making the sensor unsuitable for fully implantable fluorescence detection applications.

As an ongoing cross-disciplinary research project, we aim to design a small implantable application-specific integrated circuit (ASIC) aimed for the detection of a few picowatts of fluorescent light intensity in the 530 nm wavelength from the target cells. The block diagram of the aimed implantable fluorescence sensor is depicted in Fig. 1. This paper focuses on the power consumption and sensitivity of the optical analog front-end of the fluorescence sensing system. The received emitted light intensity from the cells is proportional to the excitation light intensity of the LED. To avoid photobleaching and phototoxicity of the target cells [4], the fluorescence excitation on the cells is necessary to be a pulse with controlled pulse width, duty cycle, and pulse amplitude. Therefore, there is a need to have a sufficient dynamic range for sensing a wide range of emitted light intensity with different pulse widths. On the one hand, the lower end of the dynamic range is limited by the front-end optical and electrical sensitivity.

On the other hand, the upper end of the dynamic range is limited by the saturation point when the input light intensity is high (overload current). The targeted system is aimed to be wirelessly powered, and the energy will be stored in a battery temporarily between each measurement; the available wireless power after the on-chip antenna, the battery size, and the battery capacity will limit the power budget of the total system; thus, the power consumption of the front-end must be minimized at all input light intensities. Moreover, it is required that the implanted system works accurately in different background light intensities (ambient light interference).

This paper describes a configurable CMOS fluorescence sensing front-end with low power consumption for a wide range of received light intensities employing a controllable set of switches. The front-end is configurable to achieve two performance modes: high sensitivity mode and low

power consumption mode to find the optimal PD structure, amplification, and pulsing scheme. The proposed optical front-end consists of three different PN junction PDs for light to current conversion. Two transimpedance topologies achieve the electrical current to voltage conversion and amplifications: These include: (i) A Shunt-feedback topology with high resistance bulk-driven active resistor for low current amplification and ability to detect sinking and sourcing input currents, and (ii) the proposed linearity-modified common gate (MCG) topology for amplifying midrange sinking and sourcing input currents at low power consumption. Furthermore, an ambient light canceling (ALC) switching method is proposed to make the implantable sensor insensitive to the experiment environment.

The paper is organized as follows. In Sect. 2, an overview and analysis of the proposed configurable analog front-end is presented, which includes the designed PD structures, the proposed TIA, and the ALC switching technique. In Sect. 3, the post-layout simulation results are discussed, followed by Sect. 4 reporting the measurement results, and finally, conclusions are made in Sect. 5.

2 The proposed configurable analog front-end

The complete CMOS implementation of the proposed configurable analog front-end is depicted in Fig. 2. The system input stage comprises three PDs of different structures and dimensions along with transmission gate selector switches (TGSW). The selector switches are controlled off-chip to provide suitable PD and amplification stages at varying levels of input light intensities. The generated current by PDs is fed through the amplification stage, consisting of three parallel amplifiers and TGSWs. The first TIA topology is a shunt feedback (SF) amplifier with a tunable bulk-driven load. The second and third TIA topologies are the MCG stages. The third stage of the proposed system is the ALC technique consisting of three sample-and-hold (SH), the unity gain buffer, and a differential to the single-ended amplifier stage. Finally, to provide matching for measurement equipment, the output buffer is placed at the last stage.

2.1 The photodiode structures

The designed three PD structures utilized for detection of 530 nm optical wavelength are shown in Fig. 3. All PDs are PN junctions. The PD_1 is an N + /NWELL/PSUB structure with the dimension of $300 \times 300 \mu\text{m}^2$ with an estimated parasitic capacitance of 11 pF and a dark current

Fig. 1 Block diagram of the implantable fluorescence sensor

of 1.5 pA. This PD is designed for a low input light range and is more efficient for blue light (400–500 nm wavelength) because of the lateral electric field between the shallow $n+$ region and P-substrate [7]. The second structure is an NWELL/PSUB with an area of $100 \times 100 \mu\text{m}^2$ is utilized for faster operation due to smaller parasitic capacitance of 1.4 pF and eliminating the high-density $n+$ region to prevent carrier recombination [8]. The third PD structure is a P + /NWELL by the area of $100 \times 100 \mu\text{m}^2$ with a lower BW than PD_1 because of the large parasitic capacitance of 15 pF; although, it is more suitable for short-wavelength blue light and has a very low estimated dark current of 12 fA [9]. Table 1. represents a summary of all PD's characterization. Moreover, PD_3 is connected from V_{DD} to the input node of the TIAs and could be reversed biased at an adjustable voltage by an external V_{DD} , contrary to PD_1 and PD_2 that are connected from the ground node to the input node of TIAs; their reverse bias voltage is determined by the following stage's circuit biasing. The switches SW_{1-3} depicted in Fig. 2 are implemented to select the optimal PD for different pulsing and input optical intensities. Switches $\overline{SW}_{1-3}$ are utilized for shunting idle PDs currents to prevent voltage breakdown of the next stage MOSFETs by the PDs' unwanted photovoltaic operation.

2.2 The transimpedance amplification stage

In this work, two well-known topologies are used as the core of TIA stages. The SF topology provides a transimpedance amplification equal to the feedback resistor, which is independent of the circuit's biasing condition and polarities of input current. This topology provides low input impedance resulting in a high BW [10]. In Fig. 2, the proposed SF topology, M_{SF1_2} along with its buffer stage of M_{SF3_4} and its tunable floating PMOS bulk-driven active feedback resistor, M_{TR1_2} is shown. The floating PMOS bulk-driven resistor is tunable in a range of 150 M Ω up to 1.5 G Ω ; This high transimpedance gain is suitable for very low input current levels as low as few picoamperes. The PMOS transistors of the tunable active resistor work in the weak inversion region. Their bulk and drain connections are shorted; therefore, by increasing the drain voltage, the threshold voltage of the devices can be modified,

increasing the drain current. This dependence of drain current on drain voltage in the subthreshold region results in a high-value output conductance [11]. The equal output conductance of the active resistor can be controlled by the applied gate-source voltage, V_C , on M_{TR1_2} for different input current ranges. This gate-source voltage is provided by the biasing transistors of M_{TR3_4} .

The CG topology cannot be used for low input currents in the range of picoamperes, as the transimpedance gain is inversely proportional to the bias current [8]. The transistors work in a highly weak inversion region for picoampere input currents, and the circuit is highly dependent on process and temperature variations. However, for mid-range input currents in the range of few nano amperes up to microamperes, a CG topology is used with a lower bias current than SF topology to reduce the power consumption. The CG topology core consists of transistors M_{CG1_3} and zero-compensation capacitor of C_C . The input current of this stage is provided by PD_1, PD_2 , or PD_3 by controlling switches of SW_{1-3} . According to their biases, PD_1 and PD_2 draw current from the TIAs whereas PD_3 injects current into the TIA stage. While the input current from PD_3 is steadily rising, the input node voltage increases, which gradually pushes the main transistors M_{CG1} to off region.

Therefore, the PD_3 limits the dynamic range of the CG TIA. For solving this issue, a linearizing auxiliary diode-connected NMOS, M_{CG4} , at the input node is added that automatically enhances the input electrical dynamic range of the CG amplifier. When the input current is rising and feeding through the CG TIA, since the current source of M_{CG3} is constant, the input voltage node increases, which in turn M_{CG4} gradually turns on, and its drain current increases and draws current from the input node in proportion to the increased current in the input. This rise in the drain current is proportional to the rising margin of the input current. It has a role of current compensation that extends the input current range, therefore improving the circuit's linearity. The proposed MCG can linearly amplify current over a wide input range from different PDs with different biasing. For the milliampere input current range, the same structure as the first MCG is used with a larger dimension and biasing current, consisting of transistors M'_{CG1_4} .

Table 1 Estimated photodiodes' characterizations according to the literature

	Structure	Area (μm^2)	Dark current (fA)	Parasitic capacitance (pF)
PD_1	N + /NWELL/PSUB	300×300	1500	11
PD_2	NWELL/PSUB	100×100	N.A	1.4
PD_3	P + /NWELL	100×100	12	15

2.3 Small signal analysis of TIA stages

For the small-signal analysis of the amplifiers, the photodiode is modeled as a current source parallel with its parasitic capacitance. Figure 4 demonstrates the SF stage with bulk-driven PMOS resistive feedback, output buffer, and the PD equivalent circuit. For the first part of the analysis, the floating bulk-driven feedback resistor at the SF stage is considered to be a lumped resistor of R_F . The output voltage of the SF stage is V_m and the output after the buffer stage is V_{out} . The transimpedance transfer function of the SF stage is calculated as follows:

$$R_{T,SF} = \frac{V_m(s)}{I_{PD}(s)} = \frac{(-g_{m1}R_F + 1) + s(c_{gd1}R_F)}{\left(\frac{(g_{ds2} + g_{m1}) + s(c_{gd1}(g_{ds2}R_F + g_{m1}R_F) + c_{gd2} + c_{gs1}(g_{ds2}R_F + 1) + C_{PD}(g_{ds2}R_F + 1))}{+s^2R_F(c_{gd1}c_{gd2} + c_{gs1}c_{gd1} + C_{PD}c_{gd1} + c_{gs1}c_{gd2} + C_{PD}c_{gd2})} \right)} \quad (1)$$

To simplify the transfer function, simplifications are done based on design considerations of $g_{m1} \gg g_{ds1,2}$ and $1/g_{ds1,2} \gg R_F$. The parasitic capacitance of PD is significantly larger than the parasitics of the transistors, $C_{PD} \gg c_{gs,gd}$. Based on these conditions, the simplified transfer function is calculated as (2). The DC transimpedance gain of the SF stage is equal to $-R_F$ and the amplifier transfer function has two poles and one zero. The dominant pole, P_1 , is at the input node and is majorly dominated by the PD parasitic capacitance. The second pole, P_2 , and the zero are distanced enough from P_1 for a flat frequency response within the bandwidth of interest. The common drain buffer after the SF stage has a wideband response calculated as (5), and is estimated equal to unity

Fig. 4 The SF stage with bulk-driven resistive feedback, output buffer, and the PD equivalent circuit

in the band of interest for the SF stage. Based on this, the total transimpedance transfer function of the SF amplifier is calculated as (6), which totally has a DC transfer gain of $-R_F$, and one pole at the input stage after PD, dominated by the PD capacitance.

$$R_{T,SF} = \frac{V_m(s)}{I_{PD}(s)} \approx (-R_F) \frac{\left(1 - s \frac{c_{gd1}}{g_{m1}}\right)}{\left(1 + s \left(c_{gd1}R_F + \frac{C_{PD}}{g_{m1}}\right) + s^2 \left(\frac{R_F C_{PD}(c_{gd1} + c_{gd2})}{g_{m1}}\right)\right)} \quad (2)$$

$$P_1 \approx \frac{1}{c_{gd1}R_F + \frac{C_{PD}}{g_{m1}}} \approx \frac{g_{m1}}{C_{PD}} \quad (3)$$

$$P_2 \approx \frac{1}{R_F(c_{gd1} + c_{gd2})} \quad (4)$$

$$\frac{V_{out}(s)}{V_m(s)} \approx \frac{\left(1 + s \frac{c_{gs3}}{g_{m3}}\right)}{\left(1 + s \left(\frac{c_{gd4} + c_{gd3} + c_{gs3}}{g_{m3}}\right)\right)} \quad (5)$$

$$R_{T,SF,tot} = \frac{V_{out}(s)}{I_{PD}(s)} = \frac{V_m(s)}{I_{PD}(s)} \times \frac{V_{out}(s)}{V_m(s)} = (-R_F) \frac{\left(1 - s \frac{c_{gd1}}{g_{m1}}\right)}{\left(1 + s \left(c_{gd1}R_F + \frac{C_{PD}}{g_{m1}}\right) + s^2 \left(\frac{R_F C_{PD}(c_{gd1} + c_{gd2})}{g_{m1}}\right)\right)} \times \frac{\left(1 + s \frac{c_{gs3}}{g_{m3}}\right)}{\left(1 + s \left(\frac{c_{gd4} + c_{gd3} + c_{gs3}}{g_{m3}}\right)\right)} \approx \frac{(-R_F)}{\left(1 + s \left(\frac{C_{PD}}{g_{m1}}\right)\right)} \quad (6)$$

The value of the bulk-driven resistor, R_F , can be calculated as (7), defining $\Delta V = V_m - V_{in}$, two cases of (8) or (9) for the R_F happens. In either case the $G_{DS,MTR}$ is calculated as (10) [11].

$$R_F = \frac{1}{(G_{DS,MTR1} + G_{DS,MTR2})} \quad (7)$$

$$\text{If } \Delta V \geq 0 \text{ or } (I_{pd} \geq 0) R_F \approx \frac{1}{G_{DS2}} \quad (8)$$

$$\text{If } \Delta V \leq 0 \text{ or } (I_{pd} \leq 0) R_F \approx \frac{1}{G_{DS1}} \quad (9)$$

$$G_{DSi} = \frac{I_0}{U_T} \exp(V_{SGi}/nU_T) \text{ for } i = 1 \text{ or } 2 \quad (10)$$

Where $U_T = kT/q$ is the thermal voltage, n is subthreshold

transistors, $C_{PD} \gg c_{gs,gd}$. Based on these conditions, the simplified transfer function is calculated as (13), where the compensation capacitor C_C , shifts the second pole, P_2 , further away from the first pole, P_1 , and introduces a left half plan zero, Z_1 , in the transfer function. By choosing the design parameter, so as, Z_1 and P_2 to be close enough to each other, a more flat transimpedance gain and better phase margin response are achieved. Although the MCG stage is an open-loop stage, a better phase margin helps to prevent destabilizing parasitic feedback loops from happening after layout and PCB parasitics are added.

$$R_{T,MCG} = \frac{V_{out}(s)}{I_{PD}(s)} \approx \frac{(g_{m1} + sC_C)}{\left(\frac{g_{m1}g_{m2} + s(C_{PD}(g_{ds1} + g_{ds2} + g_{m2}) + g_{m2}(c_{totM4} + c_{gd3} + c_{gs1} + C_C) + g_{m1}(c_{gd1} + c_{gs2}))}{g_{m1}g_{m2} + s^2(C_{PD}(c_{gd1} + c_{gs2} + C_C))} \right)} \quad (12)$$

$$\frac{V_{out}(s)}{I_{PD}(s)} \approx \frac{1}{g_{m2}} \frac{\left(1 + s \frac{C_C}{g_{m1}}\right)}{\left(1 + s \left(\frac{C_{PD}}{g_{m1}}\right) + s^2 \left(\frac{C_{PD}}{g_{m1}g_{m2}} (c_{gd1} + c_{gs2} + C_C)\right)\right)} \quad (13)$$

$$P_1 \approx \frac{g_{m1}}{C_{PD}} \quad (14)$$

$$P_2 \approx \frac{g_{m2}}{(c_{gd1} + c_{gs2} + C_C)} \quad (15)$$

$$Z_1 \approx \frac{g_{m1}}{C_C} \quad (16)$$

slope factor for the PMOS transistors and I_0 is calculated as (11).

$$I_0 = 2n_p\mu_p C_{ox}(W/L_e)U_T^2 \exp(-|V_{T0}|/nU_T) \quad (11)$$

Where μ_p is the carrier mobility, C_{ox} is the gate oxide capacitance per unit area, V_{T0} is the threshold voltage of the PMOS device, W is the width of the device, and L_e is the effective device length. The small-signal analysis of the MCG stage is done according to Fig. 5. At the typical operation point, M_{CG4} is in weak inversion region, sinking ignorable current from the CG stage, and has a significantly larger resistance compared to the input node resistances. The transimpedance transfer function of the MCG stage is calculated as (12). The total parasitic capacitances of M_{CG4} are included in the calculations as c_{totM4} which varies by the changes in the operation point. To simplify the transfer function, the design conditions of $g_{m1} \gg g_{ds1,2}$ and $1/g_{ds1,2} \gg R_F$ are considered. The parasitic capacitance of PD is significantly larger than the parasitics of the

To further explain the role of M_{CG4} from gain and linearity perspectives, changes in I_{pd} have to be considered. At the designed operation points, when $I_{pd} < 0$, M_{CG4} is almost off, and the DC transimpedance gain is equal to $1/g_{m2}$. However, when $I_{pd} > 0$ and is rising, I_{MGC4} gradually increases, consequently $g_{m,MGC4}$ increases. In this case, the DC transimpedance is as in (17). Depending on the application requirements, different levels of nonlinearity can be defined and tolerated; as g_{m4} increases and reaches to $g_{m4} = 0.4 \times g_{m1}$, there will be a 3 dB gain reduction according to calculations. In the other case, when g_{m4} increases to be equal to g_{m1} , there will be a 6 dB gain reduction which is yet tolerable in this work's application. Therefore, at 6 dB gain fall, the maximum current that M_{CG4} can sink is equal to the original bias current of M_1 , when $g_{m4} = g_{m1}$.

$$\frac{V_o}{I_{pd}} = \frac{g_{m1}}{g_{m4}g_{m2} + g_{m1}g_{m2}} \quad (17)$$

Fig. 5 The MCG stage and the PD equivalent circuit

2.4 Pulsing scheme and ambient light canceling technique

Pulsing of the proposed front-end has been utilized for two main reasons: Firstly, to avoid photobleaching and phototoxicity of the islet cells, the excitation light cannot be continually emitted even with low light intensity from the LED. Secondly, continuous excitation increases the overall power consumption of the system. Figure 6 shows the chosen pulsing of the LED. The duration when LED is on is T_e and the fluorescence sampling period is T_s . Each of the SH circuits turns on after specified delay times of T_{D1} , T_{D2} , and T_{D3} . As the proposed optical front-end is designed for fluorescent signal detection, the ambient background light is always present during signal detection. Moreover, as the proposed optical front-end is designed to detect fluorescent ultra-low light intensities, the dark currents of the PDs are considerable. Therefore, the background light signal and the dark current signal need to be subtracted from the fluorescence signal. The block diagram of the proposed technique for this aim is shown in Fig. 7, which has three signaling phases.

In the first phase, Φ_1 , the LED is on, and the input signal of the system contains the fluorescence signal, ambient light, and dark current. In this phase SH_1 , samples the signal after a delay time of T_{D1} before the LED is turned off and holds it for an entire period. Then in the second phase, Φ_2 , the second sample and hold, SH_2 , samples the ambient light and dark current after a delay time of T_{D2} (right after the LED is turned off). Because the ambient light and dark current frequency considered to be much lower than the sampling frequency, the value of noise and dark current which are stored in the capacitors C_1 and C_2 , are almost the same. Therefore, the sampled ambient light and dark current in Φ_1 and Φ_2 act as a common-mode signal for the next stage. To avoid the discharge of C_1 and C_2 in the hold time, a unity gain buffer is used. For subtraction of ambient light and dark current from the fluorescence signal, the sampled signal in SH_2 is subtracted

Fig. 6 Pulsing scheme of the ALC technique

from SH_1 by a differential-to-single-ended amplifier. In the last phase, Φ_3 , the subtracted signal, which is the desired fluorescence signal, is fed through SH_3 to store only the desired subtracted signal value.

3 Simulation results

The proposed optical front-end is simulated in $0.35 \mu\text{m}$ AMS CMOS technology by cadence IC design software at the post-layout level including bond pad parasitics and the voltage supply is 3.3 V. The simulated transimpedance gain frequency response, R_T , of each TIA topology is depicted in Figs. 8 and 9, respectively, for worst-case PD parasitic capacitances of 1.5 pF and 15 pF. It can be seen that for the larger PD capacitance, the BW frequency decreases. The input-referred current noise of each TIA is depicted in Figs. 10 and 11, respectively, for PD parasitic capacitances of 1.5 pF and 15 pF. The complete comparison of TIAs simulation results is described in Table 2. The SF topology at $V_C = 150\text{mV}$ achieves the highest transimpedance gain of $184 \text{ dB}\Omega$ with integrated input current noise, $I_{n,rms}$, of 768 fA and PD capacitance of 1.5pF. This topology is suitable for detecting ultra-low input currents, which means ultra-low light intensities in the range of few picowatts. However, this topology has the BW of 4.4 kHz, which entails T_e to be at least $227 \mu\text{Sec}$. The SF topology at $V_C = 250\text{mV}$ has a BW of 28 kHz, which is suitable for shorter T_e and lower power consumption, but for input currents in the range of tens of pico amperes. The saturation of the SF amplifier limits the maximum input current

Fig. 7 The ALC technique block diagram

Fig. 8 Simulated transimpedance gain frequency response at $C_{PD} = 1.5$ pF

(overload current) of this topology; therefore, MCG topologies are suitable for input currents in the range of nano amperes to milliamperes.

Considering TIAs to be constantly on, the continuous power of TIAs is shown in the Table 2. The average power consumption of the front-end depends on the chosen LED light pulsing, amplification stage, and sampling scheme. For calculating the average power over $T_s = 100$ ms, each TIA is considered to be on at least for $3 T_e$ until SH_1 and SH_2 have stored the signals; after this duration, the TIA stage could be turned off. As in the proposed system, the

Fig. 9 Simulated transimpedance gain frequency response at $C_{PD} = 15$ pF

duty cycle of the LED pulse is limited by the BW of the TIA; there is an optimum T_e in the LED excitation pulsing for the lowest power consumption. The chosen T_e for each configuration is also listed in Table 2. As mentioned before, at the next step of this research, an integrated unit will automatically choose the best configuration of LED pulsing, PDs, and TIAs regarding power consumption for different input levels.

Figure 12 demonstrates the DC transimpedance gain of the proposed TIAs for the input DC current sweep from 1

Fig. 10 Simulated input-referred current noise frequency response at $C_{PD} = 1.5$ pF

Fig. 11 Simulated input-referred current noise frequency response at $C_{PD} = 15$ pF

Fig. 12 Simulated DC transimpedance gain over the DC input current sweep

pA to 10 mA. Defining the electrical dynamic range as the ratio of the overload input current to the integrated input noise, Fig. 12 shows that the designed system by the controlling of TGSWs can amplify the input currents from 1 pA to 10 mA at the MCG topologies at the positive input currents (when PD_3 injects current into the MCG) extend the linearity. The significant drop in the CG transimpedance gain without auxiliary NMOSs (abbreviated as W.O.A. in Fig. 12) indicates the main transistor in the CG is going to the off region.

Figures 13 and 14 demonstrate the ambient light and dark current cancellation mechanism in the time domain. For making results more visible, an input test current consisting of a sinewave-ambient-noise in the frequency of 100 Hz along with two levels of bio-fluorescence signal with $T_e = 50\mu s$ and $T_s = 3ms$ is fed through the modified CG_1 ; both sinewave and fluorescence pulses have amplitudes equal to 100 nA as are shown in Fig. 13. Figures 14

Table 2 Detailed characteristics of the TIAs simulation results

	SF at $V_c = 150$ mV	SF at $V_c = 250$ mV	MCG ₁	MCG ₂
R_T (dBΩ)	184	163	96	40
BW(Hz) at $C_{pd} = 1.5$ pf	4.4 K	28 K	288 K	143 M
BW(Hz) at $C_{pd} = 15$ pf	1.4 K	14.7 K	50 k	64 M
$I_{n,rms}$ (A) at $C_{pd} = 1.5$ pF	768 f	10.2 p	490 p	420 n
$I_{n,rms}$ (A) at $C_{pd} = 15$ pF	546 f	9.8 p	210 p	250 n
T_e at $C_{pd} = 1.5$ pf(s)	250 μ	50 μ	50 μ	50 μ
T_e at $C_{pd} = 15$ pf (s)	750 μ	75 μ	50 μ	50 μ
$P_{Continuous}$ (W)	45 μ	45 μ	16 μ	13.2 m
$P_{average}$ (W) at $C_{pd}=1.5$ pf	337 n	67 n	24 n	20 μ
$P_{average}$ (W) at $C_{pd} = 15$ pf	1 μ	100 n	24 n	20 μ

Fig. 13 Simulated input current test signal including ambient light and fluorescence pulses

Fig. 14 Simulated transient response of SH_1 and SH_2 function

and 15 show how SH_1 and SH_2 sample the amplified input signal at the output of the TIA.

It can be seen that the SH_1 holds the sum of noise and signal while SH_2 holds only the noise, which at last after being subtracted by a differential-to-single-ended amplifier, with a DC gain of 3, the output voltage which is shown in Fig. 16 is obtained. Considering the signal to ambient noise (SNR) ratio at the input as 1, the output SNR is 20 at this test when $T_e = 50\mu s$, $T_s = 3ms$ and using MCG_1 . This value is highly dependent on the frequency of ambient light and pulsing of sample and holds and LED excitation duration. Generally, by increasing the frequency of ambient light, the output SNR will decrease. The continuous power consumption of the ALC stage is 120 μW . For each configuration of the front-end, this stage is considered to be on for $2T_e$, in the $T_s = 100ms$ periods, therefore its average power consumption is calculated as $(2T_e/T_s) \times P_{continuous}$.

Fig. 15 Simulated transient response of SH_1 and SH_2 function

Fig. 16 Simulated transient response of the output voltage

4 Experimental results

The designed front-end is fabricated, and the chip micrograph is shown in Fig. 17; the analog front-end with additional test blocks, decoupling capacitors, and pad rings occupy $2.88mm^2$ and the circuit blocks of this design occupies only $0.25mm^2$ of the total test chip. The measurement setup is shown in Fig. 18, consisting of a printed circuit board with an external PD (SFH 2270R) and an external TIA (LMP7721) to evaluate the device under test. The optical light source is provided with two 530 nm Green LED, LXML-PM01-0090. The Keysight MSO9404A oscilloscope, Keysight B2962A current power supply, HMF2550 arbitrary signal generator, and an Arduino Duo board are utilized for the measurements.

Fig. 17 Micrograph of the fabricated chip

Fig. 18 Measurement setup of the proposed optical front-end

Regarding the measurement of the generated photocurrent by PDs, by use of external components, necessary calibrations are done for measurements. The responsivity defined as $R = (\text{photo current (A)}) / (\text{incident optical power (W)})$, is measured for the PD_1 , PD_2 , and PD_3 at 530 nm optical wavelength and are obtained as 0.23 A/W, 0.3 A/W, and 0.08 A/W, respectively. The results show that for the green light (530 nm), NWELL/PSUB structure is a suitable choice because of its highest responsivity. To

Fig. 19 Measured DC transimpedance gain over the DC input current sweep

verify the dynamic range of the TIAs, the measurement of DC transimpedance gains is done at a wide input current swept from 10 pA to 100 μ A generated by the internal PD_1 (sinking input current) and PD_3 (sourcing input current) for two cases of current polarities. The results are shown in Fig. 19. The control voltage of the SF amplifier is tuned at 110 mV and 210 mV to have comparable results to the simulated results at 150 and 250 mV.

The measurement for two cases of ultra-low current detection and low power consumption has been done. For this test the PD_1 is used, as it has the highest photocurrent due to the largest size; however, it also has the most significant parasitic capacitance and limits the bandwidth. For using the designed front-end for the detection of the ultra-low current of 1 pA, the highest achievable gain is obtained at $V_c = 50$ mV with SF topology gain equal to $R_T = 183.5$ dB Ω and BW = 80 Hz. This low bandwidth costs higher average power consumption with $T_e = 22$ mS and $T_s = 100$ mS. However, with the pulsing scheme of $T_e = 50$ μ S and $T_s = 100$ mS at $V_c = 300$ mV with SF topology, the minimum detectable current is 1 nA for transimpedance gain of 148 dB Ω . The SF topology at $V_c = 300$ mV achieves a bandwidth of 29 kHz.

Regarding noise performance, the measurements are done in the absence of an input optical signal for the SF amplifier. Figure 20 depicts a measured histogram of output noise voltage for SF amplifier at $V_c = 50$ mV, $R_T = 183.5$ dB Ω with PD_1 , which has the highest sensitivity (highest gain). The standard deviation shows 1.618 mV_{rms}, of which 49 μ V_{rms} is the oscilloscope integrated noise, which is considered a negligible deviation. Referring the output noise voltage to the input of SF TIA by a factor of $R_T = 183.5$ dB Ω , the input-referred current noise is obtained as 1.07 pA_{rms}. The difference between the simulation and the measured value of input-referred current noise is due to the power supply noise, oscilloscope noise, and the on-chip output voltage buffer, which is used to

Fig. 20 Measured histogram of the output voltage noise for SF amplifier at $V_c = 50$ mV, $R_T = 183.5$ dB Ω with PD_1

Fig. 21 Measured input current test signal including ambient light and fluorescence pulses

connect the TIAs outputs to the printed circuit board and measurement equipment.

To verify the effectiveness of the ALC technique, a sinewave input optical light representing the noise is generated by the second LED at three frequencies of 10 Hz, 100 Hz, and 1 kHz. The pulsed optical light is generated by the first LED at two-level amplitudes, and for the case of $T_e = 50 \mu\text{s}$, also T_s is chosen as 1mS instead of 100 mS for better visual representation. It is essential to consider that the noise and excitation pulses are not synchronous. In this measurement, the ALC technique is evaluated for two amplifiers of SF and MCG_1 . Figure 21 shows the transient ambient light and two-level fluorescence signal at the output of the SF amplifier for the $T_e = 50 \mu\text{s}$. For

evaluation of the cancellation of ambient light, the ratio of SNR_{OUT}/SNR_{IN} is used, which is the signal to ambient light ratio at the system's output over the signal to ambient light ratio at the input of the ALC circuit. Figure 22 shows two-level output voltages while the ambient light is attenuated. The effectiveness of the ALC technique is highly dependent on the noise frequency and excitation pulsing scheme. Therefore, the measurements are done for excitation duration of 50 μs , for three noise frequencies of 10 Hz, 100 Hz, and 1 kHz. The obtained results are shown in Table 3.

According to the obtained results, the ambient light-canceling technique works effectively. As expected, it is observable that the noise cancellation efficiency decreases

Fig. 22 Measured transient response of the output voltage **Table 3** The ALC stage performance

Ambient light frequency	SNR _{OUT} /SNR _{IN}	
	SF TIA, T _e = 50 μS	MCG ₁ TIA, T _e = 50 μS
10 Hz	16.5	18.2
100 Hz	4.6	7.7
1 kHz	1.3	2.1

by increasing the frequency of the ambient light in comparison to the fluorescence signal frequency. The ALC technique gets more effective when the ambient light frequency decreases.

The continuous power consumption of the SF amplifier, MCG₁, and MCG₂ are measured as 40 μW, 14 μW, and 12 mW, respectively. For calculating the average power consumption, according to the obtained results, minimum detectable current of 1 pA, T_e= 22 mS and T_s= 100 mS is the optimum pulsing for the SF amplifier, and the average power consumption is 26.4 μW. Furthermore, the configurability of the system has the advantage that for higher input currents, in the range of a few nano amperes, the power consumption of 21 nW is obtained by MCG₁ at a faster pulsing scheme of T_e = 50 μS and T_s = 100 mS. The continuous power consumption of the ALC circuit is measured as 105 μW, which results in average total power consumption of 105 nW and 46.2 μW for T_e = 50 μS and T_e = 22 mS, respectively.

A comparison of the proposed work with the previous similar works on the miniaturized biomedical optical front-

ends is shown in Table 4. In the literature, the minimum detectable input current is compared to show the merits of the active CMOS design. In addition to minimum detectable current, the ratio of the minimum detected optical power over the photodetector size is included in Table. 4 for a fairer comparison. As can be seen, the proposed work achieves ultra-low integrated input-referred noise at a very low power consumption compared to similar works. Considering the minimum power consumption criterion, the proposed design in the MCG configuration achieves ultra-low-power performance to detect currents as low as 210 pA with a faster pulsing scheme. Additionally, the configuration can be changed to detect currents as low as 1.07 pA at higher power consumption with a slower pulsing scheme. The sensor in [6] has the lowest minimum detectable current among all previous works, although at the cost of high power consumption of 66 mW, and still its ratio of the minimum detected optical power over the photodetector size is lower than the current work. The work in [4] is the closest effort to the goal and design criteria of the current project on similar target cells regarding high

Table 4 Comparison table of the proposed front-end with similar works

	[4]	[6]	[12]	[13]	[14]	This work ^a	This work ^b
Process	0.18 μm	65 nm	0.18 μm	0.18 μm	0.13 μm	0.35 μm	0.35 μm
Year	2018	2017	2019	2017	2019	2021	2021
V_{DD} (V)	1.8	3.3	3.3	3.3	1.2	3.3	3.3
$P_{\text{Average,Total}}$ (W)	41 μ	66 m	93 μ	60 μ	2.16 m	61.8 μ	119 n
$P_{\text{Average,TIA}}$ (W)	N. A	6 m	N. A	N. A	N. A	15.6 μ	14 n
$I_{n,\text{rms}}$ (A)	2.46 p	45 f	1.3 p	200 f	40 n	1.07 p	210 p ^c
R_T (dB Ω)	N. A	N. A	N. A	N. A	98	183.5	96
BW (Hz)	50	N. A	N. A	N. A	43.3 K	80	50 K ^c
Conversion time (ms)	N. A	0.5	0.3	1	N. A	22	0.05
PD size (μm^2)	200×200	91×123	300×300	200×200	2400×2800^c	300×300	300×300
$\frac{\text{Min. Detected Optical Power}^d}{\text{Photodiode Size}}$ (W/ μm^2)	0.24 f	0.07 f	N. A	N. A	23.8 f	0.05 f	10.1 f
Results	Meas	Meas	Meas	Sim	Meas	Meas	Meas

^aThe SF TIA at $V_c = 50$ mV and $C_{PD} = 15$ pF configuration^bThe MGC₁ and $C_{PD} = 15$ pF configuration^cPost-layout simulation^dCalculated from minimum detected current and the responsivity^eExternal photodiode

sensitivity fluorescent measurements. As can be seen, compared to [4], the current work provides a higher responsivity and lower detectable optical power at the relatively same order of power consumption and meets the application's requirements.

5 Conclusion

In this paper, a configurable optical front-end is presented for low-power light detection of bio-fluorescence signals. The switching scheme implemented after the TIA stages provide the ability to cancel out the ambient light interference. The results show that the proposed work achieves input integrated current noise as low as 1.07 pA at an average power consumption of 61.8 μW and operates at an ultra-low average power consumption of 119 nW with integrated input current noise of 210 pA. This front-end is configurable to provide a wide detectable input current of 1 pA up to 10 mA.

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Data availability The datasets generated and analyzed during the current study are available from the corresponding author on reasonable request.

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Maryam Rafati received her M.Sc. degree from Rajae University, Iran in 2017. She is currently pursuing the degree of Ph.D. at the Integrated Circuits and Systems division at Linköping University. Her research interests are analog and mixed-signal circuits for ultra-low power applications such as biomedical implants and wireless sensors.

Seyed Ruhallah Qasemi received his B.Sc. degree from Iran University of Science and Technology in 2015 and his M.Sc. degree from Rajae University, Iran in 2018. Currently, he is a Ph.D. researcher at the Integrated Circuits and Systems division at Linköping University. His research interests include biomedical analog and mixed-signal integrated circuits for optical and wireless front-ends.

Atila Alvandpour is the head of Electronic Circuit and System division at Linköping University. He received the M.S. and Ph.D. degrees from Linköping University, Sweden, in 1995 and 1999, respectively. From 1999 to 2003, he was a senior researcher at the Circuit Research Lab, Intel Corporation. In 2003 he joined Linköping University as a Professor of VLSI design, and he is the head of Integrated Circuits and Systems Division in the Department of Electrical Engineering. His research interests include various issues in design of integrated circuits and systems in advanced nano-scale technologies, with special focus on data converters, sensor readout and data acquisition systems, energy-harvesting and power management systems, low-power wireless sensors, high-performance digital/analog baseband, and RF frontends for multi-Gigabit/s radio transceivers. He has published more than 100 papers in international journals and conferences and holds 24 U.S. patents. Prof. Alvandpour has served as a member of the technical program committees for many IEEE and other international conferences, including the IEEE Solid-State Circuits Conference (ISSCC) and the European Solid-State Circuits Conference (ESSCIRC). He has also served as a guest editor for the IEEE Journal of Solid-State Circuits.