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NANO-studio, the design environment of filter banks implemented in standard CMOS technology

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Abstract
The paper presents a method of optimizing frequency characteristics of filter banks in terms of their implementation in digital CMOS technologies in nanoscale. Usability of such filters is demonstrated by frequency-interleaved (FI) analog-to-digital converters (ADC). An analysis filter present in these converters was designed in switched-current technique. However, due to huge technological pitch of standard digital CMOS process in nanoscale, its characteristics substantially deviate from the required ones. NANO-studio environment presented in the paper allows adjustment, with transistor channel sizes as optimization parameters. The same environment is used at designing a digital synthesis filter, whereas optimization parameters are input and output conductances, gyration transconductances and capacitances of a prototype circuit. Transition between analog s and digital z domains is done by means of bilinear transformation. Assuming a lossless gyrator-capacitor (gC) multiport network as a prototype circuit, both for analysis and synthesis filter banks in FI ADC, is an implementation of the strategy to design filters with low sensitivity to parameter changes. An additional advantage is designing the synthesis filter as stable infinite impulse response (IIR) instead of commonly used finite impulse response (FIR) filters. It provides several dozen-fold saving in the number of applied multipliers.. The analysis and synthesis filters in FI ADC are implemented as filter pairs. An additional example of three-filter bank demonstrates versatility of NANO-studio software.

Keywords CMOS analog circuit design · Current mode circuits · Standard digital CMOS technology · Filter banks · Frequency-interleaved ADC · Low power low sensitive circuits

1 Introduction

Filter banks are necessary to use in a wide range of applications, from data transmission to data compression and signal processing, for example to speech, audio, video, and biosignal coding, [16, 20, 21, 23]. The paper presents NANO-studio environment for designing filter banks in terms of their implementation in standard, digital CMOS technologies. Functioning of this environment has been illustrated by its application for frequency-interleaved (FI) analog-to-digital converters (ADC). Presented design strategy uses multiport lossless gyrator-capacitor (gC) circuits as prototype networks, both for analysis and synthesis filters in FI ADC.

Analysis filters are implemented in switched-current (SI) technique, while synthesis filters as digital ones with infinite impulse response (IIR). The first type of filters is analog, whereas the other-digital. However, both filters work in discrete time. It is significant from the perspective of developed software tool, as NANO-studio is based on response optimization for the sequence of time samples, as for instance in [21]. The use of a gC prototype circuit both reduces the number of integrators in an SI circuit and provides a simple digital filter as compared with finite impulse response (FIR) filters. To operate in current mode, which is necessary due to SI technique, the converter presented in the paper [10] can be used. 5-bit sub-ADCs, working in respective FI ADC channels, were implemented in C language.

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In the next section, the general structure of FI ADC has been recalled, together with matrix notation of transfer functions of filter banks present in it. The matrix and equivalent tensor relationships that describe bilinear transformation, needed for transition between prototype gC circuit and its discrete time counterpart network, have also been presented. Sect. 3 presents NANO-studio environment, whereas the two following sections describe design of analysis and synthesis filter banks in this environment, respectively. In Sect. 5 we also briefly discuss FI ADC implementation, while in Sect. 6 we demonstrate versatility of adopted design strategy and developed NANO-studio environment, using the example of a three-filter bank.

2 General structure of FI ADC

General structure of frequency-interleaved (FI) analog-to-digital converters (ADC) is presented in Fig. 1. The essential difference versus the ones so far presented in the literature, [14, 15, 26], lies in replacement of analysis and synthesis filters, present separately in each converter path, with multiport networks. Both multiport networks are designed based on multiport gC circuits, [17], described by transfer functions in the analog domain, respectively as

$$H_0^a(s),\ H_1^a(s),\ \ldots,\ H_{M-1}^a(s), \tag{1}$$

and

$$G_0^a(s),\ G_1^a(s),\ \ldots,\ G_{M-1}^a(s). \tag{2}$$

We will also use these transfer functions in the discrete z domain using bilinear transformation

$$\frac{sT}{2} = \frac{z-1}{z+1} = \frac{1-z^{-1}}{1+z^{-1}}, \tag{3}$$

then leaving out upper index a in their marking.

Transfer functions (1) and (2) may be written matrix-wise as

$$H^a(s) = \frac{P'S}{Q'S}. \tag{4}$$

where P and Q in (4) are vectors (matrices) of k-degree polynomial's coefficients of the variable s, whereas S is a vector including this variable in ascending powers:

$$S' = \begin{bmatrix} s^0 & s^1 & \ldots & s^k \end{bmatrix}, \tag{5}$$

where $'$ symbol represents transposition of a vector (matrix).

Using bilinear transformation (3) we receive a transfer function in the z domain, also in matrix-wise notation, as:

$$H(z) = \frac{A'Z}{B'Z}, \tag{6}$$

where A and B are vectors (matrices) of k-degree polynomial's coefficients of the variable z^{-1}, whereas Z is a vector including this variable in ascending powers:

$$Z' = \begin{bmatrix} z^0 & z^{-1} & \ldots & z^{-k} \end{bmatrix}. \tag{7}$$

Matrices P and Q as well as A and B are of $(k+1)*1$ order. Notations of vectors S and Z indicate that these polynomials are ordered according to ascending powers of variables s and z^{-1}, respectively. Row numbers, in the range $0, \cdots, k$ correspond to the powers of variables s and z^{-1}, that is:

$$\begin{aligned} P'S &= \sum_{i=0}^{k} p_i s^i = p_i s^i, \quad Q'S = \sum_{i=0}^{k} q_i s^i = q_i s^i, \\ A'Z &= \sum_{i=0}^{k} a_i z^{-i} = a_i z^{-i}, \quad B'Z = \sum_{i=0}^{k} b_i z^{-i} = b_i z^{-i}. \end{aligned} \tag{8}$$

Each polynomial in (8) is written in two ways: with or without the sum symbol, as per tensor notation, where an

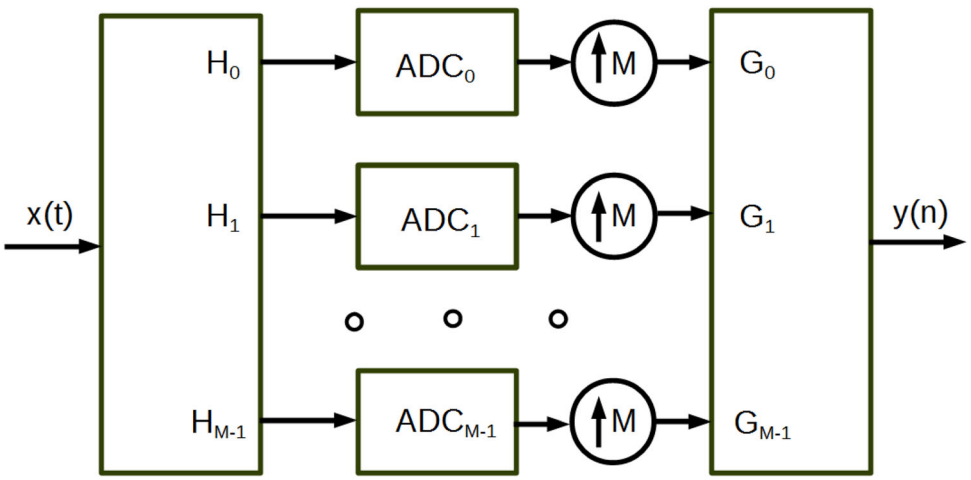

Fig. 1 Structure of an M-channel ADC composed of multiport analysis and synthesis filters

index that appears twice as lower or upper automatically means summing up over its whole range. Upper indices are at the same time exponents of powers of variables s and z^{-1}.

Matrices A, B, P, and Q, as proven in [5], are in one-dimensional networks linked by relationships:

$$P = (A'T_k)', \quad Q = (B'T_k)', \quad A = (P'T_k)', \quad B = (Q'T_k)', \tag{9}$$

where T_k is a transformation matrix, with a size $(k+1)*(k+1)$, for bilinear transformation (3).

The matrix T_k can be generated in a recurrent manner:

$$\begin{aligned} T_0 &= [\,1], \\ T_1 &= \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}, \\ T_2 &= \begin{bmatrix} 1 & 2 & 1 \\ 1 & 0 & -1 \\ 1 & -2 & 1 \end{bmatrix}, \\ T_3 &= \begin{bmatrix} 1 & 3 & 3 & 1 \\ 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 \\ 1 & -3 & 3 & -1 \end{bmatrix}, \\ &\ldots, \quad T_k. \end{aligned} \tag{10}$$

The procedure for construction of these matrices is as follows. The i-th rows, $i = 1, \cdots, k$, of the successive matrices T_j, $j = i-1, \cdots, k$, always form two neighbouring rows of a Pascal triangle with $T_0 = [1]$. For example, the first row of T_0, the first row of T_1, the first row of T_2, and the first row of T_3, etc. form a Pascal triangle. Similarly, elements composed of the second row of T_1, the second row of T_2, the second row of T_3, etc., or the third row of T_2 and the third row of T_3, etc. are also calculated like the Pascal triangle elements. The elements of the last row of each matrix are equal to elements of the first row with alternately changed signs.

It is shown in the paper [8] that each transformation matrix can be also directly calculated. The first column elements of the matrix $T_k = [t^i_{k\,j}]$, $i,j = 0, \ldots, k$ are all equal to 1 ($t^i_{k\,0} = 1$, $i = 0, \ldots, k$) and the first row elements are obtainable from the known formula

$$t^0_{k\,j} = \binom{k}{j} = \frac{k!}{j!(k-j)!}, \tag{11}$$

where $j = 0, \ldots, k$. The remaining elements $t^i_{k\,j}$, $i,j = 1, \ldots, k$ of the matrix T_k can be obtained from the formula

$$t^i_{k\,j} = t^{i-1}_{k\,j} - \left(t^{i-1}_{k\,j-1} + t^i_{k\,j-1}\right) \tag{12}$$

where $i,j = 1, \ldots, k$. In the above formulas the upper i and the lower j indices are taken as the row and the column of the matrix T_k, respectively. Such representation is convenient for the tensor notation. For example the first equation in (9) can be written as

$$p_l = a_i t^i_{k\,l}, \quad i,l = 0 \ldots k. \tag{13}$$

In [5] it was also found that

$$T_k T_k = 2^k U, \tag{14}$$

where U is a unit matrix. Hence, the normalisation factor of the matrix T_k is $1/\sqrt{2^k}$. Let us note that the transformation matrix T_k, composed of elements given by (10), (11) and (12), describes the bilinear transformation (3) for the sampling period $T = 2$.

In C^{++} class MDp (Multi-Dimensional polynomials) has been developed for calculation of polynomials of transfer function numerators and denominators at bilinear transformation between two domains, s and z, as per relationships (13). With the use of this class, transfer function transformations both for one-, as well as two- and three-dimensional circuits, are possible [3, 4]. Generalization to multi-dimensional circuits is achieved thanks to tensor notation.

Based on a transfer function in z domain, the circuit response to any input signal may be obtained in discrete time domain, as z_i^{-m} means delay by m periods in i-th dimension. Obtaining frequency response is, as is well-known, possible after the substitution:

$$z_i = exp(j\omega_i T_i), \quad i = 1 \ldots n. \tag{15}$$

T_i symbol means sampling period in i-th dimension.

The following will be called distortion transfer function and aliasing transfer function

$$V_d(z) = \frac{1}{M} H(z) G(z)', \tag{16}$$

and

$$V_a(z) = \frac{1}{M} H(-z) G(z)', \tag{17}$$

respectively, [15], where $H(z)$ and $G(z)$ mean transfer function vectors

$$H(z) = [H_0(z),\ H_1(z),\ \ldots,\ H_{M-1}(z)], \tag{18}$$

and

$$G(z) = [G_0(z),\ G_1(z),\ \ldots,\ G_{M-1}(z)]. \tag{19}$$

We say that converter ideally (perfectly) transforms (reconstructs) the input signal to the output one (perfect reconstruction — PR) if

$$V_d(z) = cz^{-d}, \tag{20}$$

and

$$V_a(z) = 0, \tag{21}$$

i.e. when the output signal $y(n)$ is delayed by d periods and scaled by a constant c in relation to the input signal $x(n)$:

$$y(n) = cx(n-d). \tag{22}$$

However, if

$$|V_d(z)| = c, \tag{23}$$

$$V_a(z) = 0, \tag{24}$$

then we say about perfect module reconstruction (PMR).

In Sect. 4 we will present design method of discrete time analog filter banks, implemented in (SI) technique, that realizes transfer functions (18), with transistor channel dimensions as variables being optimized. The method is going to be illustrated by an example of a filter pair received on the basis of a prototype gC circuit. Fully automated environment for designing such circuits has been presented in the paper [8].

Presented in Sect. 5 implementation of a synthesis filter bank described by transfer functions (19) is also possible based on a prototype gC circuit. In this case the variables being optimized are capacitances and transconductances of the prototype circuit. This approach guarantees stability of designed IIR filters.

To realise all filters presented in Sect. 4, 5 and 6 NANO-studio environment, presented in the following section, is used.

3 NANO-studio environment

Development of CMOS technology, based on constant reduction of MOS transistor channel lengths, is dedicated to digital circuits. These technologies are characterised by relatively high technological pitch as compared with transistor channel sizes. Additionally, low supplying voltages, below 1V, render implementation of many basic analog cells, such as OpAmps, unattainable in these technologies. It is particularly evident in designing precision filters which find their use in many different applications related to signal processing [12, 18, 22]. This paper, based on the example of SI circuits, demonstrates a novel approach to solving such issues. The method described will be illustrated by the example of filter pair working in SI mode [7, 9]. The starting point consists of pre-developed tools to design such circuits [22]. However, the filter characteristics obtained at this design stage are unsatisfactory due to technological pitch. When effectuating optimization of parametrised filter cells, due to the sizes of channels of transistors, which the cells are composed of, fully satisfactory frequency characteristics may be attained.

Proposed optimization method uses Hooke-Jeeves gradient-free algorithm, which, despite being for the first time presented as long ago as in 1961, is still used in many contemporary applications [1, 2, 25]. The algorithm was chosen, because performs better against other optimization algorithms background. It achieves the best results in the shortest time [19]. Presented version of the algorithm is modified for discrete issues and was presented in earlier works related to technological migration [18] and optimization [27].

Optimization procedure is presented on the flow chart in Fig. 2. Right side of the diagram, that is, feedback, can be freely modified. In particular, at the simulation stage, any tool can be used that is adequate for the issue related to the optimization. In case of the analysis filter, designed in MentorGraphics environment in SI technique, ELDO was used. This simulation program is a time-consuming tool, though. Therefore, in case of the synthesis filter, we use gC-studio, which allows symbolic analysis of prototype circuit, offering significant acceleration of optimization process. In the presented implementation, the script working in Linux has been used, which starts respective programs and manages feedback loop. We will also use MATLAB environment with suitable script for processing and analysing results of simulation, as well as for goal function value calculation based on time domain response.

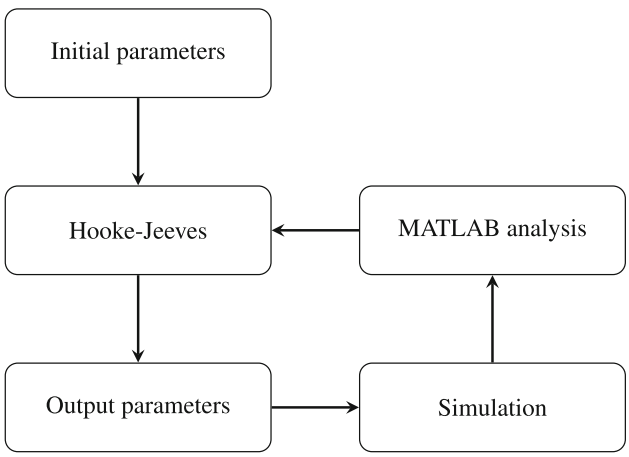

Fig. 2 Data flow-diagram of the optimization method

4 Design of the analysis multiport filter

As part of an experiment that examines the impact of optimization for improvement of time and frequency characteristics, a filter pair working in SI mode, with suitable transfer functions both for low-pass and high-pass outputs, has been used.

Trasfer functions of a prototype filter pair, designed in gC-studio, [17], can be written as:

$$H_0^a(s) = \frac{P_0' S}{Q' S}, \tag{25}$$

and

$$H_1^a(s) = \frac{P_1' S}{Q' S}, \tag{26}$$

where

$$S' = \begin{bmatrix} 1 & s & s^2 & s^3 & s^4 & s^5 \end{bmatrix} \tag{27}$$

is a vector of complex variables s, while polynomial coefficients are:

$$\begin{aligned} Q' &= [1.26088 \;\; 2.09342 \;\; 3.21886 \;\; 3.07201 \;\; 1.82409 \;\; 1], \\ P_0' &= [1.26088 \;\; 0 \;\; 1.59449 \;\; 0 \;\; 0.46813 \;\; 0], \\ P_1' &= [0 \;\; 0.53493 \;\; 0 \;\; 1.51793 \;\; 0 \;\; 1], \end{aligned} \tag{28}$$

respectively.

Filters with these coefficients have been designed by means of gC-studio for cutoff frequency $\omega_p = 1$ and $18dB$ attenuation in the stopband.

Based on the prototype gC circuit, its SI counterpart network has been obtained, using the method presented in [22]. The SI filter composed of integrators and parametrised cells has been implemented in technological process TSMC 65nm. Due to the technological pitch equal to 5nm in this process, impulse responses of the SI filter are deviated from ideal impulse responses of the prototype gC circuit. We will show that they can be effectively adjusted by means of NANO-studio.

The first 36 samples, being an impulse response in time domain of the SI filter pair, were taken for goal-function value calculation. The objective of the optimization process was to select transistor parameters (channel width and length) of parametrised cells, which, in SI circuits, are current mirrors, in such a way as to achieve two goals.

The first one was to adjust magnitude responses of the SI filter pair to the characteristics obtained from transfer functions, based on which optimum impulse responses were specified.

Another important goal was to eliminate the dc offset in the SI filter pair circuit, which has an impact on the symmetry of output signal in time domain. With this goal in mind, impulse response was also used, by comparing the response of prototype filter pair with the response of real circuit received on the basis of simulation.

Assuming, comparing the small number samples in time domain allows simultaneous optimization of frequency characteristics and elimination of dc offset. The filter pair referred to above was designed in gC-studio [17] and synthesized by means of SI-studio [9].

Sampled values of impulse responses on both outputs of the SI filter pair have been presented on Figs. 3 and 4. These figures show substantial improvement of the responses. Values of samples after optimization, marked as (+), almost entirely match ideal responses, marked as (o), as opposed to the result before optimization, marked as (x). It is noteworthy that in the time response of 5th order filter, the values of the first 36 samples are prevalent. Similarly to responses in time domain, also the frequency characteristics presented in Figs. 5 and 6 after optimization almost entirely match the ideal characteristics.

Table 1 presents key parameters related to optimization process by means of Hooke-Jeeves algorithm. Completion of the algorithm activity takes place upon reaching the set number of iterations. Special attention should be paid to the goal function value, which is minimized in the optimization procedure. This value shows significant improvement of the designed circuit. However, such improvement is achieved in a time-consuming process. Duration of single iteration amounts to approximately 11s and is used mainly to perform ELDO simulation.

To recapitulate, in the presented example, the SI analysis filter pair was designed by means of special tools that support the design process of analog circuits. However, its

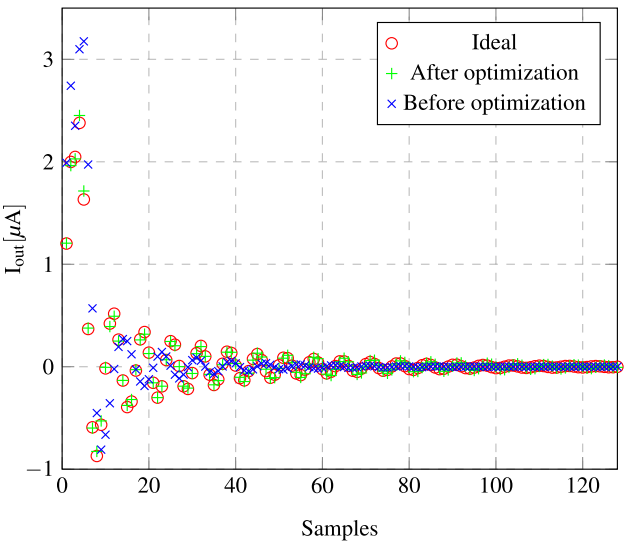

Fig. 3 Impulse response on the low-pass output

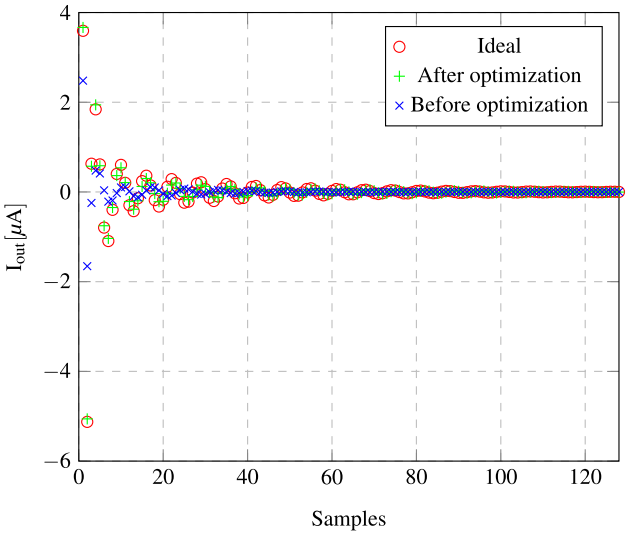

Fig. 4 Impulse response on the high-pass output

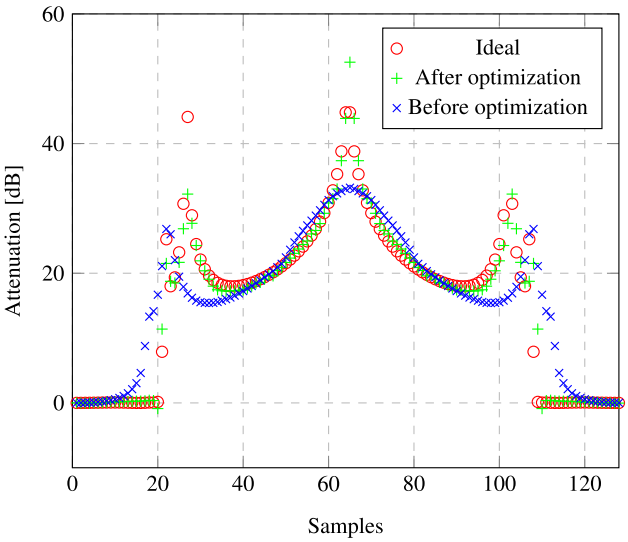

Fig. 5 Magnitude response on the low-pass output(the 62-d sample corresponds the Nyquist frequency, $\omega_N = \omega_s/2$, while the 124-th one corresponds to the sampling frequency, $\omega_s = 2\pi/T$, where $T = 1$)

implementation in advanced CMOS technologies requires additional adjustment. Optimization was done on the basis of comparison between ideal time responses of the prototype filter and discrete responses of the filter implemented in SI technique. Such approach on one hand results in reduction of the number of samples needed for optimization, and, on the other, eliminates dc offset in time responses. Using the proposed optimization method, frequency characteristics of the filter pair were adjusted on a range that is sufficient for precise signal processing.

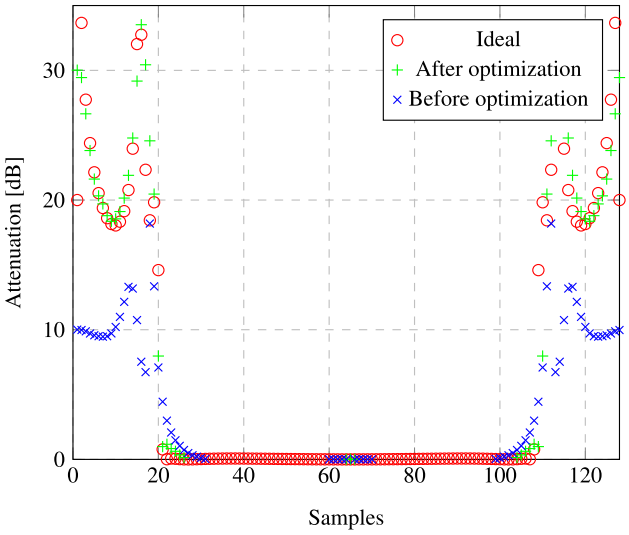

Fig. 6 Magnitude response on the high-pass output(the 62-d sample corresponds the Nyquist frequency, $\omega_N = \omega_s/2$, while the 124-th one corresponds to the sampling frequency, $\omega_s = 2\pi/T$, where $T = 1$)

Table 1 Key parameters of the optimization process

Parameter name	Value
Number of variables	60
Optimization time [hh:mm:ss]	20:22:53
Number of the called simulations	6670
Value of the goal function before optimization	57421.020679
Value of the goal function after optimization	2.240521

5 Design method of the synthesis multiport filter

Synthesis filters are usually designed as FIR filters, which results in a large number of required multiplying elements. We will demonstrate that they can be implemented as IIR filters, using a gC multiport circuit, just like in the case of the analysis filter. For this purpose, we transform transfer functions (25) and (26) from the analog domain s into the discrete one-z, using bilinear transformation (3). We receive

$$G_0(z) = \frac{A_0' Z}{B' Z}, \tag{29}$$

and

$$G_1(z) = \frac{A_1' Z}{B' Z}, \tag{30}$$

where $Z' = [1 \;\; z^{-1} \;\; z^{-2} \;\; z^{-3} \;\; z^{-4} \;\; z^{-5}]$, whereas

$$A_0 = (P_0' T_5)', \quad A_1 = (P_1' T_5)', \quad B = (Q' T_5)'. \tag{31}$$

Since matrix T_5 in the relationship (3) is given for the sampling period $T = 2$, it would require 2-fold reduction of frequencies in transfer functions $G_0^a(s)$ and $G_1^a(s)$. In case of FI ADC this scaling should be left out due to required $M = 2$, which means simultaneous doubling of frequency.

Based on (31) we receive $A_0 ini$, $A_1 ini$, $Bini$. These are, however, coefficients for the values of initial capacitances and transconductances of a prototype gC circuit. This circuit is optimized in NANO-studio environment so as to meet PR condition, (20), (21). Optimization is performed in time domain as per relationship (22). The impulse response, received as a result of optimization for 36 samples in time domain, is presented in Fig. 7. Received final values of A_0, A_1, B coefficients directly provide digital filter of a canonical structure.

Digital synthesis filters may also be designed by means of indirect method presented in p.6.3.3 in [5]. It provides full use of prototype lossless circuit properties for obtaining a filter with low sensitivity to parameter changes.

The optimized synthesis filter was implemented in Verilog language using Spiral [24], a generator of digital filters with optimum structure based on fixed-point arithmetic.

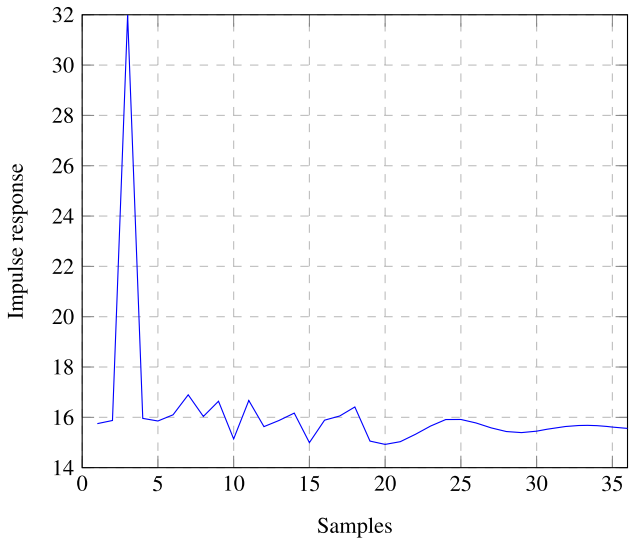

Fig. 7 Delayed impulse response on the synthesis filter output

In this paper we are focusing on analysis and synthesis filter design. However in FI ADC shown in Fig. 1 we need two sub-ADCs between these filters. In our work such role play 5-bit analog-to-digital converters implemented in C language. This allowed us to avoid calculations for real converters in ELDO simulator and, as a result, significantly accelerate synthesis filter optimization. Practical implementation of such sub-ADCs in standard CMOS technology, using continuous time integrators in current mode, has been presented in the paper [11].

6 Filter banks based on multiport networks

Design of IIR analysis and synthesis filters have been based in previous sections on the filter pair. For the set cutoff frequencies and attenuation values, coefficients P_0, P_1, Q of transfer function polynomials (25) and (26) can be obtained in closed-form solutions, just like in the case of ladder structures. Multiport networks with higher number of ports do not share this important property. Hence the commonly used implementation both for analysis and synthesis filters is to use FIR filters. The required coefficients are then directly obtained, although the implementation of these filters demands high number of multiplying elements, [13]. Based on the structure with three frequency bands in Fig. 1, we will demonstrate how the method of designing IIR filter banks with port number higher than 3 should be modified. New approach is based on reverse order in filter design: first, the synthesis filter and next, on the second stage, the analysis filter are implemented.

As a prototype circuit of the synthesis filter, a single-output 4th order gC multiport network has been used with three inputs, corresponding to lower, middle, and upper bands. It is described in VHDL-AMS language in the Appendix.

Therefore, this circuit consists of three input conductances, one output conductance and five free capacitances, as well as 17 gyrators. At the stage of synthesis filter design, so far unknown analysis filter is replaced with three elliptic filters of 6th order (of 3rd order for bandpass filter) with the parameters: ripple errors in passbands 0.3dB, attenuations in stopbands 30dB and cutoff frequencies of 1/3 and 2/3 rd/s, respectively. For these parameters, in the MATLAB environment with the use of ellip() function, we receive transfer function coefficients in z domain.

4th order transfer functions of a prototype gC circuit are obtained in a symbolic form by means of gC-studio, [8, 17], and then bilinearly transformed into discrete domain. IIR filter bank received as a result has the following transfer functions

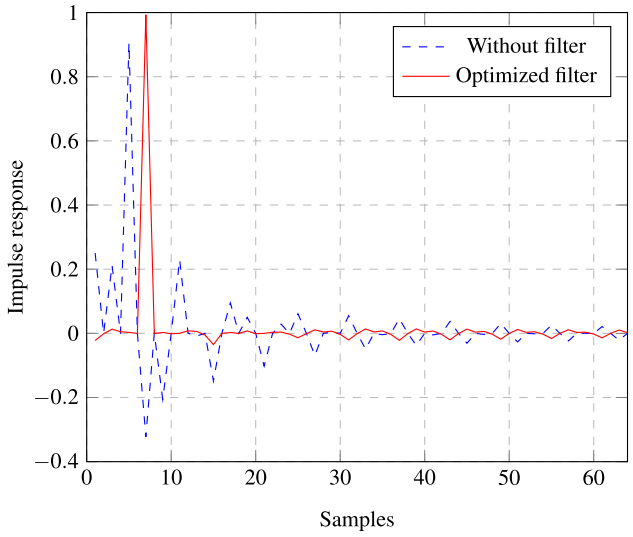

Fig. 8 Impulse responses with the use of the optimized synthesis filter (solid red line) and without this filter (dashed blue line)

$$H_l = \frac{A'_l Z}{B' Z}, \quad H_c = \frac{A'_c Z}{B' Z}, \quad H_h = \frac{A'_h Z}{B' Z}, \tag{32}$$

for each of the three subsequent bands, respectively, where $Z' = [1 \;\; z^{-1} \;\; z^{-2} \;\; z^{-3} \;\; z^{-4} \;\;]$.

Polynomial coefficients in transfer functions (32) depend on the parameters of gC circuit elements, which are the optimization variables. The whole structure is described by transfer functions, being the respective products of transfer functions of the 6th order elliptic filters and (32). In result of optimization by means of NANO-studio tool, we obtain the delayed by 7 samples version of the input impulse, presented in Fig. 8. The same figure presents a response (blue dashed line) when synthesis filter is not present, that is, when transfer functions (32) have the unit value: $H_l = H_c = H_h = 1$.

Transfer function polynomial coefficients (32) obtained as a result, are as follows

$$\begin{aligned}
A'_l &= [a_{l0} \;\; a_{l1} \;\; a_{l2} \;\; a_{l3} \;\; a_{l4}] \\
&= [-0.0376 \;\; -0.0551 \;\; 0.3180 \;\; 0.3956 \;\; 0.1140], \\
A'_c &= [a_{c0} \;\; a_{c1} \;\; a_{c2} \;\; a_{c3} \;\; a_{c4}] \\
&= [0.2179 \;\; -0.1439 \;\; 0.9991 \;\; -0.4320 \;\; -0.4579], \\
A'_h &= [a_{h0} \;\; a_{h1} \;\; a_{h2} \;\; a_{h3} \;\; a_{h4}] \\
&= [-0.6964 \;\; -1.0903 \;\; -0.2780 \;\; -0.0684 \;\; 0.9986], \\
B' &= [b_0 \;\; b_1 \;\; b_2 \;\; b_3 \;\; b_4] \\
&= [1.0636 \;\; -0.2837 \;\; -0.1590 \;\; 0.0376 \;\; 0.0339].
\end{aligned} \tag{33}$$

The spread of values of the above coefficients is $1.0636/0.0339 = 31.4$. The received circuit has two pairs of coupled complex poles $0.4350 \pm 0.2376i$, $-0.3017 \pm 0.1968i$, the position of which, presented in Fig. 9, confirms stability of the synthesis filter, inherited after the prototype passive gC circuit.

The structure of the received synthesis filter, with multiplier values given in (33), is presented in Fig. 10. The implemented IIR bank contains only $4 \cdot 4 = 16$ multipliers, hundreds of which may be present in FIR structures, with a high spread of their values [14]. Furthermore, let us mention that thanks to the prototype gC circuit, being lossless,

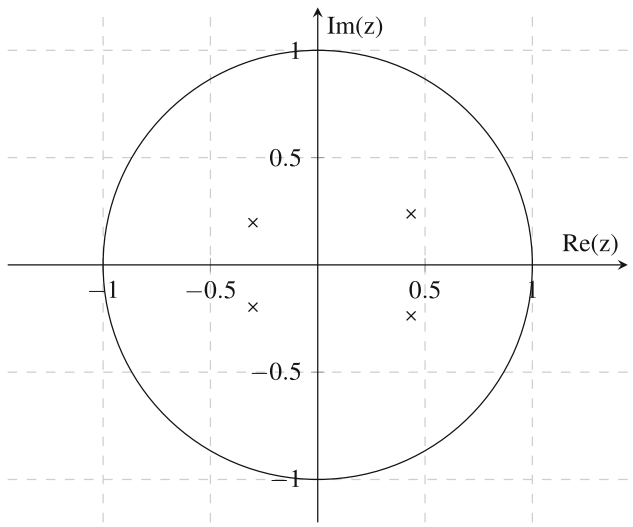

Fig. 9 Roots location of the stable synthesis filter

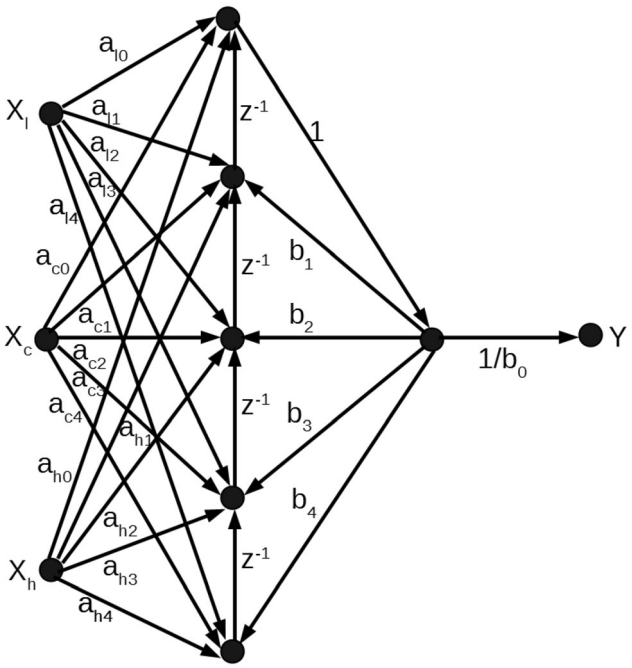

Fig. 10 Direct form I structure of the four port synthesis filter containing 3 inputs and 1 output

the presented method implements the design strategy of stable IIR filters with low sensitivity to circuit parameter changes.

As mentioned at the beginning of this section, after designing the multiport synthesis filter, we can move to a second stage, that is, implementation of the analog bank of analysis filters. Similarly as in the case of synthesis filter, a prototype gC circuit is looked for first. Its counterpart circuit can be implemented in the SI technique, as it was shown for the filter pair.

7 Conclusions

Optimization methods presented in the paper allow to obtain high precision signal processing in analysis and synthesis filters for FI ADC. The analog analysis filter is difficult to obtain in advanced CMOS technologies due to their focus on digital circuits. It is associated with relatively high technological pitch as compared with the sizes of transistor channels, which are in the order of several dozens or even a dozen or so nanometres. NANO-studio environment allows optimization of analysis filter characteristics, taking into account such pitch. This environment is also very effective in the process of digital synthesis filter optimization. It has been demonstrated that taking into account low number of time samples is sufficient to meet PR condition. In the FI ADC example, pairs of analysis and synthesis filters have been used. An additional example of three-filter bank demonstrates full potential of the developed NANO-studio software. All filter types are designed on the basis of the lossless multiport gyrator-capacitor (gC) prototype circuit, as per the strategy of designing circuits with low-sensitivity to parameter changes. Additional advantage of using this multiport circuit is represented by filters with low number of elements, integrators and multipliers, as compared with traditional design techniques.

Appendix

[VHDL-AMS description of the gC prototype circuit]

The prototype circuit of the synthesis filter, used in Sect. 6, is described in VHDL-AMS language as follows:

```
library VLSI;
use VLSI.SI.all;
entity 3inBank is port (
        terminal input VinL : electrical;
        terminal input VinC : electrical;
        terminal input VinH : electrical;
        terminal output Vout : electrical;
        terminal ground gnd: electrical);
end entity 3inBank;
architecture bank_arch of 3inBank is
variable v1,v2,v3,v4,v5,v6,v7 : real;

begin
---- input elements
-- LP input
G1 : GC_CON port map (Ni=>VinL, Nj=>v1);
C1 : GC_CAP generic map(dim=>1)
     port map (Ni=>v1, Nj=>v4);
ig1 : GC_GYR port map( Ni=>v1, Nj=>v4);
-- CP input
G2 : GC_CON port map (Ni=>VinC, Nj=>v2);
C2 : GC_CAP generic map(dim=>1)
     port map (Ni=>v2, Nj=>v4);
ig2 : GC_GYR port map( Ni=>v2, Nj=>v4);
-- HP input
G3 : GC_CON port map (Ni=>VinH, Nj=>v3);
ig3 : GC_GYR port map( Ni=>v3, Nj=>v4);
---- chain elements
ig4 : GC_GYR port map( Ni=>v4, Nj=>v5);
C4 : GC_CAP generic map(dim=>1)
     port map (Ni=>v4, Nj=>v5);
ig5 : GC_GYR port map( Ni=>v5, Nj=>v6);
C5 : GC_CAP generic map(dim=>1)
     port map (Ni=>v5, Nj=>v6);
ig6 : GC_GYR port map( Ni=>v4, Nj=>v6);
C6 : GC_CAP generic map(dim=>1)
     port map (Ni=>v4, Nj=>v6);
-- output node
ig7 : GC_GYR port map( Ni=>v6, Nj=>v7);
ig8 : GC_GYR port map( Ni=>v5, Nj=>v7);
G4 : GC_CON port map (Ni=>v7, Nj=>gnd, Vo=>Vout);
---- gyrators from inputs to chain nodes
-- LP input
ig11 : GC_GYR port map( Ni=>v1, Nj=>v5);
ig12 : GC_GYR port map( Ni=>v1, Nj=>v6);
-- CP input
ig21 : GC_GYR port map( Ni=>v2, Nj=>v5);
ig22 : GC_GYR port map( Ni=>v2, Nj=>v6);
-- HP input
ig31 : GC_GYR port map( Ni=>v3, Nj=>v5);
ig32 : GC_GYR port map( Ni=>v3, Nj=>v6);
---- gyrators betwen inputs
ig41 : GC_GYR port map( Ni=>v1, Nj=>v2);
ig42 : GC_GYR port map( Ni=>v1, Nj=>v3);
ig43 : GC_GYR port map( Ni=>v2, Nj=>v3);

end architecture;
```

This circuit, described in VHDL-AMS, is composed of 4 conductances, 5 capacitances and 17 gyrators. Only the part of the schematic is shown in Fig.11. The omitted gyrators are represented by dashed lines. Full schematics of simpler gyrator-capacitor circuit structures are presented in the literature [6].

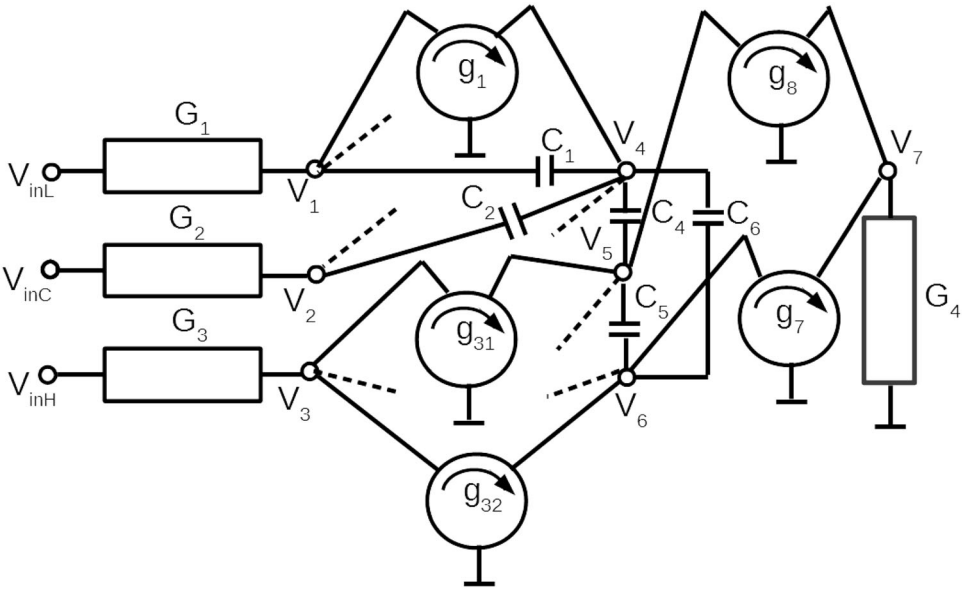

Fig. 11 Simplified schematic of the gyrator-capacitor circuit described in VHDL-AMS, the omitted gyrators are represented by dashed lines

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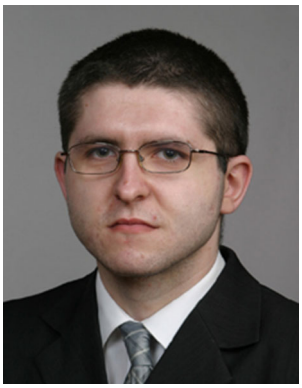

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