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MIXED SIGNAL LETTER

A 0.25–1.0 V fully synthesizable three-stage dynamic voltage comparator based XOR&XNOR&NAND&NOR logic

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Abstract
To improve the performance of all-digital synthesizable comparators for the stochastic circuit, we present a three-stage rail-to-rail fully synthesizable dynamic voltage comparator. Compared with the state-of-the-art designs, the proposed comparator uses *XOR*, *XNOR*, *NAND*, and *NOR* logic gates to further improve the comparator's common-mode input range, offset, speed and power-delay product (PDP). The comparator is implemented on CMOS 45 nm technology, operating with a supply voltage of 250 mV–1.0 V. The comparator has reduced the delay by 0.70 to 0.82×, increased the standard deviation of offset by 1.28 to 1.65× and reduced the PDP down to 0.67× compared to *NAND* & *NOR*-based comparator. Hence, these improvements help to increase the performance of the stochastic Flash ADC, and improve the reliability of the stochastic PUF circuit.

Keywords Digital gates · Standard cells · Synthesis · Analog-to-digital converter (ADC) · Flash ADC · Stochastic ADC · Physical unclonable function (PUF)

1 Introduction

The traditional analog circuit requires careful custom-designed and layout matching, resulting in a higher design cost and a longer design cycle. The continuous scaling of the feature sizes in advanced CMOS technology allows digital circuits to achieve a more competitive cost, area, and power consumption compared to analog circuits. If an analog circuit design can be entirely written in Verilog and synthesized into digital standard cells with similar circuit performance, it will significantly reduce design time, and cost while enhancing the portability and scalability of analog circuits. Hence, analog circuit designers need to consider all-digital design method, reducing complexity, and improving productivity.

In recent years, we have witnessed different types of synthesizable digital design, such as comparator, analog-to-digital converters (ADC) [1–8], time-to-digital converter (TDC) [9, 10], filter [11], physical unclonable function (PUF) [12–14], low-dropout regulator (LDO) [15], phase-locked loop (PLL) [16], delay-locked loop (DLL) [17], transmitter [18, 19]. Since this research direction is relatively new, there are many ongoing works to improve the performance of these state-of-the-art designs.

Synthesizable comparator is the key building block for stochastic based circuits, such as stochastic based Flash ADC [1, 2, 8], TDC [9], PUF [12, 13], and sensor system [20]. Stochastic PUFs [12, 13] leverage on the variation in the comparator's offset to generate a random sequence. Reference [12, 13] reported that comparator should be designed to have a large variation in the offset to generate a reliable output across varying environmental conditions. In another example, Fig. 1(a) illustrates a new type of ADC architecture, stochastic Flash ADC, that leverages on the variation in comparator's offset to provide intrinsic voltage references. Since the comparator's offset follows Gaussian random distribution, the summation of the outputs follows the cumulative distribution function (CDF) of the comparator's offset, eliminating the need for a power-hungry resistive ladder. Hence, an inverse Gaussian CDF function is implemented to linearize the ADC's output [1]. An *N*-bit stochastic Flash ADC requires a minimum of 2×4^N

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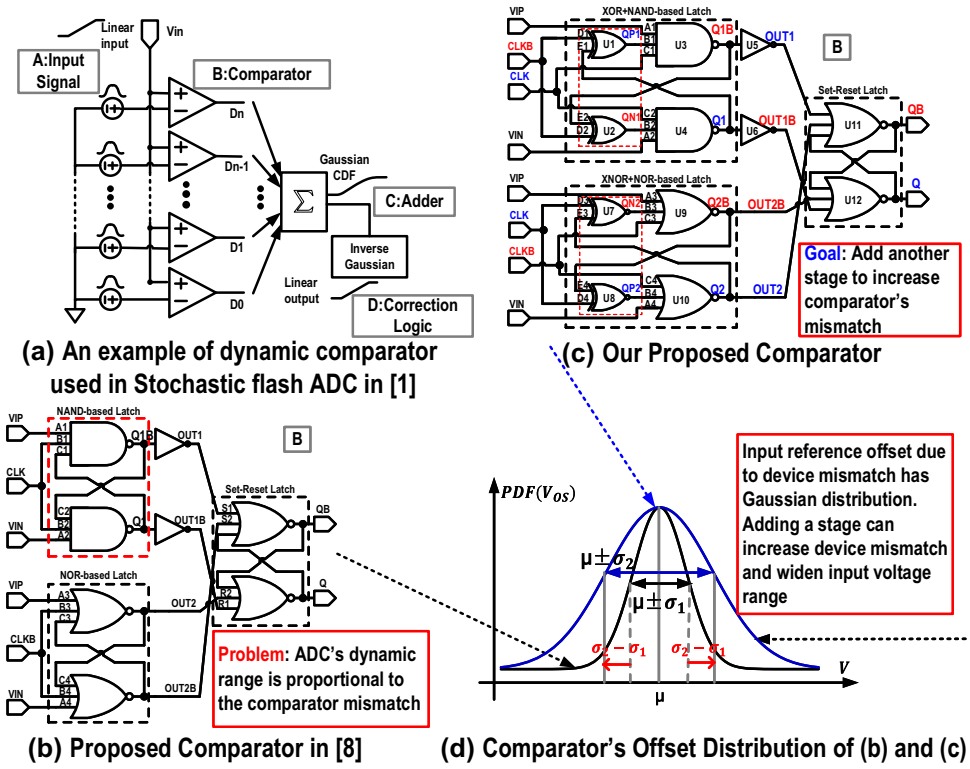


Fig. 1 **a** An example of dynamic comparator used in Stochastic flash ADC [1], **b** *NAND&NOR*-based comparator [8], **c** our proposed fully-synthesizable *XOR+NAND&XNOR+NOR*-based comparator, **d** comparator's offset distribution

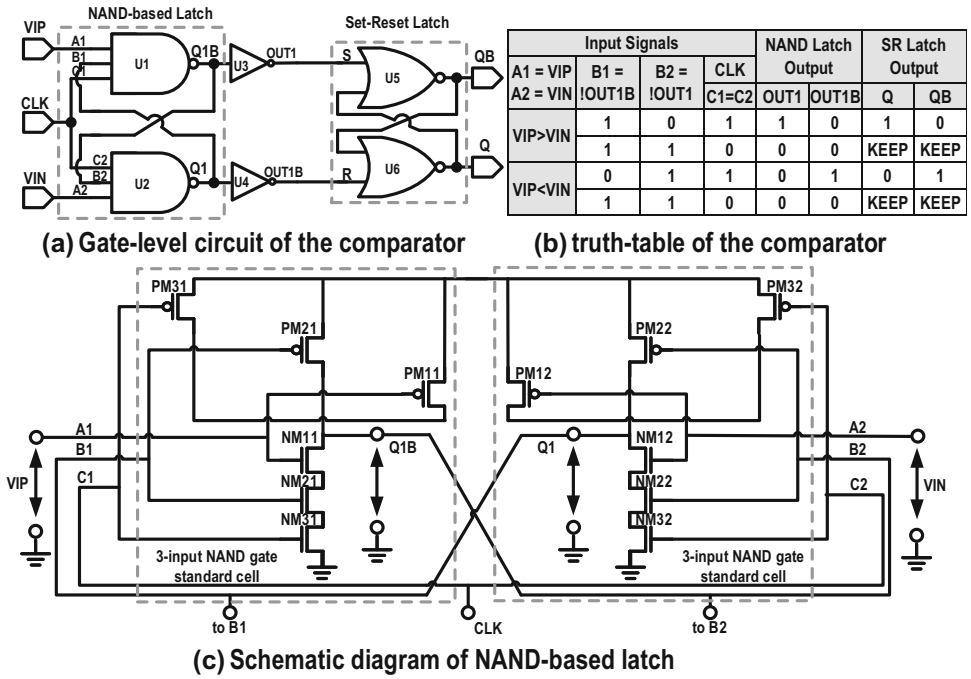
number of comparators [1] and its input dynamic range is associated with the comparator's offset and common-mode input range. The first reported synthesizable stochastic ADC [1] uses a *NAND*-based comparator, which faced a limitation in the common-mode input range. The input dynamic range of the ADC is approximately from $-\sigma$ to $+\sigma$, where σ is the standard deviation of the comparator's offset [1]. Reference [2] uses multiple groups of comparators, biased at different common-mode voltage to extend the input dynamic range, allowing a configurable resolution, dynamic range, and power consumption for various applications. Both architectures have a limited common-mode input range since the input transistors need to be high enough to ensure input-connected PMOS transistors are in the cut-off region [3, 8]. A new type of comparator is proposed in [3, 8], by combining 2-to-5-input *NAND*-based and *NOR*-based comparator to extend its common-mode range (Fig. 1(b)) at the expense of increasing area and power consumption. Hence, there is a need to explore a new type of synthesizable comparator to further improve its intrinsic offset variation to increase the stochastic ADC's input dynamic range [1, 2] and improve the reliability of the stochastic PUF circuit [12, 13], and reduces its delay to achieve a higher operating frequency/throughput.

As shown in Fig. 1(c–d), we explored a different combination of standard cell logic and proposed a new dynamic voltage comparator using *XOR*, *XNOR*, *NAND*, and *NOR* logic gates (Fig. 1(c)) to further improve the common-mode range, speed, offset and power-delay product (PDP) compared to the state-of-the-art designs [1–3, 8]. Our comparator has reduced the delay by 0.70-to-0.82×, increased the standard deviation of offset by 1.28-to-1.65× and reduced the PDP down to 0.67× compared to *NAND&NOR*-based comparator [8]. Hence, the new design can be used to increase the performance of the stochastic Flash ADCs [1, 2], and improve the reliability of the stochastic PUF circuits [12, 13].

The rest of the paper is organized as follows. Section 2 reviews the state-of-the-art synthesizable comparators. Section 3 describes the proposed architecture and explains the functional blocks of the architecture. Section 4 details the verification results of our proposed comparator and analyzes its performance. Finally, conclusions are drawn in Sect. 5.

2 Synthesizable *NAND*-based and *NAND & NOR*-based comparators

As shown in Fig. 2(a), the synthesizable dynamic comparators are made up of a regenerative latch, and an SR latch [1, 2, 7, 8, 21]. These latches can be made up of *NAND3* (three-input *NAND* logic gate), and *NOR2* (two-input *NOR* logic gate) logic gates, respectively [1]. The input and output terminals of the *NAND*-based comparator



Input Signals				NAND Latch Output		SR Latch Output	
A1 = VIP A2 = VIN	B1 = !OUT1B	B2 = !OUT1	CLK C1=C2	OUT1	OUT1B	Q	QB
VIP>VIN	1	0	1	1	0	1	0
	1	1	0	0	0	KEEP	KEEP
VIP<VIN	0	1	1	0	1	0	1
	1	1	0	0	0	KEEP	KEEP

Fig. 2 Fully synthesizable comparator with *NAND*-based input stage **a** gate-level circuit, **b** truth-table of the comparator, and **c** schematic diagram of a *NAND*-based latch circuit

are expressed in the truth table, as shown in Fig. 2(b). The differential input signals, non-inverting *VIP* and inverting *VIN*, are connected to input terminals, *A1* and *A2*, of the *NAND3* logic gates. The input terminals, *B1* and *B2*, are connected from the output signals, *Q1B* and *Q1*, in a cross-coupled structure. The input terminals, *C1* and *C2*, are connected to the sampling clock signal, *CLK*.

NAND-based regenerative latch Upon careful observation of the *NAND3* schematic diagram (Fig. 2(c)), the synthesizable dynamic comparator resembles an analog-input comparator if the common-mode of the input terminals is high enough to ensure that the PMOS transistors (PM11 and PM12), connected to the input terminals, are in the cut-off region. When the clock signal, *CLK*, is at the logic-low signal (reset phase), both output terminals, *Q1* and *Q1B*, are reset to the logic-high signal (supply voltage, *VDD*). When the clock signal, *CLK*, becomes the logic-high signal (comparison phase), the output terminals begin to discharge through the NMOS transistors. The discharge rate depends on the capacitance on the output terminals and the current through these transistors. When one of the output nodes discharges below a PMOS threshold voltage, the cross-coupled connection creates a positive feedback that causes the comparator to force the outputs to the supply rails.

SR latch A static Set-Reset (SR) latch consists of a cross-coupled *NOR* logic gate, and it is connected to the output terminals of the regenerative latch. The SR latch holds the output data valid even if the comparator is in the reset phase. The SR-latch input is buffered with inverters to reduce a memory-effect on the comparator due to the SR-latch.

3 Our synthesizable comparator architecture

XOR+NAND&XNOR+NOR-based regenerative latch As discussed in Sect. 1, the performance of stochastic flash ADC [1, 2, 8], stochastic TDC [9], and PUF [12, 13] circuits, are largely limited by the common-mode input voltage, offset, and speed of the comparator. We have carefully revisited the *NAND*-based comparator and proposed a new type of comparator based on the combination of *XOR+NAND*-based regenerative latch and *XNOR+−NOR*-based regenerative latch. As shown in Fig. 1(c), our proposed regenerative latch can be divided into two stages: *XOR* and *XNOR* logic gates as the first stage, and *NAND* and *NOR* logic gates as the second stage. By observing and comparing the comparators between Fig. 1(b) and (c), we have added *XOR* and *XNOR* logic gates in the *NAND*-based and *NOR*-based comparators, respectively. The cross-coupled output signals *Q1* and *Q1B* are connected to the input terminals of the *XOR* logic gate instead of the terminals from the *NAND* logic gate. To ensure the proper functionality of the comparator, a logic-low signal (ground voltage), *VSS*, is connected to the input terminal of the *XOR* logic gate. The input and output terminals of the proposed comparator are expressed in the truth table, as shown in Table 1.

Table 1 Truth table of our proposed comparator

VCM Cond.	Input Signals					Internal Signals				XOR + NAND Latch Output		XNOR + NOR Latch Output		SR Latch Output	
	A1 = A3 = VIP, A2 = A4 = VIN	CLK= C1,C2	CLKB= C3,C4	VSS= D1,D2	VDD= D3,D4	B1	B2	B3	B4	OUT1 != E2	OUT1B != E1	OUT2 = E3	OUT2B = E4	Q	QB
VDD/2 < VCM	VIP>VIN	1	0	0	1	1	0	0	0	1	0	0	0	1	0
		0	1	0	1	0	0	1	1	0	0	0	0	KEEP	KEEP
	VIP<VIN	1	0	0	1	0	1	0	0	0	1	0	0	0	1
		0	1	0	1	0	0	1	1	0	0	0	0	KEEP	KEEP
VDD/2 > VCM	VIP>VIN	1	0	0	1	1	1	1	0	0	0	1	0	1	0
		0	1	0	1	0	0	1	1	0	0	0	0	KEEP	KEEP
	VIP<VIN	1	0	0	1	1	1	0	1	0	0	0	1	0	1
		0	1	0	1	0	0	1	1	0	0	0	0	KEEP	KEEP

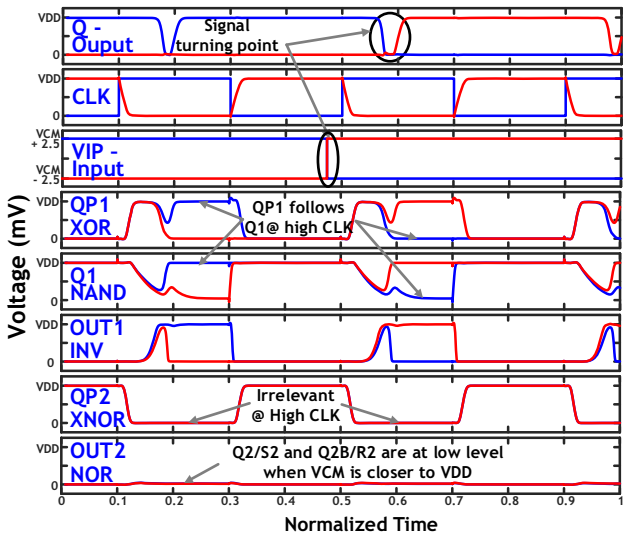


Fig. 3 Signal behavior of the propose comparator for common-mode input voltage, *VCM*, is nearer to *VDD*

The behavior simulation results of our proposed comparator are shown in Fig. 3. During the reset phase, the clock signal, *CLK*, is at a logic-low signal (ground voltage), the nodes *Q1* and *Q1B* are precharged to the logic-high signal (supply voltage), *VDD*. Similarly, the output signals of *NOR*-based latch, *OUT2*, and *OUT2B*, are at a logic-low signal (ground voltage) because one of the *NOR* logic gate's input terminal is connected to *CLKB*, which is inverted to a logic-high signal. During the comparison phase, the clock signal, *CLK*, changes to a logic-high signal (supply voltage), the outputs will begin to discharge the charge through the NMOS transistors in the *NAND* logic gate. The input terminals of the *NAND* logic gate are connected to the output terminals of the *XOR* logic gate instead of the feedback signals *Q1* and *Q1B*. The *XOR* logic gate acts as a buffer to improve the slew rate of the signal, thus improve the delay of the comparator. According to the symmetry of digital circuit, replacing *XOR* logic gates with *XNOR* logic gates, *CLK* with *CLKB*, and *VSS* with *VDD*, *XNOR* + *NOR*-based regenerative latch will have the same function as the *XOR* + *NAND*-based Latch.

Multi-input SR latch When the common-mode input voltage, *VCM*, is nearer to supply voltage, *VDD*, the output signals from *XNOR+NOR*-based latch stuck at the precharge value *VSS*, as shown in Fig. 3. Similarly, the outputs of the *XOR+NAND*-based latch are stuck at the precharge value *VDD* when *VCM* is closer to *VSS*, which will be inverted to *VSS*, ensuring the multi-input SR latch operates correctly. In both cases, only one of the two latches (*XOR+NAND*-based or *XNOR+NOR*-based) works correctly. Hence, a multi-input *SR* latch, with two groups "set" and "reset" inputs (*S1*, *R1*) and (*S2*, *R2*), is required to handle the output signals (*OUT1*, *OUT1B*) and (*OUT2*, *OUT2B*) from our proposed *XOR+NAND*-based and *XNOR+NOR*-based latches, respectively. Since the SR latch is a three-input *NOR* logic gate, the additional devices led to an increase in device mismatch, which is beneficial for stochastic circuit design.

Circuit analysis The implementation of *XOR/XNOR* logic gate can be done in multiple ways (e.g. complementary CMOS, complementary/double pass-transistor, and rail input logic design) and typically it requires up to fourteen (14) transistors [22]. In the complementary CMOS standard cell design, the *XOR/XNOR* logic gates require twelve (12) transistors. The increased number of transistors in these logic gates increases the variability in the design [21]. As shown in Fig. 1(c), since the feedback signals, *Q1* and *Q1B*, are now connected to the complementary inverter logic gate (*INV*) instead of the *NAND/NOR* logic gates, the logic effort has reduced from 4/3 (*NAND*) and 5/3 (*NOR*) to 1 (*INV*). These feedback signals are amplified after *XOR/XNOR* logic, resulting in signals' amplitude connecting to *NAND/NOR* logic and reducing the overall delay. From our analysis, our proposed architecture is expected to achieve a higher input voltage offset and speed compared to the *NAND&NOR*-based comparator.

4 Design verification and discussion

In this work, we have designed and verified the *NAND*-based comparator [1], the *NAND&NOR*-based comparator [8], and our proposed comparator using the 45nm CMOS technology. The performance of these comparators is summarized in Table 2. These comparators are evaluated at three different supply voltages, *VDD* of 0.25 V (sub-threshold voltage), 0.6 V (near-threshold voltage), and 1.0 V (operating near nominal supply voltage).

Delay/speed The clock-to-output propagation delay and power consumption are compared by varying the common-mode input voltage from *VSS* to *VDD* with a differential input voltage (*vdiff*) of 5 mV. Figures 4(a–c) and 5(a–c)

Table 2 Comparison with state-of-the-art comparators

Specifications	Supply Voltage (mV)	NAND [1]	NAND & NOR[8]	Our work	Best Case Differences
Technology	-	CMOS 45nm			-
Max. Delay (ns)	250	6,889	17,760	12,860	↓ 0.72×
	600	138	112	92	↓ 0.82×
	1,000	0.459	1.81	1.23	↓ 0.70×
Offset (mV)	250	-	4.8	7.9	↑ 1.65×
	600	-	4.6	5.9	↑ 1.28×
	1000	-	4.9	7.2	↑ 1.47×
Max. Power	250	42.62 pW	130.29 pW	161.39 pW	↑ 1.24×
	600	27.49 nW	54.21 nW	51.14 nW	↓ 0.94×
	1000	2.40 μW	11.98 μW	12.54 μW	↑ 1.05×
PDP (fJ) @25°C, VCM=VDD/2	250	-	2.16 (ss)	2.20 (ss)	↑ 1.02×
		-	2.38 (tt)	2.16 (tt)	↓ 0.91×
		-	2.86 (ff)	2.77 (ff)	↓ 0.97×
	600	-	4.83 (ss)	3.26 (ss)	↓ 0.67×
		-	6.10 (tt)	4.97 (tt)	↓ 0.81×
		-	7.21 (ff)	5.74 (ff)	↓ 0.80×
	1000	-	16.98 (ss)	12.69 (ss)	↓ 0.75×
		-	21.47 (tt)	15.30(tt)	↓ 0.71×
		-	24.73 (ff)	17.90 (ff)	↓ 0.67×
Area (μm^2)	-	21.0752	41.0112	51.6912	↑ 1.26 ×

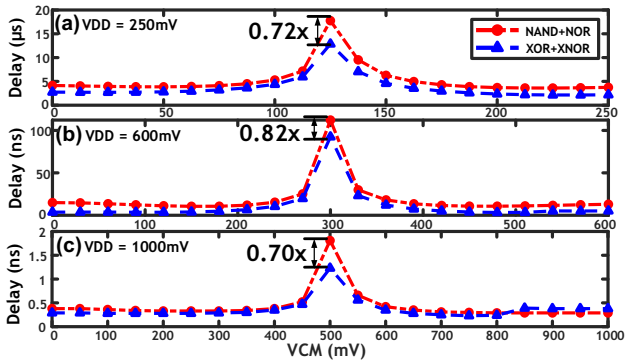


Fig. 4 Clock-to-output propagation delay versus common-mode input voltage (*VCM*) for *NAND&NOR*-based *comparator* and *XOR&XNOR*-based comparator for *vdiff* = 5 mV at **a** *VDD* = 0.25 V, **b** *VDD* = 0.6 V and **c** *VDD* = 1.0 V

show the comparators' propagation delay and power consumption against the common-mode input voltage at a supply voltage *VDD* of 0.25 V, 0.6 V, and 1.0 V, respectively. Similar to the reported results in [8], we have observed that the largest delay occurs when the common-mode input voltage is near half of the supply voltage. However, our proposed circuit reduces the delay by 0.72× (*VDD* = 0.25 V), 0.82× (*VDD* = 0.6 V), and 0.70× (*VDD* = 1.0 V) compared to *NAND&NOR*-based comparator [8].

Voltage offset The standard deviation of the input offset voltage for the two designs is compared using Monte Carlo simulations with 500 runs each. The results are shown in Fig. 6. The standard deviation of our comparator's input offset voltages are 7.9 mV at *VCM* = 175 mV (*VDD* = 0.25 V), 5.9 mV at *VCM* = 420 mV (*VDD* = 0.6 V), and 7.2 mV at *VCM* = 700 mV (*VDD* = 1.0 V), which are 1.65×, 1.28×, and 1.47× compared to *NAND&NOR*-based comparator, respectively. Therefore, the increased offset voltage in our proposed comparator is highly preferable for use in the synthesizable stochastic circuits (i.e. ADC [1, 2, 8], TDC [9] and PUF circuits [12, 13]).

Power consumption Even with the additional logic gates used in our proposed circuit, the power consumption is still comparable to the *NAND&NOR*-based comparator for *VDD* = 0.6 V and 1.0 V. However, at the sub-threshold region (*VDD* = 0.25 V), the slew rate in the feedback signals has been severely degraded due to the transistors operating in the sub-threshold region, resulting in increased power consumption by 1.24×.

Area To allow the comparators to operate at the minimum supply voltage (*VDD* = 0.25 V), we have selected a drive strength of 8×, which is the maximum available logic gate in the standard cell library, for the second stage: *NAND&NOR*-based regenerative latch. The *INV/XOR/XNOR* and multi-input SR latch have a drive strength of 1×. Note that the circuit variations become smaller with the increased drive strength of the logic gate; however, our proposed comparator has enabled us to achieve up to 1.65× offset improvement compared to the *NAND&NOR*-based comparator. The layout area of *NAND*-based comparator, *NAND&NOR*-based comparator and our proposed comparator are shown in Fig. 7. Our comparator requires a total of 12 logic gates with the layout area of 51.69 μm^2.

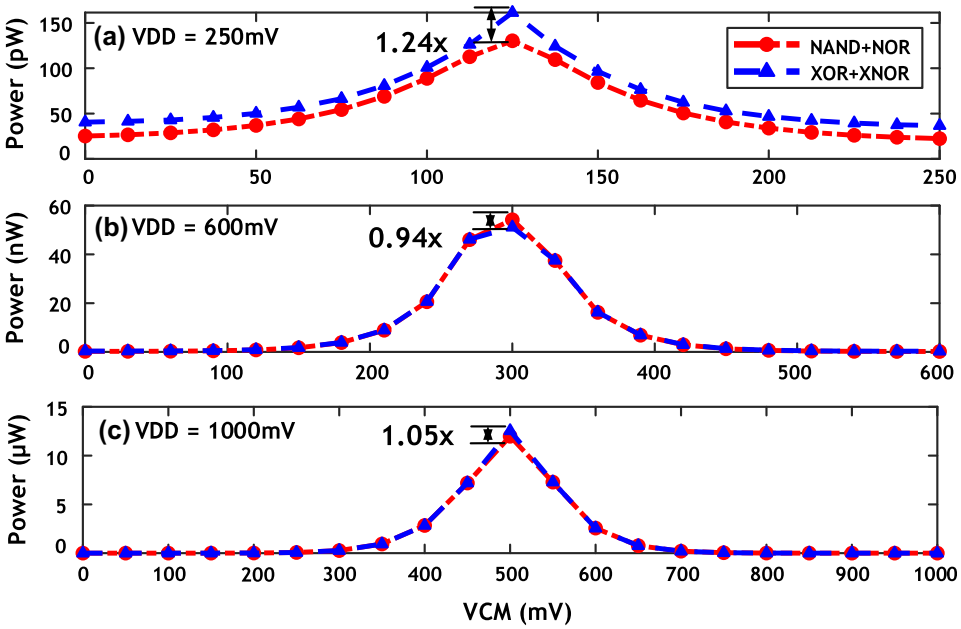


Fig. 5 Power consumption versus common-mode input voltage (*VCM*) for *NAND&NOR*-based comparator and *XOR&XNOR*-based comparator for *vdiff* = 5 mV at **a** *VDD* = 0.25 V, **b** *VDD* = 0.6 V and **c** *VDD* = 1.0 V

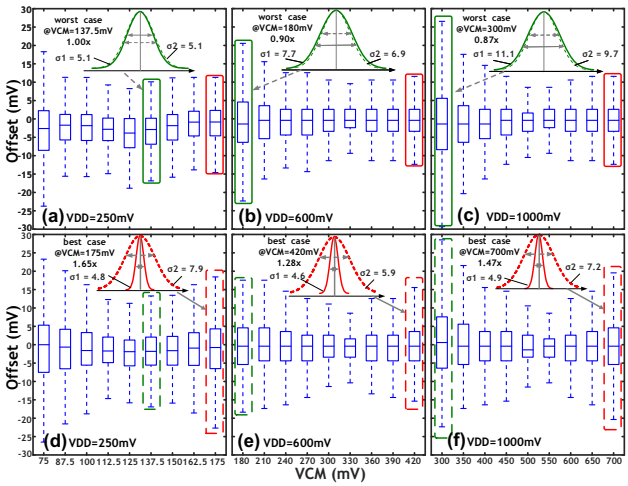


Fig. 6 Input offset voltage of 500 Monte Carlo runs versus common-mode input voltage (*VCM*) for *vdiff* = 5 mV at *VDD* = 0.25 V, 0.6 V and 1.0 V: *NAND&NOR*-based comparator (**a**–**c**), our proposed comparator (**d**–**e**)

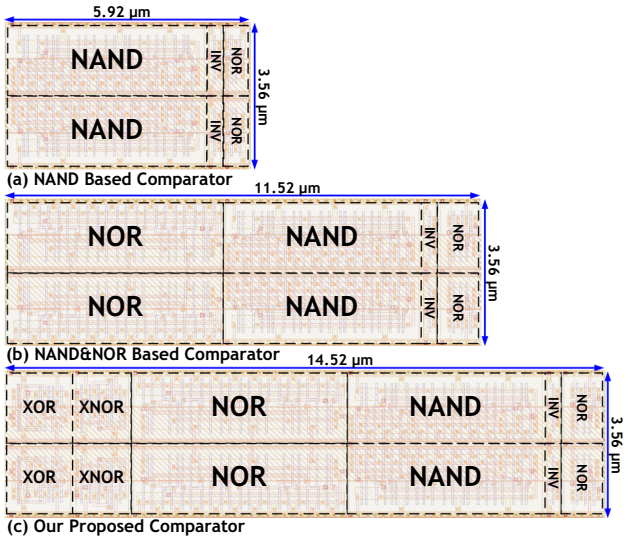


Fig. 7 Layout: **a** *NAND*-based comparator, **b** *NAND&NOR*-based comparator and **c** our proposed comparator

Although our proposed circuit requires an additional area of four logic gates, it has significantly outperformed the state-of-the-art synthesizable comparators [1, 8]. With the continuous scaling of the standard cell in advanced CMOS technology, the improved performance of our proposed circuit outweighs the area penalty.

Power delay product (PDP) analysis across process, voltage, and temperature (PVT) corners PDP is a common figure of merit (FoM) to evaluate the performance of circuits. Since the *VCM* of comparators typically operates near mid of the supply voltage and it has been proven that the circuit achieves an optimum speed and yield when *VCM* is 70% of the supply voltage [23]. Therefore, we have evaluated the PDP of the comparators at different process, voltage, temperature (PVT) conditions. i.e., five process corners: *tt, ss, sf, fs, ff*, three supply voltages: *VDD* = 0.25 V, 0.6 V, 1.0 V, and three temperatures: −40 °C, 25 °C, 125 °C with a *VCM* of *VDD*/2. The PDP simulation result is shown in Fig. 8. Our proposed comparator has reduced the PDP by 0.84× (fs), 0.67× (ss) and 0.67× (ff) when *VDD* = 0.25 V, 0.6 V and 1.0 V, respectively compared to *NAND&NOR*-based comparator. Note

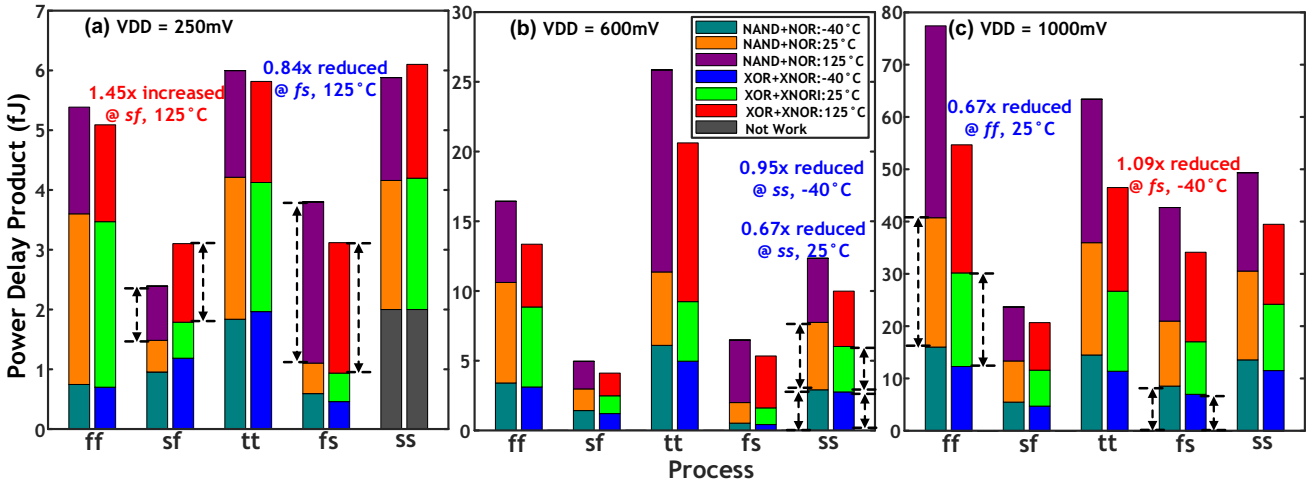


Fig. 8 Power delay product (PDP) at different *process, voltage, temperature (PVT)* conditions. i.e., five process corners: *tt*, *ss*, *sf*, *fs*, *ff*, three supply voltages: $VDD = 0.25\,\text{V}$, 0.6 V, 1.0 V and three temperatures: $-40\,^{\circ}\text{C}$, $25\,^{\circ}\text{C}$, $125\,^{\circ}\text{C}$ at $VCM{=}VDD/2$ and $vidff = 5\,\text{mV}$: **a** $VDD = 0.25\,\text{V}$, **b** $VDD = 0.6\,\text{V}$, **c** $VDD = 1.0\,\text{V}$

that when at a supply voltage of $VDD = 0.25\,\text{V}$ and $VCM = VDD/2$, both *NAND&NOR*-based comparator and the proposed comparator are unable to function correctly at the process of *ss* with a temperature of $-40\,^{\circ}\text{C}$.

5 Conclusion

In this work, we have proposed and presented a new type three-stage rail-to-rail fully synthesizable dynamic voltage comparator, where *XOR* and *XNOR* logic gates are placed in the first stage. A comparison between our comparator and the state-of-the-art works have been analyzed and discussed in detail. These designs are implemented on CMOS 45nm technology, operating with a supply voltage of 250 mV–1.0 V. The comparator has reduced the delay by 0.70-to-0.82×, increased the standard deviation of offset by 1.28-to-1.65×, and reduced the PDP down to 0.67× compared to *NAND&NOR*-based comparator. This work will lay a good foundation to design more complex stochastic based circuits in the near future.

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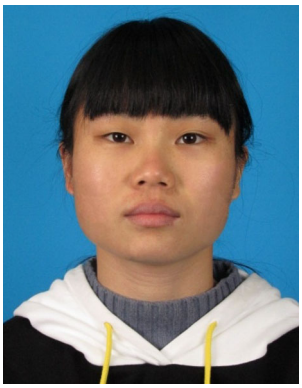

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