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Design of a 40 GHz low noise amplifier using multigate technique for cascode devices

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Abstract

Increased parasitic components in silicon-based nanometer (nm) scale active devices have various performance trade-offs between optimizing the key parameters, for example, maximum frequency of oscillation (f_{max}, gate resistance and capacitance, etc. A common-source cascode device is commonly used in amplifier designs at RF/millimeter-wave (mmWave) frequencies. In addition to intrinsic parasitic components, extrinsic components due to wiring and layout effects, are also critical for performance and accurate modelling of the devices. In this work, a comparison of two different layout techniques for cascode devices is presented to optimize the extrinsic parasitic elements, such as gate resistance. A multi-gate or multi-port layout technique is proposed for optimizing the gate resistance (r_g). Extracted values from measurement results show reduction of 10% in r_g of multi-gate layout technique compared to a conventional gate-above-device layout for cascode devices. However, conventional layout exhibits smaller gate-to-source and gate-to-drain capacitances which leads to better performance in terms of speed, i.e. f_{max}. An LNA is designed at 40 GHz frequency using proposed multi-gate cascode device. LNA achieves a measured peak gain of 10.2 dB and noise figure of 4.2 dB at 40 GHz. All the structures are designed and fabricated using 45 nm CMOS silicon on insulator (SOI) technology.

Keywords mm-wave · RF · LNA · Receiver · 5G · Multi-gate · Communication systems · CMOS · SOI

1 Introduction

Existing wireless communication technology can not cope up with the increasing demands of data rates from wireless networks due to the increased number of multimedia applications and devices. More complex and higher-order modulation techniques, for example, quadrature amplitude modulation (QAM), are inevitably required to meet the next generation network capacity demands. This also requires higher values of signal-to-noise ratio (SNR) of the radio frequency front end (RF FE) modules. Due to the non-availability of enough bandwidth (BW) of existing mobile communication technologies, utilization of unused mmWave frequency bands for fifth generation mobile communication (5G) is needed. Third generation partnership project (3GPP) has standardized the first frequency bands for 5G new radio (5GNR) from 24 to 29 GHz and 39 GHz. Different 5GNR frequency bands with available BW are listed in Table 1.

Moving to mmWave communication also leads to lots of challenges in terms of path loss, scalability, packaging and its associated parasitic effects. Due to that phased arrays are used to increase the antenna aperture in order to compensate free space path loss at mmWave frequencies [2]. Miniaturization of bigger antenna systems is realized using silicon based technologies (CMOS and BiCMOS) which offer integrated solutions for faster and scalable mmWave systems for phased arrays [3]. Applications of silicon based technologies are classified by the performance of their active devices and passive structures. For example, nanoscale bulk CMOS technologies offer ultra fast transistors which are useful for logic or digital circuitry. However, they have low ohmic substrate which results in

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Table 1 Allocated millimeter-wave frequency bands in 5G NR FR2 standard [1]

5G NR FR2 bands	Frequency (GHz)	Bandwidth (GHz)
n257	28	3
n258	26	3.250
n260	39	3

more losses in passive structures. Contrarily, in addition to ultra fast transistors, CMOS silicon-on-insulator (SOI) technology also provides the opportunity to use high resistive substrate to integrate high performing passive structures. Moreover, SOI technology reduces substrate related cross-talk and improves isolation in metal oxide semiconductor (MOS) based switches. Therefore, CMOS SOI technology can be considered as a good candidate for future mmWave integrated systems consisting of RF front ends as well as digital baseband circuitry on the same chip. Gate length of a transistor is considered as the major driving factor towards technology scaling. High frequency performance of a transistor is determined by the gate length and its associated parasitic components, i.e. capacitance and resistance. These parasitic components and their values highly depend on the layout style. For example, instead of single side connection, gate resistance (r_g) of a multi-finger device can be reduced significantly with the dual side connections of poly silicon gate finger to metal 1 (M1) [4]. Advanced silicon technologies offer scalable intrinsic models for transistors including the realistic parasitic components up to few metal layers (e.g. M3). However, signals at mmWave frequency are routed preferably on the higher metal layers due to their reduced metal resistance which necessitates the extension of device terminals from lower to higher metal layers. Modelling of these interconnects are part of the extrinsic model of the device and it relies on the layout techniques adopted by the designer. These parasitic effects (intrinsic and extrinsic) are present in the definition of the maximum oscillation frequency of the device, i.e. f_{max}, and given as,

$$f_{max} = \frac{1}{4\pi}\sqrt{\frac{g_m}{r_g C_{gd}(C_{gs} + C_{gd})}}, \tag{1}$$

where g_m is the transconductance of the device and depends on the current density of the technology, C_{gs} and C_{gd} are the parasitic capacitance at gate terminal. Cascode devices are largely used in amplifier designs due to their benefits of better gain and improved stability conditions. Aforementioned modelling approach of a single device can also be applicable to characterize the CS stage with cascode device and it can be treated as a three terminal device as shown in Fig. 1. The junction between two devices adds

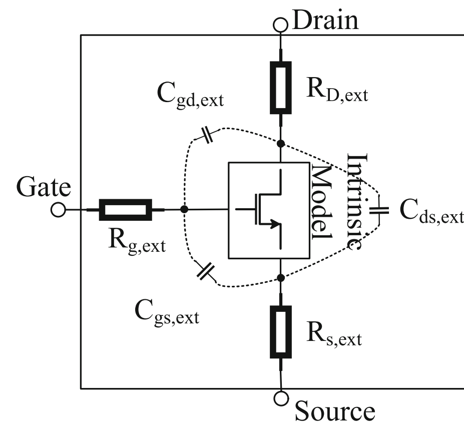


Fig. 1 Extrinsic components of an NMOS transistor

additional wiring in the conventional style of layout, which brings additional parasitic components at this node. For mmWave frequency of operations, this parasitic capacitance is compensated with additional inductance to improve interstage matching [5]. However, these parasitic components can be substantially reduced by removing the additional wiring in the junction and sharing the active area [6, 7].

This paper is an extension to our previous work in [8]. In this paper, two different layout styles are designed, characterized and compared for the key performance parameters. Section 2 describes layout design of cascode devices. Section 3 presents the design techniques for mmWave IC designs such as ground plane, port definition in electromagnetics (EM) simulation tools, etc. A 40 GHz LNA is designed based on multi-gate device and is presented in Sect. 3. Experimental results of device characterization and LNA are discussed in Sect. 4. Conclusions of the paper are given in Sect. 5.

2 Cascode devices

In addition to intrinsic parasitic components, interconnects between devices add additional parasitic effects in the modelling of active devices. These parasitic components are part of the extrinsic model of the device mainly due to the metal wiring and via connections as shown in Fig. 1. Certainly, the device behaviour is dependent on both intrinsic and extrinsic model due to wiring and therefore, they should be characterized carefully for optimum device performance. Silicon foundries provide intrinsic models of active devices which include the parasitic effects from extension of device terminals upto few metal layers. However, further extension of these terminals upto signal routing layer is custom made and these extensions are modeled in extraction tools (e.g. EM or RC extraction).

2.1 Optimization of r_g or f_{max}

Amongst all the other parameters in Eq. 1, gate to drain capacitance (C_{gd}) and gate resistance (r_g) are the most critical in terms of optimum device performance. Cascode devices improve the stability of the amplifier due to increased isolation between input and output (smaller values of C_{gd}). When designing an LNA, the main target towards optimum device performance is to optimize the active device for maximum f_{max} or lowest r_g. Total gate resistance is composed of different contributors from intrinsic and extrinsic vias, external wiring, etc. and is given in [9] as

$$R_{g,tot} = R_h + R_v + r_{via,int} + r_{via,ext} + r_{wire}, \quad (2)$$

where R_h and R_v are horizontal and vertical resistance of a single gate finger, respectively. r_{via} is the resistance of poly to metal contact and r_{wire} is the resistance of interconnect for external wiring. R_h and R_v are included in the intrinsic model of the device. While r_{wire} and part of the r_{via} depend on the external routing. All of these contributors can be reduced to an optimum value by using efficient layout techniques. For example, increasing number of fingers and gate contacts for each finger helps to significantly reduce in values of r_h, r_v, and r_{via}. Intrinsic interconnect $r_{via,int}$ is the resistance from poly to m1 and can be reduced by connecting each gate poly at both ends, as shown in Fig. 2. $r_{via,ext}$ is the extrinsic resistance of via from metal M1 to thick metal layers, e.g. M7.

In addition to various benefits, cascode devices have also limitations of the voltage swing for low voltage power supply designs, and additional wiring capacitance at intermediate node and at the output node. In mm-Wave frequency designs, inter-stage matching is used to resonate out the wiring capacitance between the transistors [7]. However, these junction-based capacitance can be reduced significantly by removing the metal wiring in the junction and sharing the active area between the two devices in cascode. Multigate technique for stacked devices proposed in [6], is one possible way in reducing inter-stage wiring parasitics. In this work, design and comparison of two layout techniques for cascode devices, i.e. conventional style and multi-gate style, is presented. Proposed multi-gate style layout helps to reduce inter-stage wiring as discussed in [6], and allows a larger number of metal M1-to-M5 vias implemented for the same area of device compared to conventional layout. This increased number of metal M1–M5 vias help to further reduce $r_{via,ext}$ as in Eq. 2. These devices are designed and fabricated using 45 nm CMOS SOI technology. Transistor size 20 µm for each layout style having 20 gate fingers is selected for comparison.

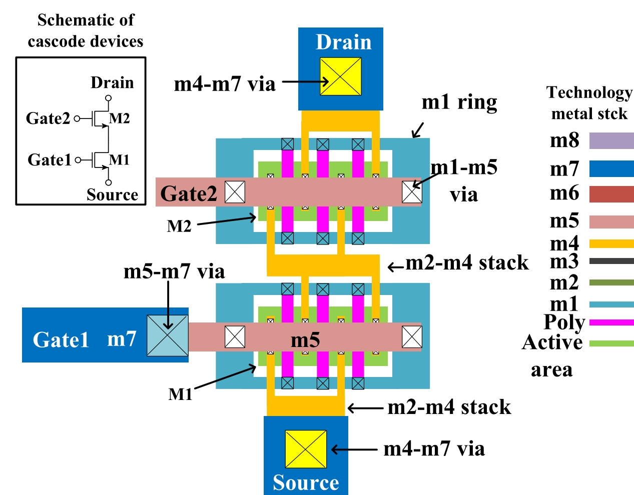


Fig. 2 Conventional-style schematic and layout of cascode devices

2.2 Conventional style layout

Figure 2 shows a conventional gate-above-device layout style of a cascode device [4]. Two transistors are placed in a vertical orientation on top of each other. To reduce $R_{g,int}$ of transistors, gate fingers are double connected from two sides using a ring of metal M1. Input signal from a ground-signal-ground (GSG) pad is routed at metal M7 and brought to M5 near the gate of common-source device M1, which is routed over the transistor and connected gate ring at metal M1 from two sides in the horizontal direction, as shown in Fig. 2. In order to achieve enough current handling capability of metal wires, source and drain connections of each finger is brought up to metal M2 to M4 and connected together with a wider stack of metal layers from M2–M4. These connections are extended further and connected to thick metal layer M7. This further extension of drain and source connections helps to reduce the additional capacitive coupling due to thick metal lines between different nodes, e.g. $c_{gg} = c_{gd} + c_{gs}$.

2.3 Multi-gate style layout

Multi-gate layout technique is drawn by sharing the active area of two transistors to eliminate intermediate metal contacts of drain and source terminals between the transistors for cascode devices [6, 7]. A unit cell of a 1um finger width using multi-gate technique is shown in Fig. 3(a). Each cell has double connected gate finger at metal M1. Source and drain connections are extended further from the device using stack of metal M2–M4. A distribution network of such cells is placed in a vertical orientation such that the gate connection at metal M1 is shared between two cells. A M1–M5 via is placed in this

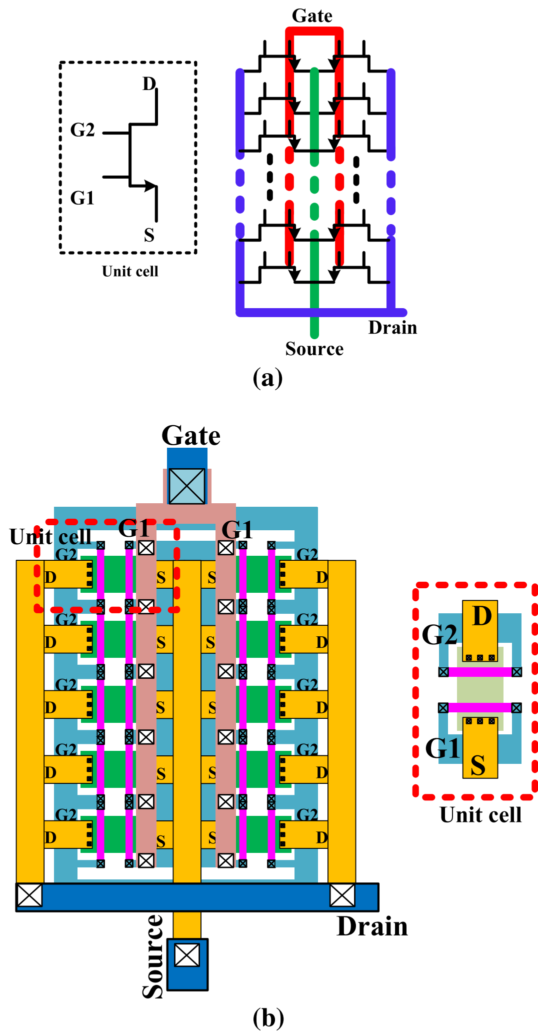


Fig. 3 Multi-gate device schematic and layout **a** single unit cell and multi-cell schematic, **b** layout of single cell and multiple cells

shared area of gate at M1. This increases the number of vias at gate terminal. Gate signal is routed at metal M5 from top of the structure and tapped to the gate contacts using these M1–M5 vias. A device schematic and layout schemes are shown in Fig. 3(b), which is composed of 20 unit cells in a tree configuration. Similarly, source connection of the cells are shared between two adjacent cells and routed from the middle of the cells towards bottom of the structure not crossing the gate wiring to minimize the gate-to-source capacitance. Drains of the cells are connected to metal M7 and routed from two sides of the structures to bottom of the structure. As it can be seen from Fig. 3(b), there are at least four times the number of M1-to-M5 vias compared to the structure in Fig. 2 to reduce $r_{via,ext}$. Similarly wiring resistance is halved by routing the gate signal at metal M5 in two parallel branches, which helps to reduce the r_{wire}. The layout presented in Fig. 3(b) is good for optimizing $r_{g,ext}$. However, due to the increased wiring at the drain terminals of the structure, c_{gd} is increased, which limits the f_{max} of the device. This is acceptable when f_{max} is not too close to the actual operation frequency.

3 mmWave design techniques

3.1 RF ground for inductors and transformers

EM modelling techniques are used in order to accurately include the behavior of a multi-layer passive device and its associated RF ground in the overall device performance. A low impedance ground plane for passive devices is very important in mmWave integrated circuit designs to provide seamless path for high frequency return currents. Definition of an RF ground is essential for ground reference of the excitation ports. Two possible ground plane definitions are shown in Fig. 4. Bottom side of the substrate can be used as RF ground (Fig. 4(a)) that requires solid connections (through-hole via) from top metal layer through substrate [10] because external ground connections to chip are only possible through metal bond pads. However, manufacturing of these vias are expensive and require extra

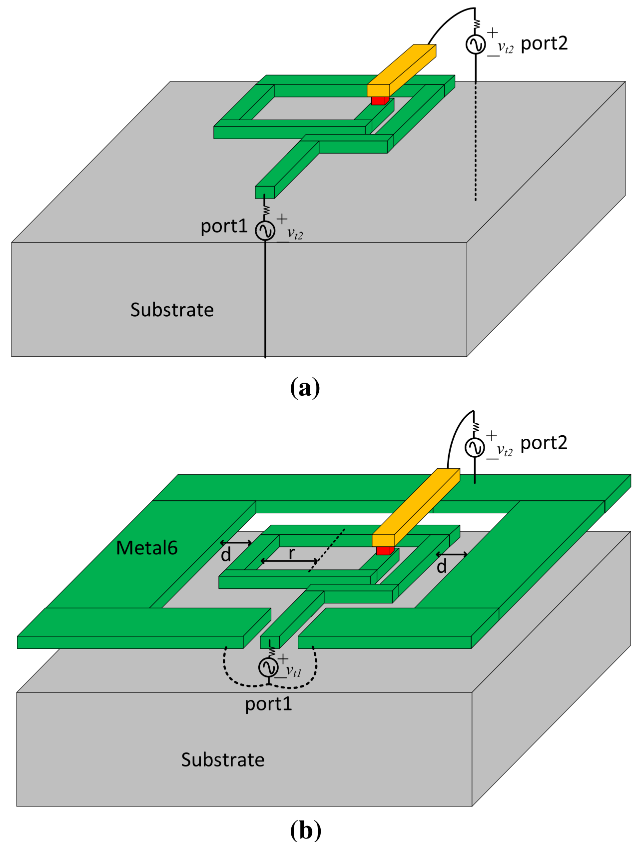


Fig. 4 Port difinition, **a** port reference from the bottom of the substrate, **b** port reference from local ground plane

manufacturing processing [11]. Moreover, eddy currents can be induced in this solid metal plate resulting in substantial loss in passive devices at mmWave frequencies. Contrarily, a local ground plane can be used as an RF ground reference which provides local reference for the excitation ports as shown in Fig. 4(b). Generally, a ground plane is composed of thick metal layer from the available metal stack of the technology due to their lower sheet resistance. Alternatively, multiple metal layers are stacked together to realize low impedance metal ground plane.

In bulk CMOS process, low resistive substrate requires metal ring (guard ring) connected with the metal ground plane around active and passive devices in order to offer low ohmic paths for currents induced from substrate coupling to reduce cross talks between neighbouring devices. In such case, a wall of ground plane around passive devices consisting of all metal layers is used which offers additional benefits of isolation between neighbouring devices. However, in high-resistive substrates, e.g. CMOS SOI, substrate connections (guard ring) are not necessary around passive devices and therefore, a metal ground plane at top metal layer with enough current handling capability is sufficient as shown in Fig. 4(b).

External transistion of signal and ground connections from the chip to outside world, i.e. printed circuit board (PCB), are realized using bond pads made of top metal layer. These bond pads are then connected to PCB with the help of bond wires or solder balls. Parasitic inductance ($\sim$ 100 s of pH) and resistance associated with bond wires make them non-feasible for most of the mmWave applications. Contrarily, solder balls have very low parasitic inductance ($\sim$ 10 s of pH) [12] from the connections when connected in flip chip orientation as shown in Fig. 5(a). When designing the mmWave circuit blocks (passive or active), extracted models of these signal and ground transitions should be included in the simulations. An RF ground can also be defined outside the chip, i.e. PCB, considering the IC is connected on the PCB as flipped chip using solder balls as shown in Fig. 5(b). In such case, top PCB layer (RF ground) interfacing with IC should be part of the EM simulations. This type of RF ground has minimum transition between PCB and IC and represents more realistic simulation environment towards real implementation.

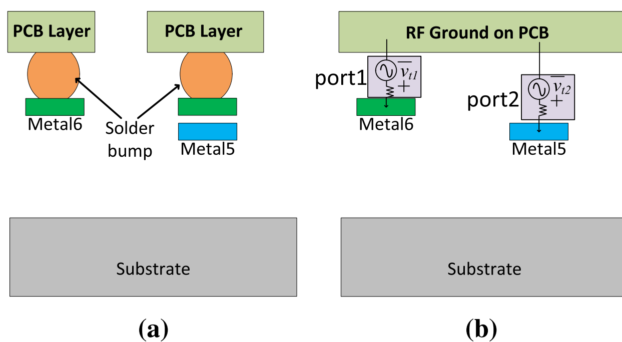


Fig. 5 Definition of ground reference in passive design

3.2 Return currents

Depending on the definition of the RF ground, an excitation current from a port finds multiple return paths as shown in Fig. 6 [13]. All these paths have finite impedance (resistance and inductance) and their lengths are different from each other. The final inductance and quality factor of the inductor highly depends on the impedance of these paths and their characteristics, e.g. inductance, resistance, length of the path, etc. For example, the current i_{t1} from source v_{t1} (port 1) travels towards output source v_{t2} (considering port2 is shorted to ground) through the inductor and it takes 4 different return paths to reach back to its source v_{t1}. Currents i_{r1} and i_{r2} travels through ground plane by passing through voltage source v_{t2}. Ground plane is capacitively coupled with the inductor conductor, due to which electric currents (i_{r3} and i_{r4}) are induced in the ground plane. Intensity of these currents and coupling depends on the distance (d) between the inductor and ground plane. Another current i_{r5} is induced in the substrate from capacitive coupling from inductor and the substrate under the structure and it flows through the substrate and into the global ground plane through the nearest via from substrate to metal ground plane. Magnitude of this current depends on substrate characteristics, i.e. high-resistive substrate substantially reduces this current due to high resistance and reduced electric coupling compared to low-ohmic substrates. All these currents see different impedance when travelling through their respective medium. The effects of these return currents and their dependency on distance d can be observed from Fig. 7. An inductor is simulated with a ground plane around it for different values of d (with

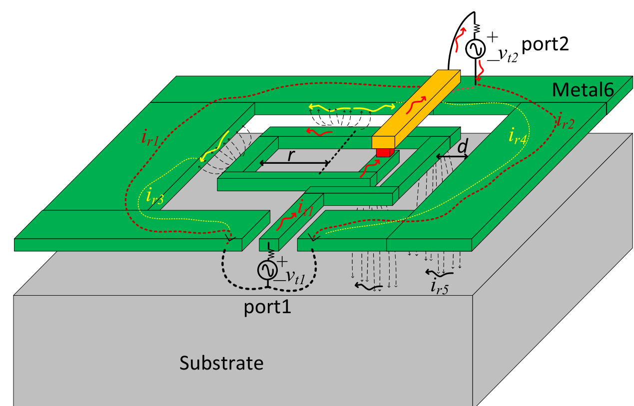


Fig. 6 Visualization of return currents of an inductor implemented with ground ring

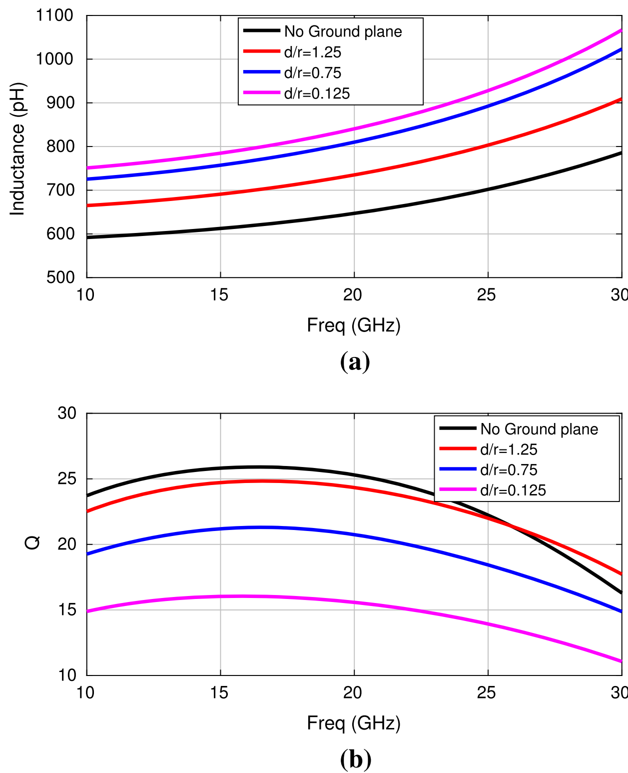


Fig. 7 **a** Inductance and **b** quality factor of an inductor with ground plane for different *d*/*r* ratios

fixed radius r). It can be noticed that effect of the ground plane on L and Q start increasing when d becomes smaller than r (i.e. $d/r < 1$). When d is greater than r (i.e. $d/r > 1$), the effect of ground plane is negligibly small compared to the case with no ground plane. From this example, it can be deduced that a ground plane has almost no effect when its distance from coil is greater than its radius.

3.3 Applying transformers in mmWave IC designs

In narrow band amplifier designs, a parallel LC based resonator is utilized which offers cancellation of capacitive reactance of the transistor at its output ($C_{parasitic}$) which results in maximum gain from the transistor at resonance frequency of the resonator. Losses in the resonator elements (quality factor), i.e. inductor (L) and capacitor (C), limit this gain. These losses increase significantly at mmWave frequencies due to associated parasitic effects, e.g. skin effect, eddy current, capacitive coupling with neighbouring structures, etc. Quality factor of inductors (Q_L) can be improved by custom made design and optimized layout techniques. However, quality factor of capacitors (Q_C) degrades with the increase in their area. Therefore, big capacitors should be avoided in the resonators at mmWave frequency operations. In order to design an amplifier covering a broad range of frequencies, a higher-order resonator design is required which occupies large silicon area when using lumped elements. A cascaded design approach consisting of multiple narrowband stages can also be utilized to cover wideband frequency range [14]. Contrarily, transformers inherit the properties of high-order resonator design with comparatively compact layout area. A generic schematic of a transformer is shown in Fig. 8(a). It has an additional mutual inductance associated with the mutual coupling (k) between its primary (L_P) and secondary L_S windings. Transformers are frequently used for mmWave designs due to their several benefits, e.g. compact area, seamless signal routing, balancing/unbalancing (balun), AC coupling, impedance transformation, etc. Moreover, a transformer can also be used in narrowband operations. A transformer-based LC resonator in Fig. 8(b) produces resonances at two different frequencies which can be calculated as

$$\omega_L = \frac{1}{\sqrt{LC(1+|k|}},\quad \omega_H = \frac{1}{\sqrt{LC(1-|k|}},\quad |k| = \frac{\omega_H^2+\omega_L^2}{\omega_H^2-\omega_L^2}, \tag{3}$$

where ω_L and ω_H are lower and higher resonance frequencies, respectively. It can be observed from Eq. 3, that separation between ω_L and ω_H can be controlled with k. Simulated magnitude of impedance of this resonator is shown in Fig. 9 with different values of k. It can be seen that for lower k, the two resonances come closer to each other. This feature is useful for wideband amplifier designs as in [15] and [3]. However, when the k is increased separation between two resonances starts to increase which is a suitable criteria for narrowband amplifier designs. In such case, only one resonance frequency (for example, ω_L) is used. Different types of layout techniques are used to achieve the desired coupling, for example, interleaved layout design (horizontal coupling) and multi-layer design (for vertical coupling) [16]. The design of the transformer layout highly depends on the available metal layers and

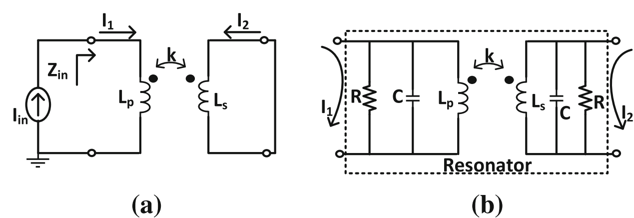


Fig. 8 **a** Transformer schematic, **b** transformer-based resonator

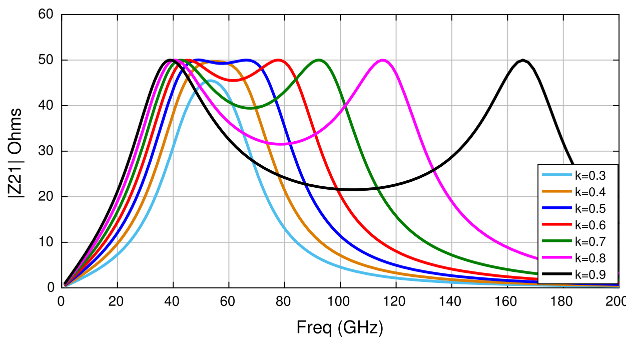


Fig. 9 Impedance of a transformer with varying coupling

their respective properties (i.e. thickness, sheet resistance, etc.).

4 LNA design

In order to optimize the input noise of the LNA towards minimum noise figure (NF_{min}), two main factors are considered, i.e. optimum noise match and minimizing the intrinsic and extrinsic gate resistance. Intrinsic gate resistance is optimized by optimizing the number of gate fingers and by increasing the poly to M1 contacts of the gate fingers. Extrinsic gate resistance is reduced by optimizing the transition of gate from M1 to higher metal layers increasing the number of M1 to M5 vias. Proposed multi-gate technique of cascode device layout as discussed in Sect. 2 helps to reduce the wiring resistance at the gate terminal and can be useful for low noise amplifier designs.

An inductively degenerated common source cascode LNA is designed using multigate layout technique. The proposed LNA is fabricated using 45 nm CMOS SOI technology at center frequency of 40 GHz. Schematics of the designed LNA is shown in Fig. 10. A unit cell of cascode connected devices is designed first and then a bigger device is designed based on these unit cells. In addition to the fast active devices, high quality factor passive structures play a key role in mmWave frequency designs. CMOS SOI technology provides not only benefits of reduced parasitics, higher f_{max} for active devices, but also offers high resistive substrate that allows the design of low loss passive structures. Presumably, CMOS SOI technology is being considered as an attractive choice for future mmWave integrated system designs. Moreover, availability of two thick metal layers in metal stack offers additional design freedom towards low-ohmic passive structures, such as inductors, transmission lines, transformers and various interconnects.

In this design, a narrowband input matching approach is used. Source inductance is realized by coplanar waveguide (CPW) transmission line, and a custom inductor is used for gate inductance. Layout of the gate inductor is similar to Fig. 6. CPW transmission line (TL) is designed using thick copper layer of M8. Since the required degeneration inductance is small, use of CPW TL provides benefits of lower inductance with compact area integration.

A one turn transformer with high k is used to resonate the capacitance at the drain of the cascode devices. Vertical coupling between the primary and secondary coils is achieved by stacking the M6 and M7 as shown in Fig. 11. Transformer was designed for maximum coupling ($k\sim0.84$) that produces two resonances separated far from each other and only the lower resonance at 40 GHz is used (also shown in Fig. 9, black trace). Ground reference port definition strategy discussed in Sect. 3, is used for EM simulations of the passive structures. Transformer is also performing balun function, providing differential signal at the output of the first stage. An output differential buffer with the similar transformer load is used as the second stage of the LNA.

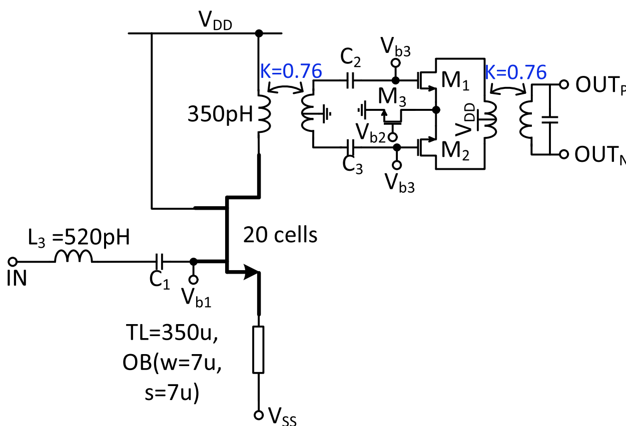


Fig. 10 Schematic of the LNA

5 Measurement results

In order to make a comparison of multi-gate cascode device with conventional style layout, two separate structures are fabricated using 45 nm CMOS SOI technology. The first device is using conventional style layout, and the second device utilizes multi-gate technique. Schematic of the measurement configurations and die micrographs of

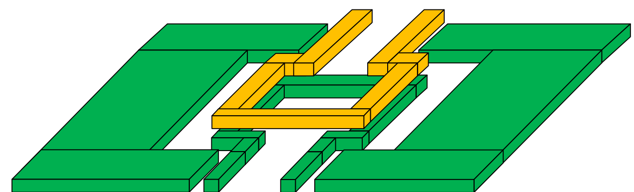


Fig. 11 3D layout view of a 1 turn transformer with lateral coupling

both structures are shown in Fig. 12. S-parameter measurements are performed from 30 to 50 GHz frequency range, using Keysight 67 GHz PNA. GSG pads and probes are used to measure the s-parameters at the input and output. Two port calibration is performed up to the probe tip using external through-reflect-load (TRL) standards on a separate calibration substrate. DC biasing for gate and drain of the structures are provided using bias-T from external sources. However, biasing of cascoded transistors are provided from on-chip power supply (VDD = 1 V) with enough decoupling capacitors. Measurement results include the input and output pads and extended transmission lines up to the device terminals.

Gate resistance of the structures are extracted from the measured s-parameters (at fixed bias voltage of 580 mV) using real part of h_{11} as also used in [9] and plotted in Fig. 13.

$$r_g = Re(h_{11}) \tag{4}$$

Gate capacitance (C_{gs} and C_{gd}) and transconductance (g_m) are extracted using following equations [17],

$$C_{gs} = \frac{Im(y_{11} + y_{12})}{\omega}$$
$$C_{gd} = -\frac{Im(y_{12})}{\omega} \tag{5}$$
$$g_m = Re(y_{21})$$

Extracted gate resistance of the multi-gate layout technique is 10% lower than the conventional layout style. However, due to the increased wiring of the multi-gate technique, gate to source (C_{gs}) and gate-to-drain capacitance (C_{gd}) are 4% and 40% higher than in the conventional layout, as shown in Fig. 14. There is roughly no change in the transconductance of both structures, as shown in Fig. 15. Due to the increase in C_{gg}, f_{max} of multi-gate device is 20% lower than the conventional layout as shown in Fig. 16. However, this is still sufficient for targeted frequency bands. Since the detailed modelling for multigate devices differs from the conventional transistors, measurements instead of simulations are used for comparison between two structures. Table 2 shows comparison results of extracted parameters at 40 GHz for the two structures (Fig. 12).

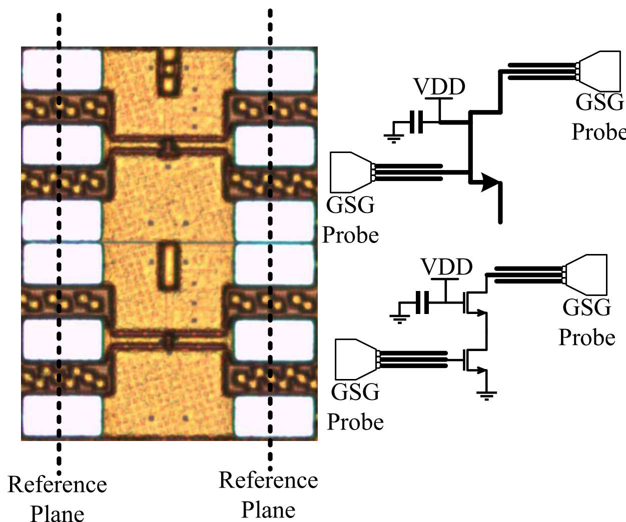


Fig. 12 Die micrographs of cascode structures and respective schematics

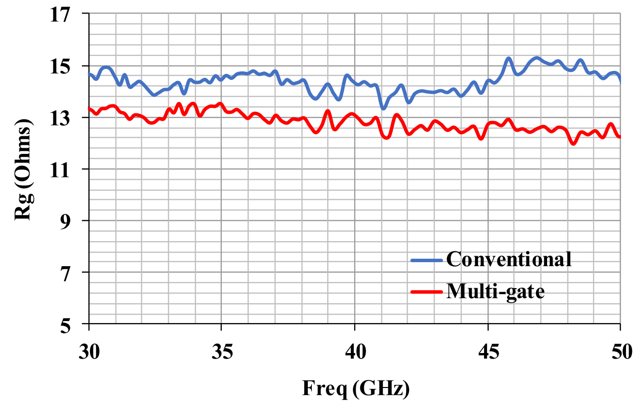


Fig. 13 Extracted R_g of two structures (VDD = 1 V, V_{bias} = 580 mV)

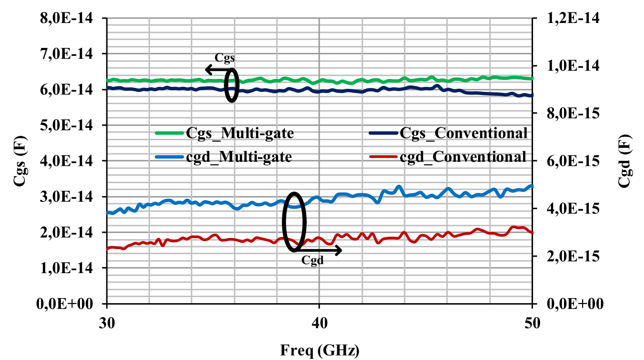


Fig. 14 Extracted capacitances, C_{gs} and C_{gd} of two structures, (VDD = 1 V, V_{bias} = 580 mV)

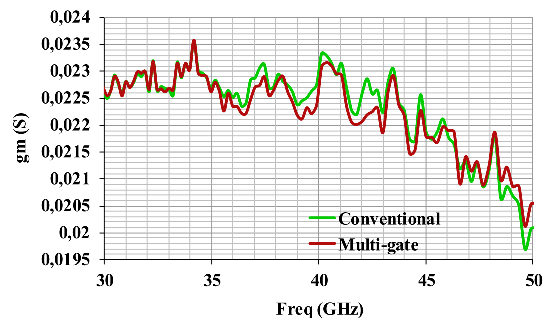


Fig. 15 Extracted g_m of two structures, (VDD = 1 V, V_{bias} = 580 mV)

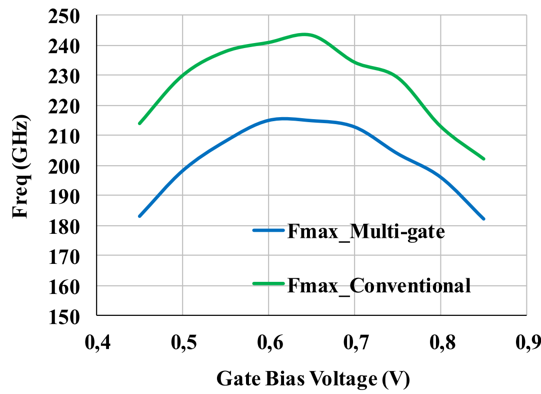


Fig. 16 Extracted f_{max} versus V_{bias} of two structures

A single-ended input, differential output LNA is fabricated using GlobalFoundries 45 nm CMOS SOI technology. Die micrograph of LNA is shown in Fig. 17, core area including input and output pads is $1061 \times 0.349\,\text{mm}^2$. Although, it is better to compare the layout effects of two styles on the noise performance of an LNA. However, this was not possible due to the limited available resources for chip fabrication. GSG probes are used to perform on wafer measurements. LNA is measured from a single-ended input to a single-ended output because of the non availability of single-to-differential probe calibration. S-parameters of the LNA are measured using Keysight 67 GHz PNA. Noise figure measurements are performed using 50 GHz noise source, 50 GHz spectrum analyzer and pre-amplifier provided by Keysight technologies. Calibration of the noise figure measurement setup is performed using on-chip through standard. Biasing of the active blocks is implemented using local current mirrors which take 100 µm current from off-chip external source using bondwire connections. Biasing voltage is controlled using on-chip integrated shift register logic. Supply voltage is also routed from external supply using bondwire connections with sufficient supply de-coupling capacitance placed on- and off-chip. Measured and simulated s-parameters and noise figure results for dual-gate LNA are shown in Fig. 18(a, b), respectively. Measured S21 gain is 10.2 dB at 40 GHz. Measured input (S11) and output (S22) reflection coefficient are below − 10 dB at 40 GHz. Noise figure is 4.3 dB at 40 GHz. Table 3 shows a brief performance comparison of the LNA with existing state-of-the-art (SOA) designs at 40 GHz. Measured (and simulated) gain of the LNA is around 3 dB lower because it was measured (and simulated) from single-ended output only. It shows that LNA is having much lower power consumption with the LNA's of similar performance.

Table 2 Comparison table of extracted parameter values at 40 GHz (VDD = 1 V, V_{bias} = 580 mV)

Parameters	Conventional	Multigate
R_g (Ω)	14.3	12.9
C_{gs} (fF)	60	62
C_{gd} (fF)	2.77	4.33
g_m (mS)	22.5	22.5
f_{max} (GHz)	243	215

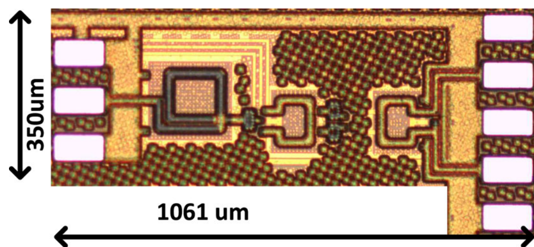
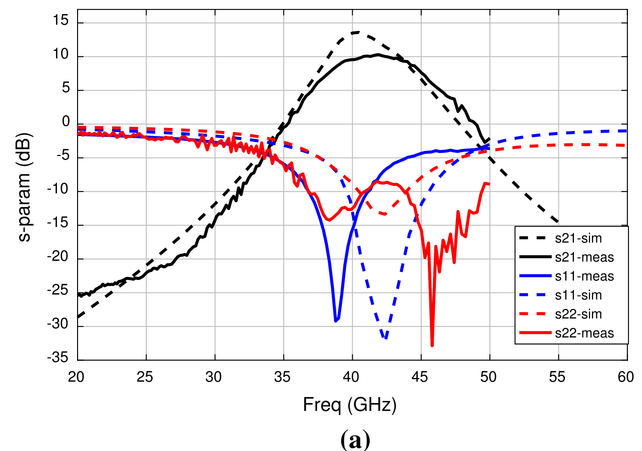


Fig. 17 Micrograph of the LNA



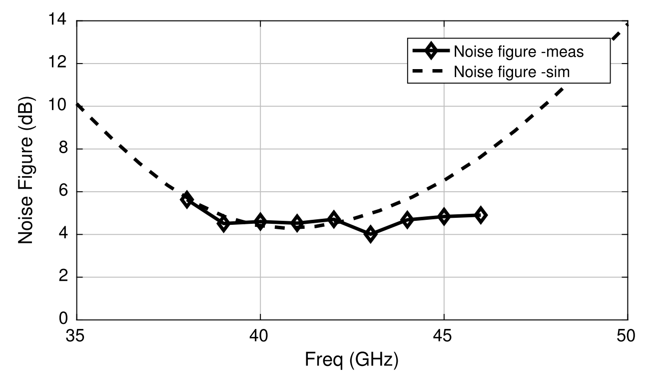


Fig. 18 Measured s-parameters of LNA

Table 3 Perfomrance comparison of LNA with existing SOA LNAs

Technology	This work 45 nm SOI	[18] 130 nm CMOS	[19] 90 nm CMOS	[20] 65 nm CMOS	[21] 90 nm SOI
Freq (GHz)	40	38	37	42	26–42
Max. gain (dB)	10.2	12.6	13.8	14.3	11.9
NF (dB)	4.2	4	3.8	6	4.2
P_{diss} (mW)	13	24	18	43.2	40.8
P_{1dB} (dBm)	− 11	N/A	N/A	N/A	N/A
Chip area (mm^2)	0.31	0.252	0.48	0.286	0.18

6 Conclusion

This work introduces layout optimization techniques of cascode connected transistors and a design of an LNA for mmWave applications. A multi-gate layout technique is compared to a conventional layout style. Optimization of intrinsic and extrinsic parasitic components for both cascode devices is discussed. Design techniques of silicon based passive structures for mmWave applications are discussed and optimization of ground connection presented. An overview was given for setting up the ground reference for port definition in EM simulation tools. Design of a 40 GHz LNA using multi-gate cascode device is also presented including key results from fabricated sample. A multi-gate layout reduces gate resistance while conventional layout reduces wiring capacitance. It is compared against cascode LNA's. The device is designed and fabricated using 45 nm CMOS SOI technology. Measurement results show a reduction of 10% in gate resistance of multi-gate layout technique compared to the conventional double contacted gate approach. However, gate-to-source and gate-to-drain capacitances are degraded by 4% and 36%, respectively, which limits the maximum speed of the input stage. Therefore, this comparison concludes that there is a trade-off in optimization between r_g and f_{max} of the cascode devices in layout designs. Measured results of LNA achieve a peak gain of 10.2 dB and noise figure of 4.2 dB at 40 GHz.

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