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GUEST EDITORIAL

Special issue: selected papers from the 1st NORCAS conference (2015 Nordic Circuits and Systems Conference (NORCAS): NORCHIP and International Symposium on System-on-Chip (SoC))

Snorre Aunet[1] · Jim Torresen[1]

This special issue includes selected papers from the 1st NORCAS Conference held in Oslo, Norway, October 26–28, 2015. The new conference emerged from a merger between the former Norchip and International Symposium on System-on-Chip conferences.

The conference covers all fields of electronics design, spanning from complex digital systems to advanced analog and mixed-mode circuits. The wide scope of the conference promotes cross-field collaboration not only between academics but also with industry. Papers of high scientific and technical quality are presented together with tutorials and talks from selected invited speakers.

All analog related papers scoring above a certain threshold after NORCAS reviews were selected for potential inclusion in this special issue of the Analog Integrated Circuits and Signal Processing. 8 manuscripts based on NORCAS contributions have been included, after regular, new, peer reviews. 101 manuscripts were submitted for review, and 68 accepted for presentation at the conference. Among the analog papers, themes cover aspects including amplifiers, DC–DC converters, oscillators, PLLs, matching networks for SC circuits and ADCs.

We hope that the papers in this special issue covering analog topics from NORCAS make interesting reading. A brief introduction to the selected papers follows:

"A Continous-Time Delta-Sigma ADC with Integrated Digital Background Calibration" was written by Siyu Tan, Yun Miao, Mattias Palm, Joachim Neves Rodrigues and Pietro Andreani from University of Lund and Ericsson Research (M. Palm). It presents a digital calibration technique for use in continuous time (CT) Delta-Sigma analog-to-digital converters (ADCs). The calibration improves SNDR by 13.5 dB, and the associated digital circuitry has a power consumption of 1.2 mW from a total of 6.2 mW for the system. Simulations based on layout, in 65 nm CMOS, leads to a maximum signal-to-noise and distortion ratio (SNDR) of 67.1 dB within 9 MHz bandwidth, for a clock frequency of 144 MHz.

The paper titled "Design and validation of a 10-bit current mode SAR ADC with 58.4 dB SFDR at 50 MS/s in 90 nm CMOS" was written by Abdelrahman Elkafrawy, Jens Anders and Maurits Ortmanns, all from the University of Ulm, Germany. Included in the concept is a Gm stage which converts the input voltage to a current which is then processed in a current based binary search algorithm SAR loop. To validate the proposed approach, a prototype 10-bit ADC was fabricated in a 90 nm TSMC CMOS process. Measured results for the ADC show an SFDR of 58.4 dB at 50 MS/s, while consuming 6 mW from a 1.2/1.8 V supply.

"High-efficiency peak-current-control non-inverting buck–boost converter using mode selection for single Ni–MH cell battery operation" is a manuscript from Jong-Seok Kim, Jin-O Yoon, Jaeyun Lee and Byong-deok Choi, all from Hanyang University in South Korea. They have implemented a non-inverting buck-boost converter in 180 nm CMOS, demonstrating enhancements from a conventional design, by chip measurements. The converter intended for use with a Ni–MH cell battery has a selection circuit that can put the circuit in buck, boost, or buck-boost modes, which is used to extend the battery lifetime.

"Analysis and design of power and efficiency in third-order matching networks for switched-capacitor power-amplifiers" is written by Antonio Passamani, Davide Ponton and Gerhard Knoblinger from Intel Mobile Communications in Austria, plus Andrea Bevilacqua from the

✉ Snorre Aunet
snorre.aunet@iet.ntnu.no

[1] University of Oslo, Oslo, Norway

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University of Pavia, Italy. They present a third-order matching network exploiting the intrinsic output capacitance of a switched capacitor power amplifier, leading to a relatively low number of passive components. An implementation in 28 nm CMOS, having a Bluetooth application in mind, was performed. Further structures have been implemented and characterized by chip measurements, covering additional applications.

"Analysis and Design of Class-O RF Power Amplifiers for Wireless Communication Systems" discusses analysis and design of power amplifiers recently called class-O. The authors, from Aachen University, are Muhammad Abdullah Khan, Ahmed F. Aref, Mohsin M. Tarar and Renato Negra. The authors state that class-O amplifiers offer improvements with respect to the design of power amplifiers constrained by linearity, efficiency and reliability. The paper presents a 706 MHz class-O RF power amplifier for handheld wireless applications. The amplifier has been implemented in 130 nm CMOS technology, and measurements from silicon are provided.

"A compact broadband stacked medium power amplifier in standard 65 nm CMOS technology" is authored by Mohsin Tarar, Muh-Dey Wei, Muhammad Abdul Khan and Renato Negra (Aachen University). The paper describes the design and implementation of a fully integrated broadband stacked power amplifier implemented in 65 nm CMOS. The amplifier topology utilizes three NMOS stacks and three PMOS stacks at the output, primarily to increase output impedance along with the output voltage swing. Chip measurements are provided.

"A wide band fractional-N digital PLL with a noise shaping 2-D time to digital converter for LTE-A applications" has Ahmed Mahmoud, Pietro Andreani and Ping Lu as authors. They come from Lund University and Silicon Labs (Lu). The wide band fractional-N PLL makes use of a Vernier time-to-digital converter where noise shaping reduces in-band phase noise. A class-D digitally controlled oscillator and noise cancellation are also included in the circuitry. Simulated results in a 65 nm CMOS process are included.

"Ultra low-power, -area and -frequency CMOS thyristor based oscillator for autonomous microsystems", contains a contribution from Dominic A. Funke, Pierre Mayr, Thomas Maeke, Johns Simpson McCaskill, Abhishek Sharma, Lukas Straczek and Jürgen Oehm, all from Ruhr University, Bochum. A thyristor based CMOS oscillator providing a clock signal of about 20 Hz, measuring 18 μm by 35 μm, is presented, being able to run more than 10 min from a 10 nF capacitor. Leakage currents and MOS capacitance are defining the time constant. Power consumption in 180 nm CMOS is 3 pW for a supply voltage of 200 mV, demonstrated by chip measurements.

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Snorre Aunet holds a Cand. Scient. degree in informatics from the University of Oslo, Norway, and a Dr. Ing. degree from the Norwegian University of Science and Technology, where he is a professor. From 2015 to 2016 he was at a sabbatical at University of California, San Diego. His research interests include mixed signal ultra low voltage/low energy integrated circuits. http://www.ntnu.edu/employees/aunet.

Jim Torresen is a Professor in computer science at the University of Oslo, Norway. He holds a Dr. Ing. (Ph.D.) degree from the Norwegian University of Science and Technology (1996). His research interests include nature-inspired computing, adaptive systems, reconfigurable hardware, robotics and applying this to complex real-world applications. More information and contact info: http://home.ifi.uio.no/~jimtoer.