

# Multiple soft fault diagnosis of DC analog CMOS circuits designed in nanometer technology

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Received: 3 November 2015/Revised: 11 February 2016/Accepted: 21 April 2016/Published online: 6 May 2016  
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**Abstract** This paper is devoted to local multiple soft fault diagnosis of nonlinear DC analog CMOS circuits designed in nanometer technology. An algorithm is developed that allows estimating the values of a set of potentially faulty process parameters. It exploits two tests with the input nodes accessible for excitation and the output node accessible for measurement. One of the tests is used to find the parameter values. It leads to a system of nonlinear algebraic type equations that are not given in explicit analytical form and may be satisfied by several sets of the parameter values. To solve the system of the equations the Nelder–Mead optimization method is applied with the objective function properly modified during the computation process. Next the obtained solution, being a set of the parameter values, is validated using the other test. If the solution passes this test it is considered as the actual one. Otherwise, another solution is calculated and verified using the same approach. The developed diagnostic procedure has been implemented in DELPHI, whereas the required by the algorithm circuit analyses are performed using IsSPICE 4 and both environments have been joined together. For illustration three numerical examples are given.

**Keywords** Analog nonlinear circuits · Fault diagnosis · Multiple soft faults · Nanometer technology · Nelder–Mead method

## 1 Introduction

Fault diagnosis of analog circuits is an important problem in the design and testing of electronic devices [1–22]. Generally, fault diagnosis includes detecting faulty circuits, locating faulty parameters and evaluating their values. If a faulty parameter is drifted from its tolerance range but does not lead to some topological changes, the fault is said to be soft or parametric. If a fault is open circuit or short circuit, it is called hard or catastrophic. In integrated circuits physical imperfections, such as near–opens or near–shorts may occur as spot defects [7, 10, 21, 22]. The methods dedicated to soft fault diagnosis usually exploit the simulation after test approach, where circuit simulations take place after any testing. They are based on measurements of the voltages at accessible points of the circuit, leading to equations with the tested parameters as unknown variables.

In current CMOS technology the global variations of parameters are measured by dedicated test structures included in the wafer. However, the problem is how to identify the random local variations of the process parameters. The local variations are due to fabrication or due to aging phenomenon. They affect the components across the die independently. Examples of local variations in ICs include local geometrical deformations, such as variations in the channel length and width, the oxide thickness, etc.

Many concepts and methods focused on parametric fault diagnosis are presented in references [1–3, 5, 9, 11, 13, 16–20]. Most of the works, dealing with soft fault diagnosis of analog circuits, address only the case when just one parameter is faulty. Fewer papers are devoted to the multiple fault diagnosis, where several parameters can be faulty. In real circuits the test equations, that express the measured voltages in terms of the parameters are nonlinear

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and cannot be presented in explicit analytical form. These equations may actually have multiple solutions, which means that several sets of the parameter values meet the test. To find the multiple solutions the parametric homotopy [17], the simplicial homotopy [18], or the block relaxation method [19] were proposed. To determine the actual solution a new efficient approach was proposed in Ref. [20] as follows. Two tests of the circuit are arranged, one used to find the solutions and the other to check if the obtained solution is the actual one. To compute the solution the extended systematic search method was developed [20]. In this paper the Nelder–Mead optimization method is applied with the objective function properly modified during the computation process and similarly as in [20] the obtained result is checked using the validation test. If the obtained solution passes this test the algorithm terminates, otherwise another solution is calculated and verified. The procedure is carried out as long as the solution which meets the validation test is obtained.

### 2 Diagnostic tests

Let us consider a nonlinear DC circuit, with  $n$  parameters  $x_1, \dots, x_n$  considered as potentially faulty, having one or more input nodes accessible for excitation and one output node accessible for measurement. We connect to the output node a resistor  $R_o$  and apply DC voltage sources to the input nodes (see Fig. 1). We choose  $n$  sets of the input voltage values and read the corresponding values of the output voltage. They are labelled  $v_o^{(1)}, \dots, v_o^{(n)}$  and used to form vector  $\mathbf{v}^{(o)} = [v_o^{(1)} \dots v_o^{(n)}]^T$ , where T means transposition. Each of the voltages is a function of the circuit parameters  $x_1, \dots, x_n, v_o^{(j)} = \tilde{g}_j(\mathbf{x})$ , where  $\mathbf{x} = [x_1 \dots x_n]^T$  is the vector consisting of the parameters considered as potentially faulty. Thus, it holds

$$\mathbf{v}^{(o)} = \tilde{\mathbf{g}}(\mathbf{x}), \tag{1}$$

where  $\tilde{\mathbf{g}}(\mathbf{x}) = [\tilde{g}_1(\mathbf{x}) \dots \tilde{g}_n(\mathbf{x})]^T$ . Equation (1) can be rewritten in the compact form

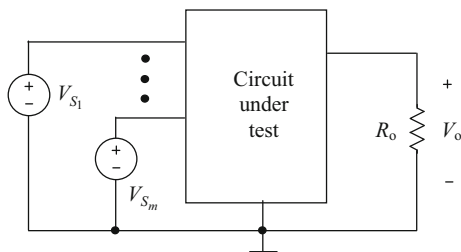


Fig. 1 Diagnostic test

$$\mathbf{g}(\mathbf{x}) = \mathbf{0}, \tag{2}$$

where  $\mathbf{g}(\mathbf{x}) = [g_1(\mathbf{x}) \dots g_n(\mathbf{x})]^T = \tilde{\mathbf{g}}(\mathbf{x}) - \mathbf{v}^{(o)}$ , and named a test equation.

The diagnostic method developed in Sect. 3 requires two tests arranged using the above–described approach. As a result the voltages  $\hat{v}_o^{(1)}, \dots, \hat{v}_o^{(n)}$  are measured in the circuit as depicted in Fig. 1, but driven by different sets of the input voltage sources, forming vector  $\hat{\mathbf{v}}^{(o)} = [\hat{v}_o^{(1)} \dots \hat{v}_o^{(n)}]^T$ . The first test leading to Eq. (2) will be named a principal test (PT), whereas the second one will be named a validation test (VT).

Unfortunately, in real electronic circuits the function  $\mathbf{g}(\mathbf{x})$  cannot be presented in explicit analytical form. However, the values of  $\tilde{g}_i(\mathbf{x})$   $i = 1, \dots, n$ , for given  $\mathbf{x}$ , can be found by performing the analyses of the circuits driven by the sources as in the test, with the parameters being the elements of vector  $\mathbf{x}$ .

### 3 Fault diagnosis algorithm

An algorithm that allows finding actual values of the parameters  $x_1, \dots, x_n$  is developed in this section. The algorithm solves the PT Eq. (2) and verifies the obtained solutions applying the VT. Its core is the Nelder–Mead optimization method [23–25]. The algorithm takes into consideration the possibility of existing several solutions of the nonlinear Eq. (2). Each of the solutions is a set of the parameters that meet the PT.

Since the algorithm exploits the Nelder–Mead method, a background of this method as well as the version that is used in this paper is described below. The Nelder–Mead method is designed to solve the unconstrained optimization problem of minimizing given nonlinear function  $f(\mathbf{x}) : R^n \rightarrow R$ . In this paper the method is adapted to solve Eq. (2). For this purpose the function

$$f(\mathbf{x}) = \sqrt{\alpha_1 g_1^2(\mathbf{x}) + \dots + \alpha_n g_n^2(\mathbf{x})} \tag{3}$$

is formed, where  $\alpha_1, \dots, \alpha_n$  are coefficients equal to zero or one. If all the coefficients are equal to one the function  $f(\mathbf{x})$  will be called a complete function, otherwise a reduced function. The complete function is identical to the Euclidean norm of  $\mathbf{g}(\mathbf{x})$ , i.e.,  $f(\mathbf{x}) = \|\mathbf{g}(\mathbf{x})\|_2$ . The Nelder–Mead method uses only the function values at some points in  $R^n$  and does not require gradients at the points. This is why this method is very useful to solve Eq. (2), with  $\mathbf{g}(\mathbf{x})$  not given in explicit analytical form. The Nelder–Mead method is simplex–based [23–25]. An  $m$ -simplex is a figure formed by  $m + 1$  independent points, written as  $S = \{\mathbf{x}^0, \dots, \mathbf{x}^m\}$ , where  $\mathbf{x}^i = [x_1^i \dots x_n^i]^T$ ,

$i = 0, 1, \dots, m$ , are called vertices. It is a convex hull of the  $m + 1$  independent points  $\mathbf{x}^i$  ( $i = 0, 1, \dots, m$ ). For example, 2-simplex is a triangle (see Fig. 2).

The method exploits simplices having  $n + 1$  vertices  $S = \{\mathbf{x}^0, \dots, \mathbf{x}^n\}$ . The corresponding function values at these vertices are labeled  $f^0 = f(\mathbf{x}^0), \dots, f^n = f(\mathbf{x}^n)$ . At any stage of the computation process the method generates a new simplex, aimed at decreasing the function values at its vertices. To construct this simplex one or more new points are searched comparing their function values with those at the vertices. Generally the method terminates when the simplex becomes sufficiently small, or the simplex is flat or degenerated [24]. The crucial point of the Nelder–Mead method is creating an adjusted simplex to the current simplex  $S$ . In this paper the approach described in [23] is adopted. Choose the indices  $h, s, l$ , of the worst, second worst, and the best vertex of  $S$  so that  $f^h = \max_i f^i, f^s = \max_{i \neq h} f^i, f^l = \min_i f^i$ . Calculate the centroid  $\mathbf{c}$  of the side opposite to the worst vertex  $h, \mathbf{c} = \frac{1}{n} \sum_{i \neq h} \mathbf{x}^i$  and find the reflection point  $\mathbf{x}^r = \mathbf{c} + (\mathbf{c} - \mathbf{x}^h)$  as well as  $f^r = f(\mathbf{x}^r)$  (see Fig. 3).

If  $f^l \leq f^r < f^s$  choose  $\mathbf{x}^r$  as the new vertex of the adjusted simplex. Otherwise, continue the procedure depending on whether  $f^r < f^l$  or  $f^r \geq f^s$ .

- If  $f^r < f^l$ , compute the point  $\mathbf{x}^e = \mathbf{c} + \gamma(\mathbf{x}^r - \mathbf{c})$  and  $f^e = f(\mathbf{x}^e)$ . If  $f^e < f^r$  choose  $\mathbf{x}^e$  as the new vertex, otherwise, choose  $\mathbf{x}^r$  as a new vertex.
- If  $f^r \geq f^s$ , compute a point  $\mathbf{x}^c$  using the following approach.
- If  $f^r < f^h$ , compute  $\mathbf{x}^c = \mathbf{c} + \beta(\mathbf{x}^r - \mathbf{c})$  and  $f^c = f(\mathbf{x}^c)$ . If  $f^c \leq f^r$ , choose  $\mathbf{x}^c$  as the vertex, otherwise, perform a shrink operation as described below.
- If  $f^r \geq f^h$ , compute  $\mathbf{x}^c = \mathbf{c} + \beta(\mathbf{x}^h - \mathbf{c})$  and  $f^c = f(\mathbf{x}^c)$ . If  $f^c \leq f^h$ , choose  $\mathbf{x}^c$  as the vertex. Otherwise, perform a shrink operation.

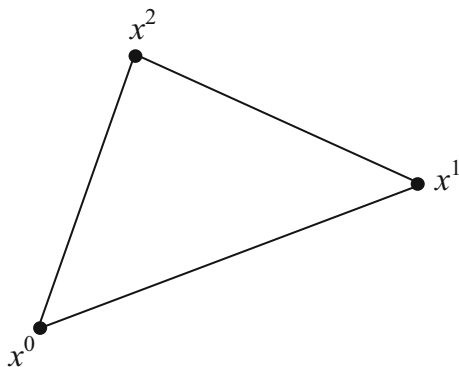


Fig. 2 Exemplary 2-simplex

Shrink operation: Compute  $n$  new vertices  $\mathbf{x}^i = \mathbf{x}^l + \delta(\mathbf{x}^i - \mathbf{x}^l)$ , for  $i = 0, \dots, n, i \neq l$ , (see Fig. 4).

### 3.1 Note

The coefficients  $\gamma, \beta, \delta$  are chosen as proposed in Ref. [25]:  $\gamma = 1 + \frac{2}{n}, \beta = 0.75 - \frac{1}{2n}, \delta = 1 - \frac{1}{n}$ .

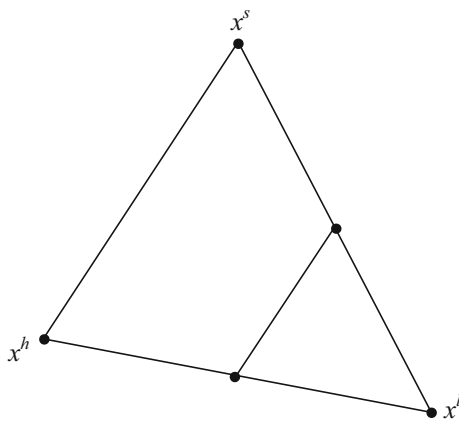
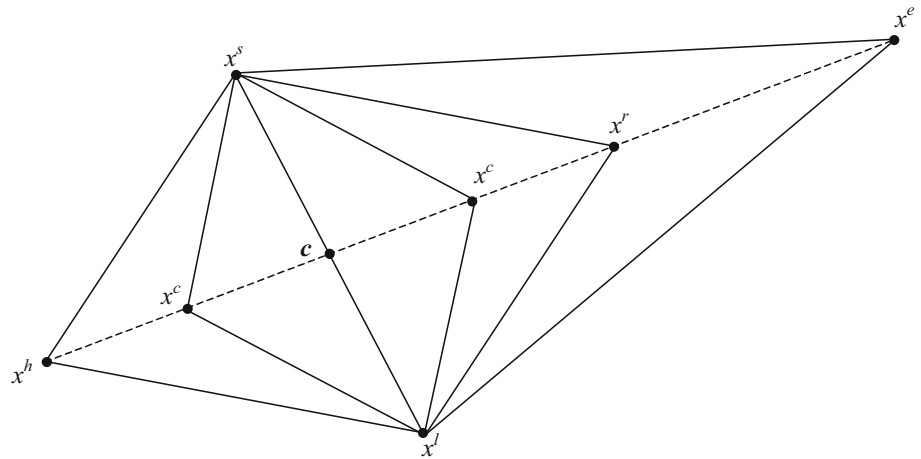
As the initial simplex we choose the regular one using the procedure described in Ref. [24].

It should be emphasized that the function  $f(\mathbf{x})$  is not given in explicit analytical form. In consequence, to find the value of the complete function  $f(\mathbf{x})$  at given  $\mathbf{x}, n$  analyses of the circuit must be performed applying the sources as in PT. This is time consuming process. The time is shrunk if  $f(\mathbf{x})$  is the reduced function. Since the Nelder–Mead method requires large number of the values of  $f(\mathbf{x})$  at various points  $\mathbf{x}$ , the reduced function is exploited at some stages of the algorithm proposed in this paper. Moreover, for different reduced functions the method searches for the solution (a set of the parameters) in different directions. This observation is used to find a new solution, when the obtained one does not pass the VT.

## 4 Sketch of the algorithm

1. Pick the required measurement accuracy of the voltages  $v_0^{(1)}, \dots, v_0^{(n)}$  and  $\hat{v}_0^{(1)}, \dots, \hat{v}_0^{(n)}$ , the tolerance  $\epsilon_1$  such that the inequality  $\|\mathbf{g}(\mathbf{x})\|_2 < \epsilon_1$  is a good approximation of  $\|\mathbf{g}(\mathbf{x})\|_2 = 0$ , the tolerance  $\epsilon_2$  used in Step 4, a maximum number of the generated simplices  $M$ , and the side  $a$  of the initial regular simplex.
2. Arrange two diagnostic tests, PT and VT, and form the vectors  $\mathbf{v}^{(0)}$  and  $\hat{\mathbf{v}}^{(0)}$  consisting of the measured voltages.
3. Create the reduced function  $f(\mathbf{x})$  specified by Eq. (3) with  $\alpha_1 = \dots = \alpha_{n-1} = 1, \alpha_n = 0$  and apply the Nelder–Mead method. If during the process a simplex is obtained so that the value of  $f(\mathbf{x})$  at the best vertex is  $< 100\epsilon_2$ , the computation process is modified as follows. The obtained  $\mathbf{x}$  is considered as an approximate solution. Next the complete function  $f(\mathbf{x})$  is created by setting  $\alpha_1 = \dots = \alpha_n = 1$ , a new regular simplex is constructed around this best vertex and the procedure is continued. If during the process a vertex, at which the value of  $f(\mathbf{x})$  is less than  $\epsilon_1$  appears, the parameters  $x_1, \dots, x_n$  corresponding to this vertex meet the PT. Otherwise, go to Step 5.
4. Check if the obtained parameters satisfy the VT. For this purpose analyse the circuit with these parameters, driven by the sources as in VT, find the voltages labelled  $\tilde{v}_0^{(1)}, \dots, \tilde{v}_0^{(n)}$  and form vector  $\mathbf{r} = [r_1 \dots r_n]^T$ , where  $r_j = \tilde{v}_0^{(j)} - \hat{v}_0^{(j)}, j = 1, \dots, n$ . If  $\|\mathbf{r}\|_2 =$

**Fig. 3** Basic simplex operations



**Fig. 4** Shrink operation

$\sqrt{r_1^2 + \dots + r_n^2} \leq \varepsilon_2$ , the parameters are the actual ones. In such a case the algorithm terminates. Otherwise, they are virtual and we proceed to Step 5.

5. Modify the function  $f(\mathbf{x})$  by setting  $\alpha_{n-1} = 0$ ,  $\alpha_1 = \dots = \alpha_{n-2} = \alpha_n = 1$  and repeat the steps 3–4 adapted to this case.

This procedure can be continued if the actual parameters have not been found, by setting in succession  $\alpha_{n-2} = 0, \dots, \alpha_1 = 0$ . In any case the remaining coefficients are equal to one and the number of the generated simplices cannot exceed maximum value  $M$ .

#### 4.1 Note

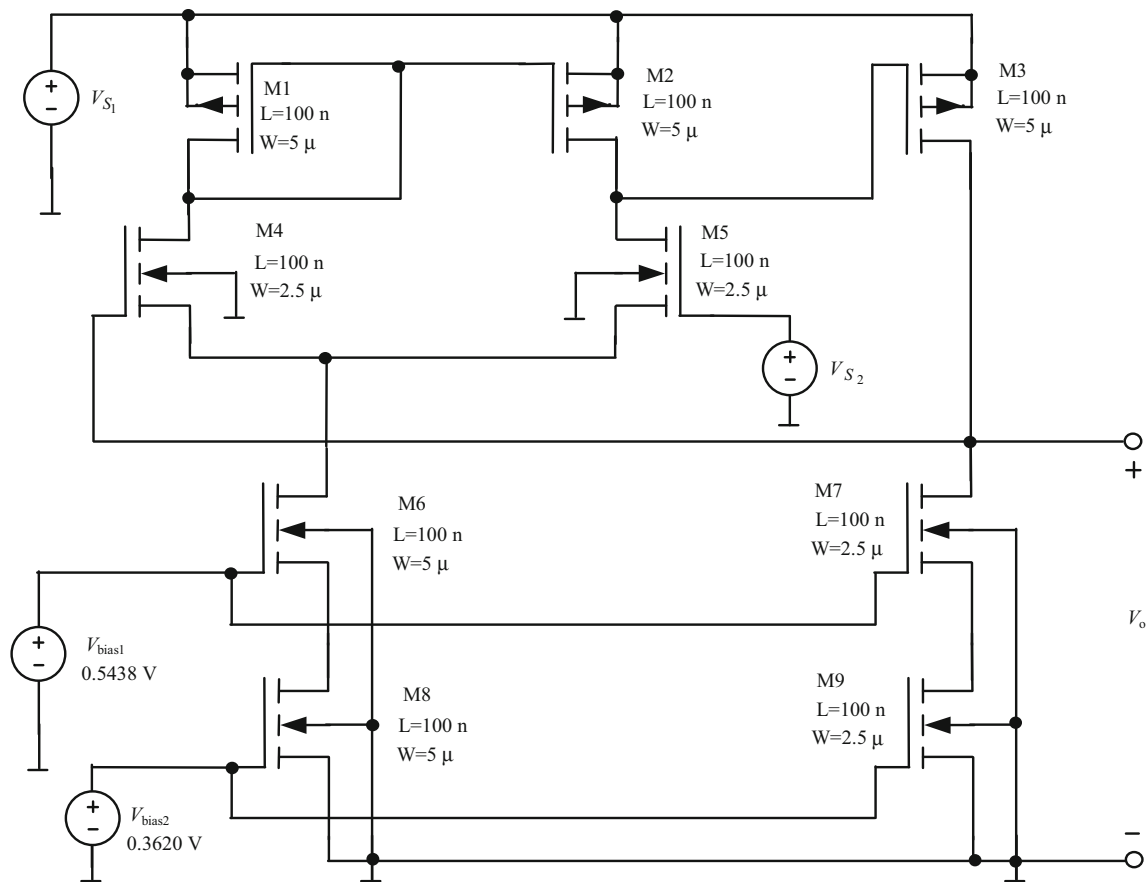
If at any stage of the algorithm the small or the flat simplex [24] appears, the set of the coefficients  $\alpha_1, \dots, \alpha_n$  is changed as described in step 5. If the degenerated simplex [24] appears, a new regular simplex is created around the best vertex of this simplex and the process is continued.

## 5 Numerical examples

The proposed algorithm has been implemented in the joined environments: DELPHI and IsSPICE 4, and tested numerically using MOS circuits designed in nanometer technology. The calculations were executed on PC with the processor Intel Core (TM) i7-2600. To illustrate effectiveness of the algorithm we consider three exemplary circuits designed in nanometer technology. In all the examples the transistors are characterized by the BSIM 4.6 model implemented in IsSPICE 4, Level 14 [26]. The nominal values of the channel lengths of the transistors are indicated in Figs. 5, 6 and 7, whereas the nominal values of the oxide thicknesses are  $(TOX)_p = (TOX)_n = 1.4$  nm. The other quantities are as follows:  $XL = 5$  nm,  $XW = 15$  nm. The discussed in this section soft faults are variations in the channel length  $\Delta L$  and in the oxide thickness  $\Delta TOX$ , considered separately for NMOS and PMOS transistors.

### 5.1 Example 1

Let us consider the bias two-stage op-amp shown in Fig. 5 [27]. To arrange the diagnostic tests (PT and VT) the input voltages  $V_{S_1}$  and  $V_{S_2}$  as well as the output voltage  $V_o$  are selected. It is assumed that the measurement accuracy of  $V_o$  is 1  $\mu$ V,  $M = 2000$ ,  $\varepsilon_1 = 10^{-6}$ ,  $\varepsilon_2 = 10^{-5}$ ,  $a = 0.05$ , the output resistance  $R_o = 10$  k $\Omega$ . At the preliminary stage of the diagnosis process the sensitivities of the voltage  $V_o$  due to variations of the parameters  $L$  and  $TOX$  of all the transistors, for different values  $V_{S_1}$  and  $V_{S_2}$ , are calculated. The analysis shows that the sensitivities of  $V_o$  due to the parameters of the transistors M6 and M7 are approximately 100 times smaller than due to the parameters of the other transistors. Thus, deviations of the parameters of transistors M6 and M7 have slight influence on the tested voltage  $V_o$  and they cannot be diagnosed in real conditions. In the



**Fig. 5** Bias two-stage operational amplifier

sequel we consider the soft faults of the following parameters:

- the channel lengths and the oxide thicknesses of PMOS transistors M1, M2, M3,
- the channel lengths and the oxide thicknesses of NMOS transistors M4, M5, M8, M9.

On the basis of sensitivity analyses and numerical experiments the following sets of the values of  $V_{S1}$  and  $V_{S2}$  have been chosen to perform of the PT and VT.

PT		VT	
$V_{S1} = 1.30 \text{ V}$	$V_{S2} = 1.25 \text{ V}$ ,	$V_{S1} = 1.20 \text{ V}$	$V_{S2} = 0.90 \text{ V}$ ,
$V_{S1} = 1.10 \text{ V}$	$V_{S2} = 0.95 \text{ V}$ ,	$V_{S1} = 0.90 \text{ V}$	$V_{S2} = 0.70 \text{ V}$ ,
$V_{S1} = 0.55 \text{ V}$	$V_{S2} = 0.50 \text{ V}$ ,	$V_{S1} = 0.70 \text{ V}$	$V_{S2} = 0.50 \text{ V}$ ,
$V_{S1} = 0.80 \text{ V}$	$V_{S2} = 0.65 \text{ V}$ ,	$V_{S1} = 0.60 \text{ V}$	$V_{S2} = 0.40 \text{ V}$ .

All the four sets are exploited to test the parameters of the four NMOS transistors M4, M5, M8, M9 and the first three of them are used to test the parameters of the three PMOS transistors M1, M2, M3.

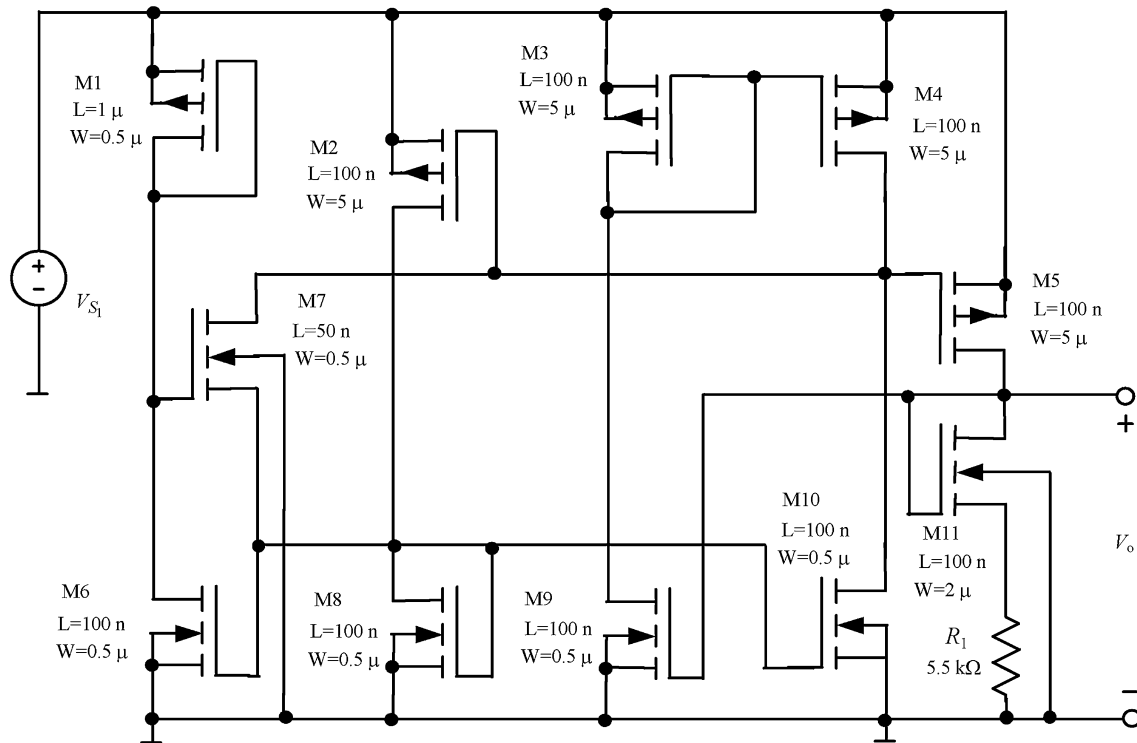
The results of different multiple soft fault diagnoses are summarized in Tables 1, 2, 3, 4. They comprise three sets

of the simultaneous variations of all the channel lengths in NMOS transistors M4, M5, M8, M9 (Table 1), and in PMOS transistors M1, M2, M3 (Table 2), three sets of the simultaneous variations of all the oxide thicknesses in NMOS transistors M4, M5, M8, M9 (Table 3) and in PMOS transistors M1, M2, M3 (Table 4). In all the cases the obtained values of the parameters are very close to their actual values.

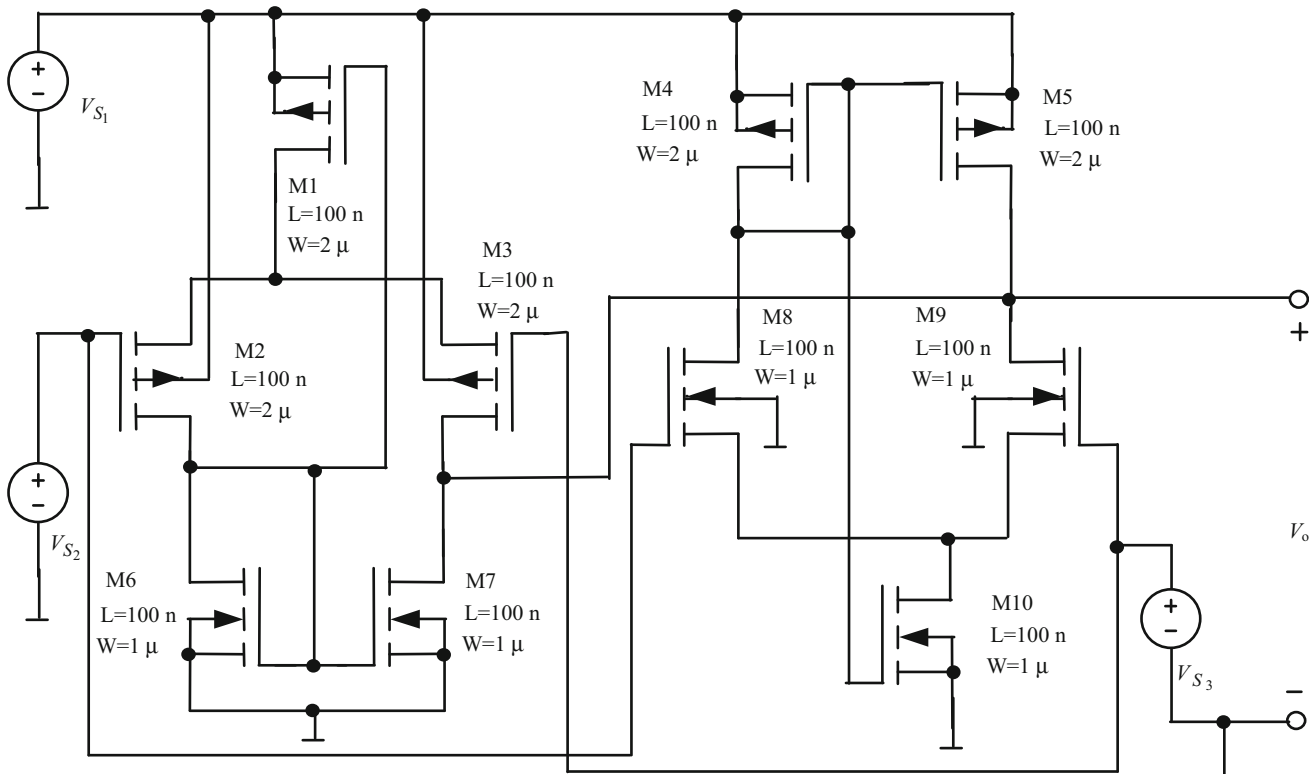
In this example the transistors M6 and M7 cannot be tested, because their parameters have very slight influence on the output voltage. Numerical experiments show that even in some idealized circumstances, under very high accuracy of the measurements of  $V_o$ , equal to  $0.01 \mu\text{V}$ , and  $M = 5000$  some determined parameters of these transistors can be erroneous and the CPU time long. Some exemplary results conforming this statement are included in Table 5.

### 5.2 Example 2

Figure 6 shows the CMOS circuit, being the voltage reference, designed in nanometer technology [27]. The measurement accuracy and the constants of the computation



**Fig. 6** Voltage reference circuit



**Fig. 7** A rail-to-rail input buffer

**Table 1** Results of the fault diagnosis of the channel lengths in NMOS transistors M4, M5, M8, M9

Actual values of the parameters	Values of the parameters determined by the method	Number of generated simplices	Computation time in seconds
$\Delta L_{M4} = 6.00$ nm	$\Delta L_{M4} = 6.02$ nm	191	59.8
$\Delta L_{M5} = 4.00$ nm	$\Delta L_{M5} = 4.02$ nm		
$\Delta L_{M8} = 2.50$ nm	$\Delta L_{M8} = 2.49$ nm		
$\Delta L_{M9} = 6.00$ nm	$\Delta L_{M9} = 5.97$ nm		
$\Delta L_{M4} = 15.00$ nm	$\Delta L_{M4} = 15.02$ nm	196	61.7
$\Delta L_{M5} = 2.00$ nm	$\Delta L_{M5} = 2.03$ nm		
$\Delta L_{M8} = 15.00$ nm	$\Delta L_{M8} = 15.00$ nm		
$\Delta L_{M9} = 4.50$ nm	$\Delta L_{M9} = 4.47$ nm		
$\Delta L_{M4} = 2.50$ nm	$\Delta L_{M4} = 2.55$ nm	742	227.5
$\Delta L_{M5} = 2.00$ nm	$\Delta L_{M5} = 2.06$ nm		
$\Delta L_{M8} = 1.75$ nm	$\Delta L_{M8} = 1.73$ nm		
$\Delta L_{M9} = 20.00$ nm	$\Delta L_{M9} = 19.90$ nm		

**Table 2** Results of the fault diagnosis of the channel lengths in PMOS transistors M1, M2, M3

Actual values of the parameters	Values of the parameters determined by the method	Number of generated simplices	Computation time in seconds
$\Delta L_{M1} = 4.50$ nm	$\Delta L_{M1} = 4.56$ nm	79	26.0
$\Delta L_{M2} = 3.00$ nm	$\Delta L_{M2} = 3.07$ nm		
$\Delta L_{M3} = 1.00$ nm	$\Delta L_{M3} = 1.00$ nm		
$\Delta L_{M1} = 15.00$ nm	$\Delta L_{M1} = 14.82$ nm	92	28.2
$\Delta L_{M2} = 10.00$ nm	$\Delta L_{M2} = 9.85$ nm		
$\Delta L_{M3} = 2.50$ nm	$\Delta L_{M3} = 2.50$ nm		
$\Delta L_{M1} = 1.50$ nm	$\Delta L_{M1} = 1.49$ nm	152	48.8
$\Delta L_{M2} = 25.00$ nm	$\Delta L_{M2} = 24.98$ nm		
$\Delta L_{M3} = 1.00$ nm	$\Delta L_{M3} = 1.00$ nm		

**Table 3** Results of the fault diagnosis of the oxide thicknesses in NMOS transistors M4, M5, M8, M9

Actual values of the parameters	Values of the parameters determined by the method	Number of generated simplices	Computation time in seconds
$\Delta TOX_{M4} = 140.0$ pm	$\Delta TOX_{M4} = 140.1$ pm	207	67.8
$\Delta TOX_{M5} = -56.0$ pm	$\Delta TOX_{M5} = -55.9$ pm		
$\Delta TOX_{M8} = -28.0$ pm	$\Delta TOX_{M8} = -27.8$ pm		
$\Delta TOX_{M9} = 98.0$ pm	$\Delta TOX_{M9} = 97.9$ pm		
$\Delta TOX_{M4} = 280.0$ pm	$\Delta TOX_{M4} = 280.1$ pm	346	106.9
$\Delta TOX_{M5} = -56.0$ pm	$\Delta TOX_{M5} = -55.9$ pm		
$\Delta TOX_{M8} = 280.0$ pm	$\Delta TOX_{M8} = 280.1$ pm		
$\Delta TOX_{M9} = -42.0$ pm	$\Delta TOX_{M9} = -42.0$ pm		
$\Delta TOX_{M4} = 70.0$ pm	$\Delta TOX_{M4} = 70.0$ pm	407	120.1
$\Delta TOX_{M5} = -56.0$ pm	$\Delta TOX_{M5} = -56.0$ pm		
$\Delta TOX_{M8} = -49.0$ pm	$\Delta TOX_{M8} = -49.0$ pm		
$\Delta TOX_{M9} = 560.0$ pm	$\Delta TOX_{M9} = 559.6$ pm		

**Table 4** Results of the fault diagnosis of the oxide thicknesses in PMOS transistors M1, M2, M3

Actual values of the parameters	Values of the parameters determined by the method	Number of generated simplices	Computation time in seconds
$\Delta TOX_{M1} = 112.0$ pm	$\Delta TOX_{M1} = 111.4$ pm	124	37.6
$\Delta TOX_{M2} = 56.0$ pm	$\Delta TOX_{M2} = 55.5$ pm		
$\Delta TOX_{M3} = -28.0$ pm	$\Delta TOX_{M3} = -28.0$ pm		
$\Delta TOX_{M1} = -42.0$ pm	$\Delta TOX_{M1} = -42.8$ pm	321	102.5
$\Delta TOX_{M2} = 420.0$ pm	$\Delta TOX_{M2} = 419.2$ pm		
$\Delta TOX_{M3} = 28.0$ pm	$\Delta TOX_{M3} = 28.0$ pm		
$\Delta TOX_{M1} = 280.0$ pm	$\Delta TOX_{M1} = 278.0$ pm	333	103.2
$\Delta TOX_{M2} = -70.0$ pm	$\Delta TOX_{M2} = -71.1$ pm		
$\Delta TOX_{M3} = 280.0$ pm	$\Delta TOX_{M3} = 280.0$ pm		

**Table 5** Results of the fault diagnosis of all NMOS transistors under the measurement accuracy  $0.01\mu\text{V}$ 

Actual values of the parameters	Values of the parameters determined by the method	Number of generated simplices	Computation time in seconds
$\Delta L_{M4} = 7.00$ nm	$\Delta L_{M4} = 7.00$ nm	2295	793.1
$\Delta L_{M5} = 7.00$ nm	$\Delta L_{M5} = 7.00$ nm		
$\Delta L_{M6} = 1.00$ nm	$\Delta L_{M6} = 0.92$ nm		
$\Delta L_{M7} = 2.80$ nm	$\Delta L_{M7} = 2.71$ nm		
$\Delta L_{M8} = 2.00$ nm	$\Delta L_{M8} = 2.00$ nm		
$\Delta L_{M9} = 4.00$ nm	$\Delta L_{M9} = 4.00$ nm		
$\Delta TOX_{M4} = 21.0$ pm	$\Delta TOX_{M4} = 21.0$ pm	1049	323.1
$\Delta TOX_{M5} = 280.0$ pm	$\Delta TOX_{M5} = 280.0$ pm		
$\Delta TOX_{M6} = -28.0$ pm	$\Delta TOX_{M6} = -28.2$ pm		
$\Delta TOX_{M7} = 70.0$ pm	$\Delta TOX_{M7} = 57.5$ pm		
$\Delta TOX_{M8} = -56.0$ pm	$\Delta TOX_{M8} = -56.0$ pm		
$\Delta TOX_{M9} = 42.0$ pm	$\Delta TOX_{M9} = 42.6$ pm		

process are the same as in Example 1. To arrange the diagnostic tests the input voltage  $V_{S1}$  and the output voltage  $V_o$  are selected. At the preliminary stage of the diagnosis process the sensitivities of the output voltage due to variations of the parameters  $L$  and  $TOX$  of all the transistors, for different values  $V_{S1}$ , are calculated. The analysis reveals that the sensitivities due to the parameters of the transistors M1, M2, M6, M7, and M8 are 100–100,000 times smaller than due to the parameters of the other transistors. Thus, they cannot be tested. This is why we perform the fault diagnosis of the parameters of transistors M3, M4, M5, M9, M10, and M11, separately for the PMOS (M3, M4, M5) and NMOS (M9, M10, M11) ones. On the basis of sensitivity analyses and numerical experiments the following values of  $V_{S1}$  have been chosen to perform of the PT and VT.

$$\begin{array}{ll} \text{PT} & \text{VT} \\ V_{S1} = 0.45 \text{ V}, & V_{S1} = 0.40 \text{ V}, \\ V_{S1} = 0.60 \text{ V}, & V_{S1} = 0.50 \text{ V}, \\ V_{S1} = 0.70 \text{ V}, & V_{S1} = 0.80 \text{ V}. \end{array}$$

The results of various multiple soft fault diagnoses are summarized in Tables 6, 7, 8, 9. They comprise three sets of the simultaneous variations of all the channel lengths in NMOS transistors (Table 6), in PMOS transistors (Table 7), and three sets of the simultaneous variations of all the oxide thicknesses in NMOS transistors (Table 8) and the PMOS transistors (Table 9). In all the cases the obtained values of the parameters are very close to their actual values.

### 5.3 Example 3

Let us consider the rail-to-rail input buffer [27] shown in Fig. 7. To arrange the diagnostic tests the input voltages  $V_{S1}$ ,  $V_{S2}$  and  $V_{S3}$  as well as the output voltage  $V_o$  are selected. The constants of the computation process are the same as in Example 1,  $R_o = 100 \text{ k}\Omega$ . Sensitivity analyses of the output voltage due to variations of the parameters  $L$  and  $TOX$  of the transistors reveal that all the transistors can be tested.

The following sets of the values of the input voltages have been chosen.



PT	VT
$V_{S_1} = 1.00 \text{ V } V_{S_2} = 0.50 \text{ V } V_{S_3} = 0.35 \text{ V},$	$V_{S_1} = 1.00 \text{ V } V_{S_2} = 0.30 \text{ V } V_{S_3} = 0.25 \text{ V},$
$V_{S_1} = 1.00 \text{ V } V_{S_2} = 0.50 \text{ V } V_{S_3} = 0.42 \text{ V},$	$V_{S_1} = 1.00 \text{ V } V_{S_2} = 0.40 \text{ V } V_{S_3} = 0.40 \text{ V},$
$V_{S_1} = 1.00 \text{ V } V_{S_2} = 0.50 \text{ V } V_{S_3} = 0.45 \text{ V},$	$V_{S_1} = 1.00 \text{ V } V_{S_2} = 0.50 \text{ V } V_{S_3} = 0.45 \text{ V},$
$V_{S_1} = 1.30 \text{ V } V_{S_2} = 0.80 \text{ V } V_{S_3} = 0.70 \text{ V},$	$V_{S_1} = 0.80 \text{ V } V_{S_2} = 0.40 \text{ V } V_{S_3} = 0.40 \text{ V},$
$V_{S_1} = 1.30 \text{ V } V_{S_2} = 0.80 \text{ V } V_{S_3} = 0.75 \text{ V},$	$V_{S_1} = 0.80 \text{ V } V_{S_2} = 0.50 \text{ V } V_{S_3} = 0.50 \text{ V}.$

**Table 6** Results of the fault diagnosis of the channel lengths in NMOS transistors M9, M10, M11

Actual values of the parameters	Values of the parameters determined by the method	Number of generated simplices	Computation time in seconds
$\Delta L_{M9} = 15.00 \text{ nm}$	$\Delta L_{M9} = 15.00 \text{ nm}$	90	31.4
$\Delta L_{M10} = 3.00 \text{ nm}$	$\Delta L_{M10} = 3.00 \text{ nm}$		
$\Delta L_{M11} = 15.00 \text{ nm}$	$\Delta L_{M11} = 15.00 \text{ nm}$		
$\Delta L_{M9} = 5.00 \text{ nm}$	$\Delta L_{M9} = 4.98 \text{ nm}$	85	29.6
$\Delta L_{M10} = 2.00 \text{ nm}$	$\Delta L_{M10} = 1.99 \text{ nm}$		
$\Delta L_{M11} = 7.50 \text{ nm}$	$\Delta L_{M11} = 7.53 \text{ nm}$		
$\Delta L_{M9} = 1.75 \text{ nm}$	$\Delta L_{M9} = 1.76 \text{ nm}$	67	23.2
$\Delta L_{M10} = 10.00 \text{ nm}$	$\Delta L_{M10} = 10.00 \text{ nm}$		
$\Delta L_{M11} = -1.50 \text{ nm}$	$\Delta L_{M11} = -1.51 \text{ nm}$		

**Table 7** Results of the fault diagnosis of the channel lengths in PMOS transistors M3, M4, M5

Actual values of the parameters	Values of the parameters determined by the method	Number of generated simplices	Computation time in seconds
$\Delta L_{M3} = 2.00 \text{ nm}$	$\Delta L_{M3} = 2.00 \text{ nm}$	94	32.2
$\Delta L_{M4} = 6.00 \text{ nm}$	$\Delta L_{M4} = 6.00 \text{ nm}$		
$\Delta L_{M5} = 6.00 \text{ nm}$	$\Delta L_{M5} = 6.00 \text{ nm}$		
$\Delta L_{M3} = 17.5 \text{ nm}$	$\Delta L_{M3} = 17.5 \text{ nm}$	92	30.8
$\Delta L_{M4} = 1.00 \text{ nm}$	$\Delta L_{M4} = 0.98 \text{ nm}$		
$\Delta L_{M5} = 1.50 \text{ nm}$	$\Delta L_{M5} = 1.50 \text{ nm}$		
$\Delta L_{M3} = 15.00 \text{ nm}$	$\Delta L_{M3} = 14.98 \text{ nm}$	79	26.6
$\Delta L_{M4} = 15.00 \text{ nm}$	$\Delta L_{M4} = 14.99 \text{ nm}$		
$\Delta L_{M5} = -3.00 \text{ nm}$	$\Delta L_{M5} = -3.00 \text{ nm}$		

**Table 8** Results of the fault diagnosis of the oxide thicknesses in NMOS transistors M9, M10, M11

Actual values of the parameters	Values of the parameters determined by the method	Number of generated simplices	Computation time in seconds
$\Delta TOX_{M9} = -140.0 \text{ pm}$	$\Delta TOX_{M9} = -140.0 \text{ pm}$	113	38.9
$\Delta TOX_{M10} = -56.0 \text{ pm}$	$\Delta TOX_{M10} = -55.9 \text{ pm}$		
$\Delta TOX_{M11} = -140.0 \text{ pm}$	$\Delta TOX_{M11} = -140.0 \text{ pm}$		
$\Delta TOX_{M9} = 490.0 \text{ pm}$	$\Delta TOX_{M9} = 489.7 \text{ pm}$	136	44.6
$\Delta TOX_{M10} = -28.0 \text{ pm}$	$\Delta TOX_{M10} = -31.0 \text{ pm}$		
$\Delta TOX_{M11} = 42.0 \text{ pm}$	$\Delta TOX_{M11} = 41.8 \text{ pm}$		
$\Delta TOX_{M9} = 70.0 \text{ pm}$	$\Delta TOX_{M9} = 69.8 \text{ pm}$	91	32.5
$\Delta TOX_{M10} = 70.0 \text{ pm}$	$\Delta TOX_{M10} = 69.6 \text{ pm}$		
$\Delta TOX_{M11} = -42.0 \text{ pm}$	$\Delta TOX_{M11} = -42.0 \text{ pm}$		

**Table 9** Results of the fault diagnosis of the oxide thicknesses in PMOS transistors M3, M4, M5

Actual values of the parameters	Values of the parameters determined by the method	Number of generated simplices	Computation time in seconds
$\Delta TOX_{M3} = -49.0$ pm	$\Delta TOX_{M3} = -48.5$ pm	155	51.8
$\Delta TOX_{M4} = 98.0$ pm	$\Delta TOX_{M4} = 98.5$ pm		
$\Delta TOX_{M5} = 112.0$ pm	$\Delta TOX_{M5} = 112.0$ pm		
$\Delta TOX_{M3} = 350.0$ pm	$\Delta TOX_{M3} = 350.6$ pm	191	60.6
$\Delta TOX_{M4} = 28.0$ pm	$\Delta TOX_{M4} = 28.5$ pm		
$\Delta TOX_{M5} = -42.0$ pm	$\Delta TOX_{M5} = -42.0$ pm		
$\Delta TOX_{M3} = -49.0$ pm	$\Delta TOX_{M3} = -47.9$ pm	149	48.6
$\Delta TOX_{M4} = 210.0$ pm	$\Delta TOX_{M4} = 211.1$ pm		
$\Delta TOX_{M5} = 210.0$ pm	$\Delta TOX_{M5} = 210.0$ pm		

**Table 10** Results of the fault diagnosis of the channel lengths in NMOS and PMOS transistors

Actual values of the parameters	Values of the parameters determined by the method	Number of generated simplices	Computation time in seconds
$\Delta L_{M6} = 8.00$ nm	$\Delta L_{M6} = 7.98$ nm	544	170.6
$\Delta L_{M7} = -2.00$ nm	$\Delta L_{M7} = -2.02$ nm		
$\Delta L_{M8} = 1.00$ nm	$\Delta L_{M8} = 0.99$ nm		
$\Delta L_{M9} = 8.00$ nm	$\Delta L_{M9} = 8.00$ nm		
$\Delta L_{M10} = 6.00$ nm	$\Delta L_{M10} = 5.99$ nm		
$\Delta L_{M1} = 15.00$ nm	$\Delta L_{M1} = 15.03$ nm	482	146.8
$\Delta L_{M2} = 3.00$ nm	$\Delta L_{M2} = 3.00$ nm		
$\Delta L_{M3} = 15.00$ nm	$\Delta L_{M3} = 15.00$ nm		
$\Delta L_{M4} = 3.00$ nm	$\Delta L_{M4} = 3.00$ nm		
$\Delta L_{M5} = 2.00$ nm	$\Delta L_{M5} = 2.00$ nm		

**Table 11** Results of the fault diagnosis of the oxide thicknesses in NMOS and PMOS transistors

Actual values of the parameters	Values of the parameters determined by the method	Number of generated simplices	Computation time in seconds
$\Delta TOX_{M6} = 42.0$ pm	$\Delta TOX_{M6} = 42.1$ pm	1316	408.1
$\Delta TOX_{M7} = 168.0$ pm	$\Delta TOX_{M7} = 168.1$ pm		
$\Delta TOX_{M8} = -42.0$ pm	$\Delta TOX_{M8} = -42.0$ pm		
$\Delta TOX_{M9} = 168.0$ pm	$\Delta TOX_{M9} = 168.0$ pm		
$\Delta TOX_{M10} = 42.0$ pm	$\Delta TOX_{M10} = 42.0$ pm		
$\Delta TOX_{M1} = 28.0$ pm	$\Delta TOX_{M1} = 27.9$ pm	530	181.3
$\Delta TOX_{M2} = -14.0$ pm	$\Delta TOX_{M2} = -14.0$ pm		
$\Delta TOX_{M3} = 98.0$ pm	$\Delta TOX_{M3} = 98.0$ pm		
$\Delta TOX_{M4} = 56.0$ pm	$\Delta TOX_{M4} = 56.0$ pm		
$\Delta TOX_{M5} = -28.0$ pm	$\Delta TOX_{M5} = -28.0$ pm		

**Table 12** Results of the fault diagnosis of the channel lengths in NMOS transistors M4, M5, M8, M9 given by method M2014

Actual values of the parameters	Values of the parameters determined by the method	Computation time in seconds
$\Delta L_{M4} = 6.00$ nm	$\Delta L_{M4} = 5.99$ nm	178.2
$\Delta L_{M5} = 4.00$ nm	$\Delta L_{M5} = 3.99$ nm	
$\Delta L_{M8} = 2.50$ nm	$\Delta L_{M8} = 2.50$ nm	
$\Delta L_{M9} = 6.00$ nm	$\Delta L_{M9} = 6.02$ nm	
$\Delta L_{M4} = 15.00$ nm	$\Delta L_{M4} = 15.02$ nm	180.3
$\Delta L_{M5} = 2.00$ nm	$\Delta L_{M5} = 1.98$ nm	
$\Delta L_{M8} = 15.00$ nm	$\Delta L_{M8} = 15.04$ nm	
$\Delta L_{M9} = 4.50$ nm	$\Delta L_{M9} = 4.53$ nm	
$\Delta L_{M4} = 2.50$ nm	$\Delta L_{M4} = 2.47$ nm	183.8
$\Delta L_{M5} = 2.00$ nm	$\Delta L_{M5} = 1.96$ nm	
$\Delta L_{M8} = 1.75$ nm	$\Delta L_{M8} = 1.76$ nm	
$\Delta L_{M9} = 20.00$ nm	$\Delta L_{M9} = 20.06$ nm	

**Table 13** Results of the fault diagnosis of the channel lengths in PMOS transistors M1, M2, M3 given by method M2014

Actual values of the parameters	Values of the parameters determined by the method	Computation time in seconds
$\Delta L_{M1} = 4.50$ nm	$\Delta L_{M1} = 4.57$ nm	172.7
$\Delta L_{M2} = 3.00$ nm	$\Delta L_{M2} = 3.05$ nm	
$\Delta L_{M3} = 1.00$ nm	$\Delta L_{M3} = 1.01$ nm	
$\Delta L_{M1} = 15.00$ nm	$\Delta L_{M1} = 15.01$ nm	178.4
$\Delta L_{M2} = 10.00$ nm	$\Delta L_{M2} = 9.99$ nm	
$\Delta L_{M3} = 2.50$ nm	$\Delta L_{M3} = 2.51$ nm	
$\Delta L_{M1} = 1.50$ nm	$\Delta L_{M1} = 1.46$ nm	171.2
$\Delta L_{M2} = 25.00$ nm	$\Delta L_{M2} = 25.03$ nm	
$\Delta L_{M3} = 1.00$ nm	$\Delta L_{M3} = 1.00$ nm	

**Table 14** Results of the fault diagnosis of the oxide thicknesses in NMOS transistors M4, M5, M8, M9 given by method M2014

Actual values of the parameters	Values of the parameters determined by the method	Computation time in seconds
$\Delta TOX_{M4} = 140.0$ pm	$\Delta TOX_{M4} = 141.3$ pm	190.2
$\Delta TOX_{M5} = -56.0$ pm	$\Delta TOX_{M5} = -55.6$ pm	
$\Delta TOX_{M8} = -28.0$ pm	$\Delta TOX_{M8} = -26.9$ pm	
$\Delta TOX_{M9} = 98.0$ pm	$\Delta TOX_{M9} = 97.9$ pm	
$\Delta TOX_{M4} = 280.0$ pm	$\Delta TOX_{M4} = 281.4$ pm	158.6
$\Delta TOX_{M5} = -56.0$ pm	$\Delta TOX_{M5} = -59.2$ pm	
$\Delta TOX_{M8} = 280.0$ pm	$\Delta TOX_{M8} = 282.7$ pm	
$\Delta TOX_{M9} = -42.0$ pm	$\Delta TOX_{M9} = -40.7$ pm	
$\Delta TOX_{M4} = 70.0$ pm	$\Delta TOX_{M4} = 70.8$ pm	179.5
$\Delta TOX_{M5} = -56.0$ pm	$\Delta TOX_{M5} = -56.0$ pm	
$\Delta TOX_{M8} = -49.0$ pm	$\Delta TOX_{M8} = -48.1$ pm	
$\Delta TOX_{M9} = 560.0$ pm	$\Delta TOX_{M9} = 559.1$ pm	

Some results of multiple soft fault diagnosis are summarized in Tables 10, 11. The obtained values of the parameters are very close to their actual values.

## 6 Conclusion

The method developed in this paper allows effective diagnosing multiple soft faults of the process parameters in small and middle-size ICs designed in nanometer technology. The method does not require access to internal nodes of the circuit. The set of the parameter values is obtained by solving nonlinear equations, not given in explicit analytical form, that may have more than one solution. The proposed approach, whose core is the Nelder–Mead optimization method, is capable of finding the multiple solutions and select the actual one. Numerical examples reveal that the accuracy of the determined parameter values is very good. The method does not allow testing the transistors whose parameters have slight influence on the output voltage. This is why the fault diagnosis process should be preceded by the sensitivity analyses.

The proposed method has been compared with the methods recently published in references [18] and [20] devoted to similar problem. They will be named M2016, M2014 and M2015, respectively.

At first we concentrate on the methods M2016 and M2014. To perform the comparison, method M2014 has been implemented to allow diagnosing CMOS circuits designed in nanometer technology, comprising the transistors characterized by the model BSIM 4.6. All 30 fault diagnoses included in Tables 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 providing the results found by method M2016, have been performed using method M2014 with the same diagnostic tests and the assumed measurement accuracy and the parameters  $\phi$ ,  $\xi$ ,  $k_{\max}$  as in [18] (Example 1). On the basis of these experiments the following conclusion can be drawn. Method M2014 is very sensitive to the tests and in numerous cases several tries must be taken to select the proper one. Moreover, sometimes this method requires more than one measurement node. In the great majority of cases method M2014 is more time consuming than method M2016. To be specific, let us consider in detail Example 1. For the diagnoses included in Tables 1, 2, 3 the results given by method M2014 are very similar to the ones provided by method M2016 (see Tables 12, 13, 14). In all cases, except one, method M2014 consumes more CPU time which is 1.48–6.64 times longer. For the cases presented in Tables 4, 5 method M2014 fails. However, it is possible to arrange another tests so that the method works and gives correct results. Unfortunately, the tests relating to the diagnoses indicated in Table 5 requires access to two measurement nodes.

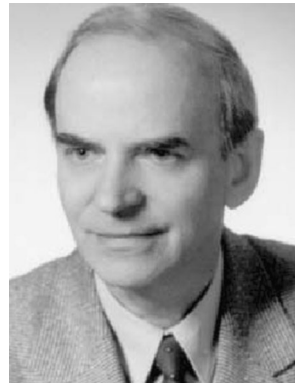
Method M2015 comprises very large class of circuits, including bipolar and CMOS ones, designed in micrometer and submicrometer technologies. In Ref. [20] the MOS transistors designed in nanometer technology are characterized by PSP103.1 model introduced into DELPHI environment. Thanks to this the circuit analyses are executed using a dedicated program written in DELPHI, that considerably improves the computation process and makes the method sound. To compare with M2016 the method M2015 was implemented including BSIM 4.6 modeled MOS transistors and circuit analyses were performed in IsSPICE 4. Method M2015 requires numerous sensitivity analyses that in this case must be performed using the brute-force incremental approach. In consequence this method needs large computing power and consumes much CPU time. Thus, method M2016 is less universal than M2015 but, in the case of CMOS circuits with BSIM 4.6 modeled transistors, faster and easier to implement. To be specific, all the cases presented in Tables 1, 2, 3, 4 were retaken using method M2015 with  $h = 0.05$ . The method gives the results very close to the ones provided by M2016, but the CPU time is 7–45 times longer.

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