Analog Integr Circ Sig Process (2015) 85:451–460
DOI 10.1007/s10470-015-0556-5

A 12-bit track and hold amplifier for giga-sample applications

Francesco Cannone[1] · **Gianfranco Avitabile**[1]

Received: 1 December 2014 / Revised: 29 April 2015 / Accepted: 2 May 2015 / Published online: 15 May 2015
© The Author(s) 2015. This article is published with open access at Springerlink.com

Abstract The paper presents a track-and-hold amplifier (THA), based on the switched emitter follower topology, suitable for emerging receivers architectures and data acquisition systems. The THA exploits four concurrent techniques, all described in the paper, which allow to reduce the hold-mode feedthrough; to attenuate the differential droop rate; to improve the linearity of the input buffer; and to optimize the third order harmonic distortion for RF sampling operation. The effectiveness of this novel approach is demonstrated using a low cost 0.35 µm SiGe technology. The THA core draws about 145 mA from 3.5 V supply. The THA provides a spurious-free dynamic range (SFDR) better than 72 dB when it is used for sampling an incoming signal of 0.9 V_{pp} centered around 925 MHz at a sampling rate of 0.5 GS/s. The THA allows a max sampling frequency equal to 6 GS/s and a max input frequency equal to 2.5 GHz and provides a SFDR better than 50 dB in all the available working conditions.

Keywords Track and hold amplifier · Switched emitter follower · RF sampling · SiGe · Microwave circuits

1 Introduction

In the last decades, the introduction of a number of different telecommunication standards and the corresponding growth of consumer markets strongly pushed forward both technologies and architecture developments for the transceiver analog front end. The cost effectiveness and the design reusability of the transmitter and receiver architecture became a key issue and the approaches based on the software radio (SR) paradigm [1] and RF sampling [2] begun to furnish viable solutions even for consumer applications. The acquisition and successive quantization of the received signal, indeed, allow a numerical manipulation of the signal with evident advantages in terms of re-configurability and adaptability of the receiver to different standards, most of all, when these operations are performable over a wide RF input frequency range covering several telecommunication standards.

The SR exploitation is strongly subject to the availability of high frequency ADCs and DSPs, which have to be still improved in terms of both speed and accuracy to be adequate to the challenge. At the state-of-the-art, the receiver architecture still relies on a preliminary down conversion to match the available ADCs and DSPs performances. As an alternative to the mixer, the sample & hold (S/H) mixer can perform the down conversion operation with comparable performances [2]. The resulting structures are usually referred as software defined radio (SDR) receivers.

An efficient reduction of the conversion rate of the sampling frequency is a key issue in the receiver in that it relaxes the DSP requirements. This goal can be achieved using various techniques, such as analog-decimation and sub-sampling ADCs, and their effectiveness strongly relies on the THA architecture.

As a matter of facts, multi-standard operation, resolution and flexibility requirements call for high sampling frequencies and high resolution track and hold amplifiers (THAs). The THAs architectures fall in two main categories, open-loop and closed-loop architectures. Open-loop structures allow high-speed operations while closed-loop structures assure better accuracy. Different technologies lead to different THA solutions.

✉ Francesco Cannone
f.cannone@poliba.it

[1] Politecnico di Bari, Bari, Italy

The use of advanced and, thus, expensive processes furnishes the means to satisfy speed and bandwidth requirements.

Recent literature reports InP THA operating up to 70 GS/s [3, 4]. Usually, a CMOS ADCs requiring a two-chip solution extremely difficult to package while preserving high-speed performance follows the InP THAs. In [5] is reported a THA in an InP BiCMOS process. The SiGe BiCMOS technologies are promising and cheaper alternatives which allow the use of high-f_T HBTs with CMOS devices even if these HBTs operate at lower frequencies than InP HBTs. Moreover, the literature reports high sampling frequency THAs fabricated in advanced RF-CMOS technologies [6].

Concurrently with the improvements achieved by the technologies, THA architectures must be improved in order to guarantee a suitable equivalent number of bits (ENOB). The most popular architectures are based on the diodes-bridges and switched emitter follower (SEF) stages. Usually the diode-bridge architecture requires higher supply voltage than the SEF architecture that, however, normally consumes more power.

The paper introduces a THA architecture whose core is a SEF sampling scheme which is the preferred choice when high sampling rates ($f_s > 0.5$GS/s) in conjunction with medium-to-high resolution performances ($\geq$8 bit) are required [7–15]. The proposed THA allows to increase the ENOB at high sampling rates. To achieve this result is mandatory to attenuate the effects of all the non-idealities of the THA. Four techniques are concurrently used to this purpose. The first technique described in [15] is able to minimize the differential droop rate, which is one of the key point in SEF architectures. The second technique aims to minimize the harmonic distortions by using the technique presented in [16]. The third technique gives an improved linearity and is based on an input buffer topology described in [17, 18], while the fourth technique introduced in [18] allows an advanced hold-mode feedthrough cancellation. The process independence of the reported techniques allows the porting of the THA in advanced processes when higher performances are required.

The paper is organized as follows: in Sect. 2 the proposed THA is presented and analyzed and in Sect. 3 the prototype measurements are discussed and compared with other THAs operating at GHz sampling rates and medium-to-high resolution.

2 Proposed THA

The open-loop THA has a pseudo-differential structure composed by two similar branches. The pseudo-differential topology allows to reduce the effect of the even order distortion components coming from all the "common-mode" non-idealities, like even order buffering distortion, common-mode pedestal errors and so on.

As depicted in Fig. 1, the THA is composed by three main blocks: the input buffer, the sampling circuit and the output buffer. The input signal is buffered, sampled by the SEF and, then, fed to the load via the output buffer. Two secondary blocks, the inter-stage buffer and the auxiliary amplifier, allow to minimize the effects of the signal feedthrough on the hold capacitor, C_H, during the hold phase.

In Fig. 2 the simplified schematic of the input buffer, the inter-stage buffer and the SEF stage are sketched.

The THA combines the techniques presented in [15–18]. The THAs in [15, 16] rely on the same topology and the same technology. Differently from the proposed THA, these circuits have an emitter degenerated cascode amplifier, shown in Fig. 3(c), as input buffer. Moreover, they do not use the inter-stage and auxiliary amplifier for reducing the hold-mode feedthrough, but a clamping diode which reduces the gain of the input amplifier during the hold mode. These THAs adopt the same output buffer topology and the HD3 reduction technique as the THA described in this paper.

The THAs in [15, 16] achieve high SFDR but a lower maximum sampling frequency when compared to the present THA, even being implemented in a much more performant and expensive technology. The improvements introduced in the THA presented in this paper depend on the improved control of the SEF operations given by the input buffer depicted in Fig. 3(a) and the auxiliary amplifier, if compared to the emitter degenerated cascode amplifier with the clamping diode of [15, 16].

The THA in [18] adopts the input buffer introduced in [17] and shares with the proposed THA the same technology process, the input buffer and auxiliary amplifier topologies but it uses a different output buffer and also a different sizing of many design parameters. The re-design and the substitution of the output buffer allowed to improve

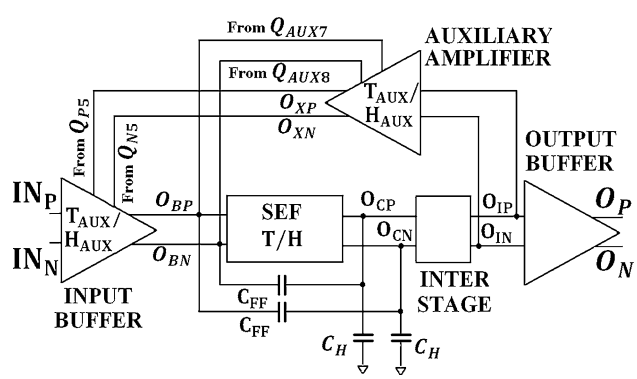

Fig. 1 THA architecture

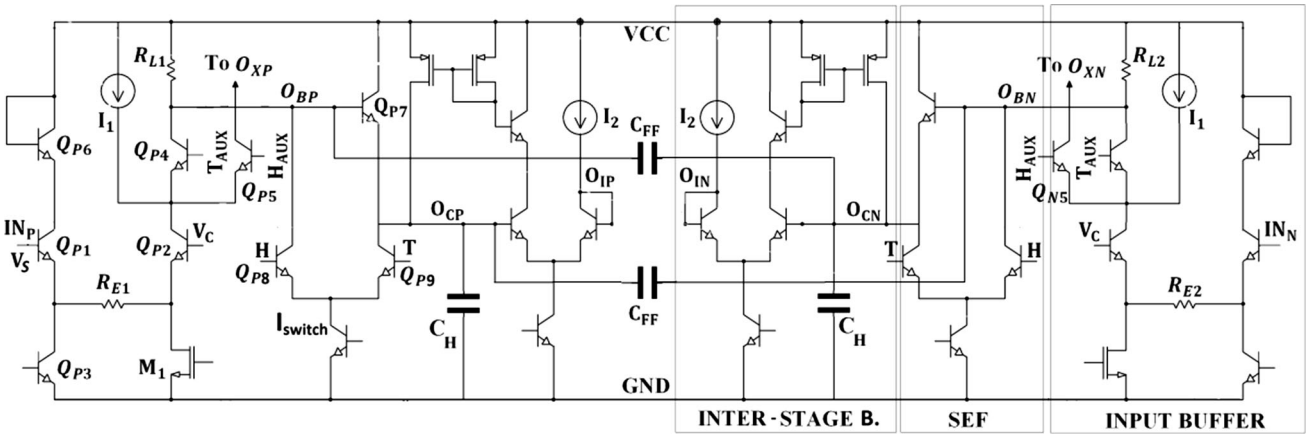

Fig. 2 Simplified schematic of Input buffer, inter-stage buffer and SEF stage

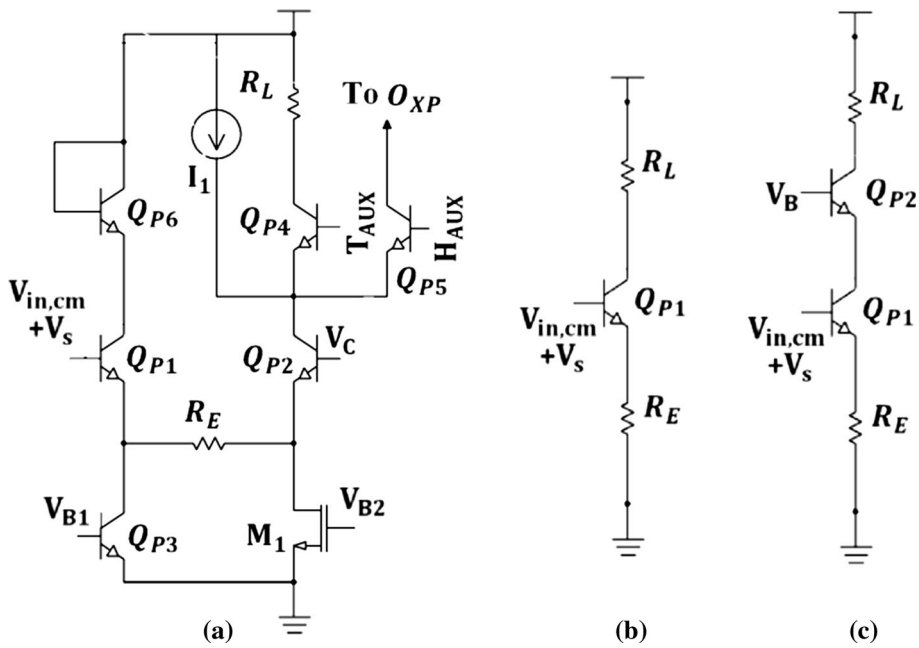

Fig. 3 Single ended version for: **a** adopted input buffer, **b** emitter degenerated amplifier, **c** emitter degenerated cascode amplifier

the performances of the THA in terms of SFDR and differential droop rate.

2.1 The input stage

The input buffer and SEF must be extremely linear during the tracking phase if an overall high linearity has to be achieved. The simplified schematic of the input buffer is depicted in Fig. 2. The input buffer is based on the scheme introduced in [18] which allows to design a degenerated common-emitter cascode amplifier with high linearity. This scheme is a modified version of the input buffer reported in [17]. The change consists in the replacement of the common base transistor of the original structure with the switching pair (Q_{P4}–Q_{P5} in Fig. 2). This modification allows to exploit the hold-mode feedthrough cancellation technique. In track mode the buffer has the same behavior of that in [17].

Normally for applications in the GHz range, the input buffer topologies are based on the degenerated common emitter amplifier. Some common choices are shown in Fig. 3(b), (c) in single-ended arrangements for sake of simplicity.

The buffer depicted in Fig. 3(a) assures distortion performances similar to the cascode (Fig. 3(c)) with the advantage of a voltage supply requirements much lower and similar to the simple degenerated common emitter amplifier (Fig. 3(b)). At high frequencies the simplified analytical model described in [17], confirmed by the simulations result, is able to predicts with a good approximation that

the linearity of the circuits in Fig. 3(a), (c) are similar and better than that of Fig. 3(b).

The couple Q_{P1} and R_E creates a trans-conductance amplifier similar to Fig. 3(b), the difference is that the other terminal of R_E is connected to the emitter of Q_{P2} instead of the ground. Since Q_{P2} is strongly current biased in order to work at very high frequencies, its emitter shows a very low impedance thus resulting in a "virtual" ground for the couple Q_{P1}–R_E which, considering only the first order effects, thus, behaves as the circuit in Fig. 3(b). The current dependent by the input signal and generated by the trans-conductor Q_{P1}–R_E reduced by the amount of bias current pulled by M_1 is fed by Q_{P2} to the load R_L through Q_{P4}. The current source I_1 sketched in Fig. 3(a) is used to reduce the supply requirements by removing part of the current through Q_{P4}, and thus through R_L. Since the emitter of Q_{P4} is a very low impedance node, loading it with a PMOS current source does not produce a sensible reduction of both the bandwidth and linearity, given the resulting reduced voltage swing. Hence, Q_{P1}–R_E–Q_{P2}–M_1–Q_{P5} form the highly linear trans-conductance amplifier of an equivalent "conventional" cascode and Q_{P4} the common base transistor. In the proposed circuit, the only nodes subject to a high voltage swing are the base and emitter of Q_{P1} and the collector of Q_{P4}.

It can be noticed that the distortion of the circuit in Fig. 3(b) is significantly higher because it is mainly determined by the Q_{P1} base–collector junction which undergoes a signal whose amplitude is two times that of the transistors subjected to high swing in Fig. 3(a, c).

The circuit in Fig. 3(a) draws more current than the one in Fig. 1(c), resulting in a higher power consumption because the larger drawn current is not completely compensated by the reduction in the supply voltage. This is the main drawback of the structure [17].

The design of the input buffer is brought out using the distortion model reported in [17]. The frequency dependent component of the third order harmonic distortion HD3 can be expressed as:

$$\begin{aligned}\left|HD_{3,im}\right| \cong j\omega\frac{V_S^2}{4} * \Bigg\{ & \frac{C_{\pi,Q_{P1}}}{V_T^2 T^3}\left(\frac{R_{B,Q_{P1}}+R_E}{R_E}\right) \\ & + \left(\frac{g_{m,Q_{P1}}}{g_{m,Q_{P2}}}\right)^4 \frac{C_{\pi,Q_{P2}}}{V_T^2 T^3}\left(\frac{R_{B,Q_{P2}}+R_E}{R_E}\right) \\ & + \left(\frac{g_{m,Q_{P1}}}{g_{m,Q_{P4}}}\right)^3 \frac{C_{\pi,Q_{P4}}}{V_T^2 T^3} \\ & + \alpha\left[\frac{R_{B,Q_{P1}}}{R_E}\frac{C_{\mu,Q_{P1}}}{\left(1+\frac{V_{cb,Q_{P1}}}{V_j}\right)^2} + \frac{C_{\mu,Q_{P4}}}{\left(1+\frac{V_{cb,Q_{P4}}}{V_j}\right)^2}\right]\Bigg\},\end{aligned} \tag{1}$$

where $\alpha = m_j(m_j+1)/V_j^2$, m_j and V_j are process parameters determining the capacitance of the reversed biased base–collector junction, V_S is the input signal voltage across the node IN_P, R_B is the base resistance, $T = g_{m,Q_{P1}}R_E$ is the loop gain, V_T is the thermal voltage. The load resistors $R_{L1,2}$ and the degeneration resistors $R_{E1,2}$ are 105 and 95 Ω, while the dc voltage at the node $IN_{N,P}$, V_C, T_{AUX} and $O_{BP,N}$ are 1.8, 1.3, 2 and 2.3 V respectively in track mode.

2.2 The SEF stage

The sampling circuit is the classical SEF optimized for high sample rates and high resolution. As shown in Fig. 2, the three transistors Q_{P7}, Q_{P8}, Q_{P9} represent the core of the SEF fed by I_{switch}, and loaded by the hold capacitance, C_H. In track-mode, the signal T is high and Q_{P7} acts as an emitter follower while Q_{P9} is in a common base configuration and the voltage across C_H tracks the input signals. The emitter coupled Q_{P8} and Q_{P9} are used to switch the current, I_{switch}, from Q_{P7} to R_{L1} during the hold phase. The augmented current in R_{L1} during the transition from the track to hold mode pulls down the voltage across the base of Q_{P7}.

The values of R_{L1}, I_{switch} and C_H are the key points to design a high sampling frequency THA. The voltage drop value must be enough for the SEF operation but simultaneously must avoid the complete switching off of Q_{P7} as this would reduce the speed of the THA. To improve the bandwidth, the load resistor R_{L1} of the input amplifier has to be small to maintain small the time constant at the node, but this means that, to produce the required voltage drop, a current higher than the optimum value for sampling rate could be needed. Finally the value of I_{switch} which optimizes the f_{max} of Q_{P7} usually is not compatible with the current necessary to produce the suitable voltage drop.

The values of I_{switch} and C_H are the main parameters which determine the linearity of the THA provided by the SEF stage. The suitable value of I_{switch} determines the compliance with the target distortion performances for a given value of C_H. The proposed THA use the technique described in [16] to further improve the HD3. This solution is based on the existence of a minimum of the HD3 related to the value of C_H as shown in Fig. 4(a).

This effect is due to a compensation between two different distortion sources which have different slope and opposite sign. One of these sources is related to the distortion component proportional to ω^3 [19]. The imaginary part of the HD3 can be expressed as:

$$\mathrm{IM}(\mathrm{HD}_3) = \left|\left(\frac{\omega}{\omega_1}\right)^{\alpha} - \left(\frac{\omega}{\omega_2}\right)^3\right| = 0, \tag{2}$$

where ω_1, ω_2 and α ($\alpha < 3$) are fitting parameters extracted from the simulations, therefore (2) is a partial aid for the designers and in order to better manage this technique, an

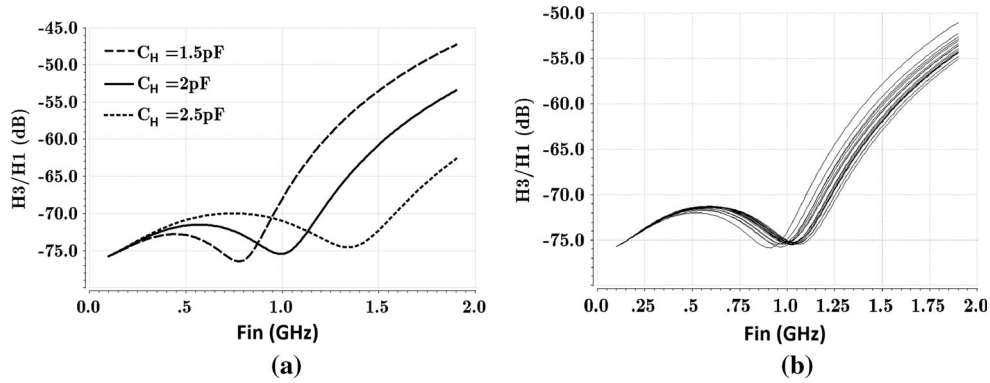

Fig. 4 **a** Third harmonic versus hold capacitor. **b** Third harmonic versus process variations

approximated analytical expression of the minimum should be useful. At the moment, the study on these distortion sources with different slope and opposite sign has not still provided this kind of equation. The basic idea is to size C_H for placing the minimum of HD3 close to the center band of the input signal. To verify the reliability of this technique over process variation, several Monte carlo simulations have been done. As shown in Fig. 4(b) the technique maintains its efficiency over process variation around the design point (1 GHz in this case).

Actually as mentioned before, the value of C_H directly affects the speed and linearity of the THA, then to exploit this technique a tradeoff is necessary.

2.3 The output buffer

As depicted in Fig. 5, the output buffer is obtained by the cascade of two voltage followers. These are optimized to reduce the differential droop-rate by using the technique described in [15]. The two cascaded stages have two different values of bias current, I_{ob1} and I_{ob2}. In the hold phase, the differential droop rate is one of the main factors limiting the resolution of the THA. This error has been mitigated by properly biasing the first stage of the output buffer.

It is possible to show that the differential droop rate is mainly due to the mismatch between the base currents of Q_{P10} and Q_{N10} [20] which depends on the sampled value across C_H during the hold phase. Taking into account that the order of magnitude of the current difference is proportional to the bias current, I_{ob1}, this latter must be kept as small as possible. On the other hand, the THA must drive the capacitive load presented by the first stage of the ADC. For this reason, a second buffer biased with a higher value of current, I_{ob2}, has been added to achieve a satisfactory slew rate.

Figure 6 reports the differential droop rate with a single buffer, the second one, and with the configuration with two cascaded buffers which result to be 1.55 and 0.18 mV/ns respectively.

The currents I_{ob1} and I_{ob2} are 1.2 and 12 mA. This technique is simple and effective. Indeed the comparison evidences that the proposed buffer provides a differential droop rate, equal 0.18 mV/ns, almost ten times better than the other one confirming that this error is roughly proportional to the value of the base current.

The relatively low dropped value is also due to the high value of the hold capacitor which is optimized for the specific application.

2.4 The hold-mode feedthrough reduction technique

The signal feedthrough on the hold capacitor C_H during the hold mode is one of the most important source of

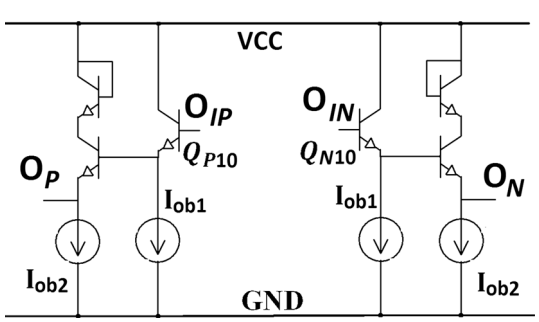

Fig. 5 Simplified schematic of output buffer

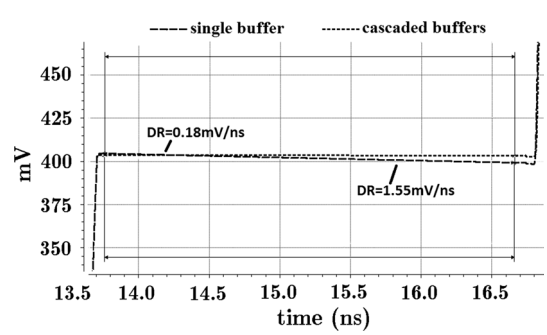

Fig. 6 Droop rate in the case of a single buffer and cascaded buffers

degradation of the overall performances. To reduce the effect of this non-ideality, usually the feed-forward capacitor C_{FF} [21] is adopted as shown in Fig. 2, generally in conjunction with other circuital solutions.

Different techniques can be used to further reduce this sampling error. The solution used for the THA is based on the solution introduced in [18]. The basic idea for attenuating the feedthrough is to reduce the swing at the entrance of the SEF stages. To this purpose, the same approach described in [7] has been exploited. However, a drawback of that technique is the sensible differential pedestal which derives from the asymmetric common mode drop during the hold phase at the differential input of the SEF stage (O_{BP}, O_{BN} in Fig. 1). If this differential pedestal is not properly managed it introduces a significant sampling error. The proposed THA is capable to reduce the differential pedestal thanks to the use of the auxiliary amplifier depicted in Fig. 7.

Indeed, to avoid the mentioned common mode drop it is sufficient that a proper copy of the input signal is present at the input of the SEF during the entire hold phase while the sampled value is stored on C_H. This is achieved by using the inter-stage buffer and the auxiliary amplifier. This latter tracks the differential voltage across C_H during the track-mode by means of the inter-stage buffer. During the transition from the track-mode to the hold-mode the input signal just before the sampling instant is restored at the differential input of the SEF stage by the auxiliary amplifier. To this purpose at the transition from track-mode to the hold-mode, the current flowing in Q_{P2} is switched from R_{L1} to R_{D1} through the couple Q_{P4} and Q_{P5} and the current flowing in R_{D1} is switched towards R_{L1} through the couple Q_{AUX5} and Q_{AUX7}. In this way, neglecting the effects of the layout parasitic and substrate coupling, the feedthrough is virtually completely removed. It is important to underline that this mechanism does not affect the SEF operation, indeed the sampling is properly realized switching-off Q_{P7} by steering the bias current from Q_{P7} to R_{L1}, until a fast and sufficient voltage drop at O_{BP} is assured.

3 Experimental results

3.1 The prototype and the measurement set up

The THA prototype has been designed using AMS 35 μm SiGe f_T—65 GHz technology. A photograph of the multi-function chip containing the THA is reported in Fig. 8. Its dimensions are about 0.65 × 1.4 mm^2. A QFN-64 package houses the chip and the test board used for measuring the THA is shown in Fig. 9. The THA absorbs 145 mA from 3.5 V supply voltage. Figure 10 depicts the test bench used to evaluate the THA prototype. A spectrum analyzer measures the output of the THA in both the track and hold phases while the input signal is fed by a signal generator to the DUT using a 1:1 balun mounted on the test board. The clock signal is equally fed in a balanced form with a similar balun. The output pins are loaded by a suitable voltage divider in order to reduce the effects of the artifacts produced by the board and bonding parasitic components. The chosen value for R is 1 kΩ.

The spectrum analyzer (HP-E4407B) has a single ended input and, thus, only one of the DUT differential outputs is measured while the other one is loaded by a 50 Ω termination. The unbalanced measurement suffers from a second harmonic component which is higher than the real residual second harmonic that pseudo-differential THA is able to provide and that would be measured by a true balanced measurement. All the simulations show that the SFDR is dominated by the third harmonics, being the residual second harmonics always lower than the third harmonics. The single-ended measurement does not allow to exactly estimate the value of the residual second harmonics provided

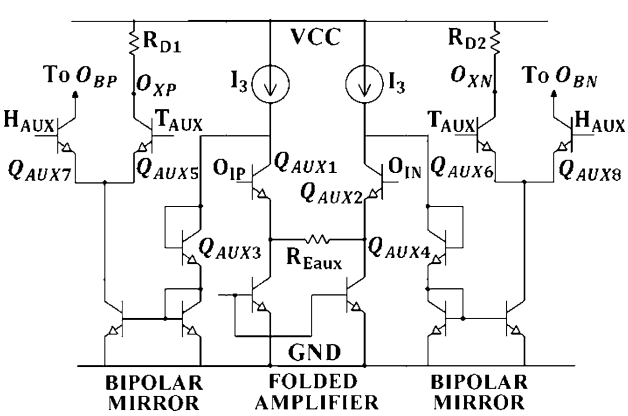

Fig. 7 Auxiliary amplifier

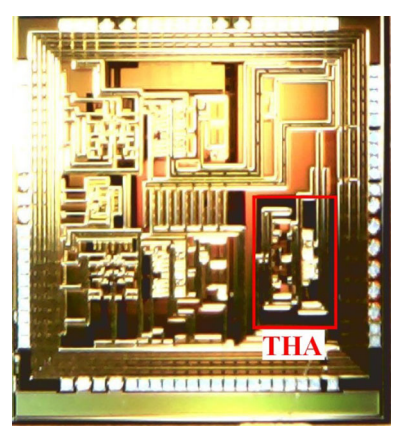

Fig. 8 Die photograph of the multi-function chip containing the prototype THA

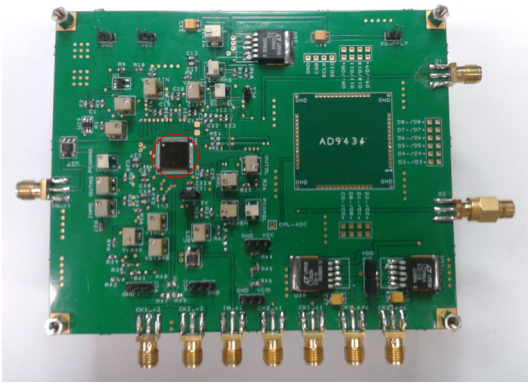

Fig. 9 Photograph of PCB used for testing the THA

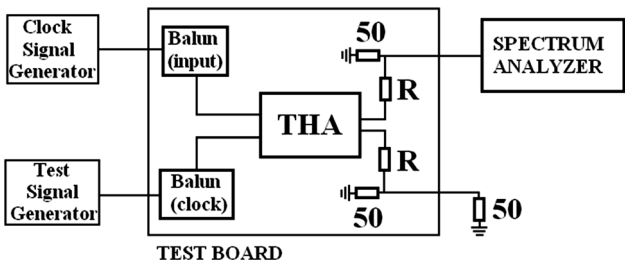

Fig. 10 Measurement set up

by the THA. Taking into account the simulations results and the single ended measurement limits, we have assumed that the real second harmonics are lower than the third harmonics and therefore we have eliminated them from the measurements of the SFDR. The DUT has been tested both in Track and T & H mode with variable clock frequencies and variable input frequency. The resolution bandwidth of the spectrum analyzer was set to its minimum value of 10 Hz in order to obtain the best noise floor that was around −130 dBm.

3.2 The measurements

The THA has been designed to maximize the linearity for sampling a RF incoming signal center around 1 GHz in the band from 900 MHz to 1.1 GHz with the minimum distortion around 1 GHz under sub-sampling condition at a sampling rate of 0.5 GS/s. The effect of the distortion cancellation discussed in Sect. 2 and reported in [16] theoretically guarantees extremely linear operations for the THA. The measurements showed that the minimum is at 925 MHz closely matching the predicted value. This shift is mainly due to the process variations, indeed the value of this shift (75 MHz) is compatible with the Montecarlo simulations reported in Fig. 4. It is worth to note that the proposed technique even in presence of this shift is still effective since at 1 GHz the SFDR reaches the very good value of 70 dB.

Figure 11 reports the fundamental and 3rd harmonic at this frequency. As mentioned before, being the measured signal single ended, the second harmonic exists but it is has been not considered in the measurements since, as simulations show, the SFDR is set by the third harmonic thanks to the pseudo-differential topology of the THA. As can be clearly seen, the instrument noise floor masks the 3rd harmonic and the suppression is better than 74 dB, compatible with a 12 bit A to D quantization.

The THA has been tested with a set of sinusoidal input signals at the full scale range level (0.9 Vpp) in the 800 MHz to 1.2 GHz frequency range in 25 MHz steps. The THA outputs have been evaluated by the spectrum both in track and in track and hold mode with f_s equal to 0.5 GS/s.

In Fig. 12 the measured SFDR in this band is shown, the values have been reported in correspondence of the input frequencies. It is possible to note how the minimum of the distortion is almost centered around 1 GHz and there is only a small shift toward the lower frequencies. In the same Fig. 9 for comparison reasons also the simulated SFDR is reported.

The measured Full Power Bandwidth is equal to 2.5 GHz and the measured differential droop rate is equal to 0.18 mV/ns.

The THA has been tested for different values of the input frequency from 50 MHz to the max input frequency equal to 2.5 GHz and different values of the sampling frequency from 0.5 GS/s to the max sampling frequency equal to 6 GS/s.

The linearity in track mode, HD3, is the parameter which mainly determines the resolution of the THA for sampling frequency close to 1 GS/s, while, for higher sampling frequency, the resolution is not still dominated only by the linearity in track mode but by all the other non-idealities. As a result, in the spectra of the sampled outputs it is no more present the maximum of the SFDR in correspondence of the minimum of HD3.

The SFDR observed at the output versus the sampling frequency is reported in Fig. 13 with an input frequency of 925 MHz and a sampling frequency ranging from 2 to 6 GS/s.

In Table 1 the comparison among THAs operating at GHz sampling rates and medium-to-high resolution reported in literature using different technologies is summarized.

For better comparing the reported THAs, the following figure of merit has been adopted, FOM = Power/(2^{ENOB} * Fs). The ENOB has been estimated starting from the available values of SFDR, in this way this FOM takes

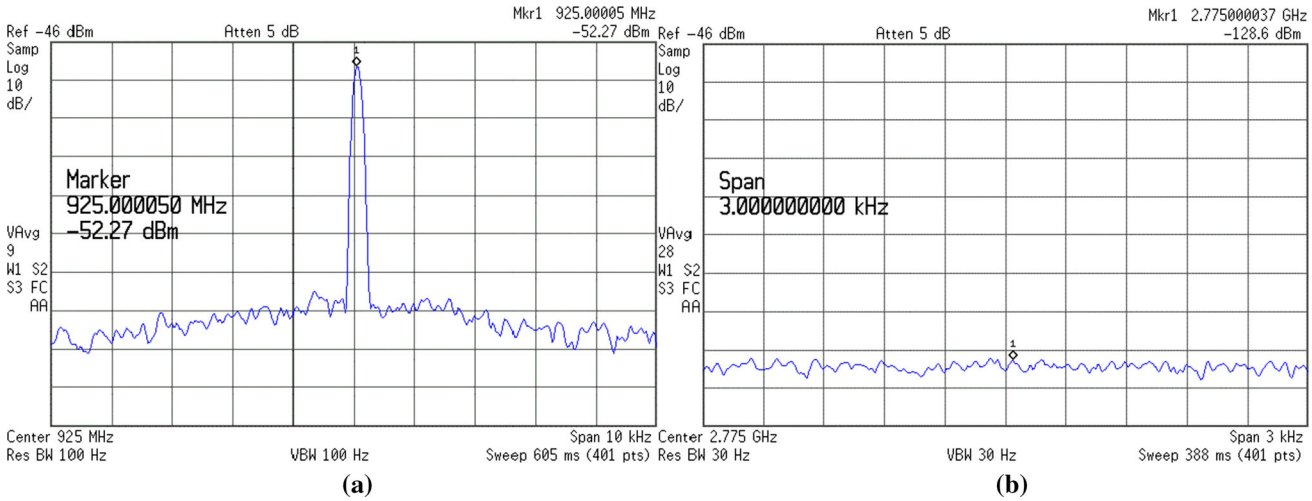

Fig. 11 First (**a**) and third (**b**) harmonic @ $f_{IN} = 925$ MHz and $f_S = 500$ MS/s

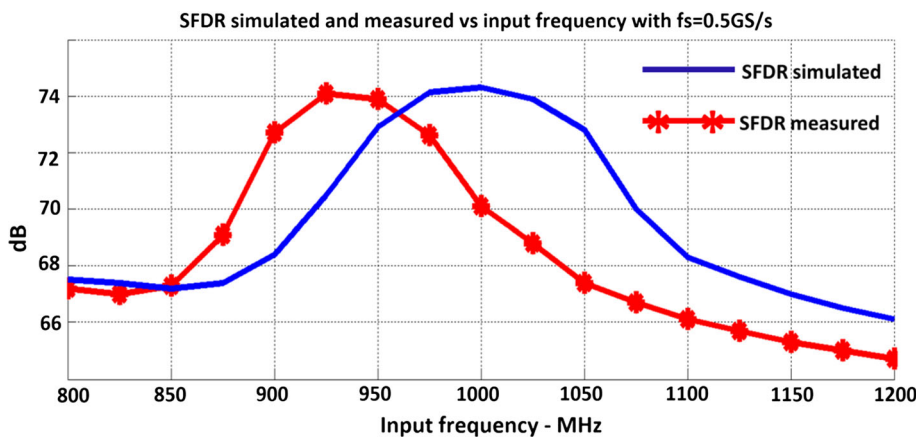

Fig. 12 Measured and simulated SFDR for f_{IN} from 800 to 1200 MHz with f_S equal to 500 MS/s

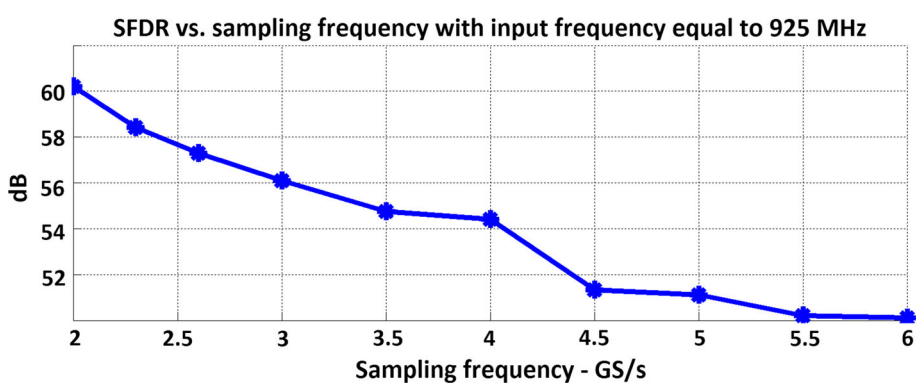

Fig. 13 Measured SFDR for f_{IN} equal to 925 MHz versus f_S from 2 to 6 GS/s

into account the power, the linearity and the speed being equal to the following ratio, FOM = Power/(Linearity * Speed).

It is possible to note that the proposed THA, properly adopting the mentioned techniques, is able to provide a better linearity than the other reported THAs, for the desired RF sampling. In this operating condition, the measured SFDR is similar to that reported in [15] which, however, uses a more expensive technology. Moreover, even when the proposed THA is used in operating conditions different from those corresponding to the optimum (that is f_{IN} from 900 to 1100 MHz and $f_S < 1$GS/s), it provides better performances than the other THAs in terms of max sampling frequency and max input frequency and

Table 1 Comparison results of THAs operating at GHz sampling rates and medium-to-high resolution

References	FSR V_{pp}	Fin (GHz)	Fs (GHz)	SFDR (dB)	Max Fs (GHZ)	Max Fin (GHZ)	Power dissipation	Technology	FOM (pJ/conv)
[7]	0.4	0.55	1.1	62	1.6	0.8	258 mW	0.18 µm—CMOS	5.01
[8]	2	1	10	49	10	3	800 mW	0.25 µm—SiGe	0.35
[9]	0.9	1.1	4	51	8	1.1	590 mW	0.5 µm—SiGe	0.25
[10]	0.8	0.4	2	54	2	0.9	550 mW	0.35 µm—SiGe	0.67
[11]	0.3	0.5	1	62	1	0.5	25 mW	0.8 µm—SiGe	0.02
[12]	0.3	0.5	2.5	45.8	2.5	0.5	n.a.	0.13 µm—CMOS	n.a.
[13]	0.7	2	1	45.1	1	15	n.a.	InP-DHBT	n.a.
[14]	0.35	0.1	0.4	62	0.5	1	164 mW	0.5 µm—SiGe	0.32
[15]	1	1	0.5	73	1.5	1.2	480 mW	0.25 µm—SiGe	0.09
This work	0.9	0.92	0.5	74	6	2.5	507 mW	0.35 µm—SiGe	0.05

similar in terms of SFDR, FSR and power consumption. Only the THA introduced in [11] presents a power consumption really lower than all the other THAs.

Looking at the FOM which represents a more complete characterization of the THAs than a single result like the power consumption, the performances provided by the THAs in [11, 15] and those described in this work are very close and are the best reported ones. As a matter of facts, given the technology, the higher is the sampling frequency the higher is the power consumption. In fact among the compared THAs those in [8, 9] and in that here presented have the higher maximum sampling frequency and the higher power consumption. In [11] a good optimization in terms of power saving has been proposed, nevertheless, the maximum sampling frequency is the lower one and this result in the lower power consumption.

In general, the increased bias currents and the supply voltage improve the speed but, also, the linearity and the power consumption. The proposed THA reaches a very high level of linearity matched only by the THA in [15] with a reasonable power consumption. This is evident looking at the Table 1, indeed aside the THA in [11] and [15], the FOM of the THA described in this work is sensibly better than all the other ones. This makes the proposed THA a suitable choice for high linearity and high speed sampling systems.

4 Conclusions

The work presented a THA operating up to 6 GS/s, with a FPBW equal to 2.5 GHz optimized for RF sampling suitable for advanced A to D stage. Measurements reported a SFDR better than 70 dB, with a 900 mVpp input signal in RF sampling operation and a SFDR better than 50 dB in all the other available sampling condition. The comparison highlighted that the THA introduces significant improvements into the state-of-the-art making it a suitable choice for advanced receivers architectures and data acquisition systems.

Open Access This article is distributed under the terms of the Creative Commons Attribution 4.0 International License (http://creativecommons.org/licenses/by/4.0/), which permits unrestricted use, distribution, and reproduction in any medium, provided you give appropriate credit to the original author(s) and the source, provide a link to the Creative Commons license, and indicate if changes were made.

References

1. Mitola, J. (1995). The software radio architecture. *IEEE Communications Magazine, 33*(5), 26–38.
2. Jakonis, D., Folkesson, K., Eriksson, P., & Svensson, C. (2005). A 2.4-GHz RF sampling receiver front-end in 0.18-µm CMOS. *IEEE Journal of Solid State Circuits, 40*(6), 1265–1277.
3. Daneshgar, S., Griffith, Z., Seo, M., & Rodwell, M. J. (2014). Low distortion 50 GSamples/s track-hold and sample-hold amplifiers. *IEEE Journal of Solid State Circuits, 49*(10), 2114–2126.
4. Deza, J., Ouslimani, A., Konczykowska, A., Kasbari, A., Godin, J., & Pailler, G. (2013). 70 GSa/s and 51 GHz bandwidth track-and-hold amplifier in InP DHBT process. *Electronic Letters, 49*(6), 388–389.
5. Gathman, T. D., Madsen, K. N., Li, J. C., Oh, T. C., Buckwalter, J. F. (2014). A 30 GS/s double-switching track-and-hold amplifier with 19 dBm IIP3 in an InP BiCMOS Technology. *Proceedings of IEEE International Solid-State Circuits Conference* (pp. 499–501).
6. Ma, S., Wang, J., Yu, H., Ren, J. (2014). A 32.5-GS/s two-channel time-interleaved CMOS sampler with switched-source follower based track-and-hold amplifier. *Proceedings of IEEE MTT-S International Microwave Symposium* (pp. 1–3).
7. Dinc, H., & Allen, P. E. (2009). A 1.2 GSample/s double-switching CMOS THA with 62 dB THD. *IEEE Journal of Solid State Circuits, 44*, 848–861.

8. Halder, S., Gustat, H., Scheytt, C. (2006). An 8 bit 10 GS/s 2 Vpp track and hold amplifier in SiGe BiCMOS technology. *Proceedings of ESSCIRC* (pp. 416–419).
9. Smola, D., Huijsing, J. H., Makinwa, K. A. A., Ploeg, H. V. D., Vertregt, M., Breems, L. (2006). An 8-bit, 4-Gsample/s track-and-hold in a 67 GHz f_t SiGe BiCMOS technology. *Proceedings of ESSCIRC* (pp. 408–411).
10. Vessal, F., & Salama, C. A. T. (2002). A bipolar 2-GSample/s track-and-hold amplifier (THA) in 0.35 pm SiGe techmology. *Proceedings of ISCAS, 5*, 573–576.
11. Boni, A., Parenti, M., & Vecchi, D. (2006). Low-power GS/s track-and-hold with 10-b resolution at nyquist in SiGe BiCMOS. *IEEE Transactions on Circuits and Systems II, 53*(6), 429–433.
12. Macedo, M., Roberts, G. W., Shih, I. (2012). Track and hold for giga-sample ADC applications using CMOS technology. *Proceedings of ISCAS* (pp. 2725–2728).
13. Bouvier, Y., Ouslimani, A., Konczykowska, A., & Godin, J. (2009). A 1-GSample/s, 15-GHz input bandwidth master-slave track-and-hold amplifier in InP DHBT technology. *IEEE Transactions on Microwave Theory and Techniques, 57*(12), 3181–3187.
14. Razzaghi, A., Chang, M. F. (2003). A l0-b, 1-GSample/s track-and-hold amplifier using SiGe BiCMOS technology. *Proceedings of CICC* (pp. 433–436).
15. Cannone, F., Avitabile, G., Coviello, G. (2013). A 11-bit track and hold amplifier in 0.25 μm SiGe BiCMOS for RF sampling receivers. *Proceedings of MWSCAS* (pp. 792–795).
16. Cannone, F., Cascella, D., Avitabile, G., Coviello, G. (2012). A high bandwidth 11-bit 1.5 GS/s track and hold amplifier in 0.25 μm SiGe BiCMOS. *Proceedings of SMACD* (pp. 459–452).
17. Avitabile, G., Cascella, D., Cannone, F., & Coviello, G. (2012). Low distortion input buffer for high resolution GS/s rate track-and-hold amplifiers. *Electronic Letters, 48*(13), 755–757.
18. Cascella, D., Cannone, F., Avitabile, G., Coviello, G. (2012). A 2.5-GS/s 62 dB THD SiGe track-and-hold amplifier with feed-through cancellation technique. *Proceedings of ICECS* (pp. 109–112).
19. Hoskins, M. J., Williams, D. R. (2003). High-speed SiGe HBT track-and-hold. *Proceedings of Instrumentation and Measurement Technology Conference* (pp. 1448–1453).
20. Baumheinrich, T., Pregardier, B., & Langmann, U. (1997). A 1-GSample/s 10-b full Nyquist silicon bipolar track&hold IC. *IEEE Journal of Solid State Circuits, 32*, 1951–1960.
21. Vorenkamp, P., & Verdaasdonk, J. P. M. (1992). Fully bipolar, 120-Msample/s 10-b track-and-hold circuit. *IEEE Journal of Solid State Circuits, 27*(7), 988–992.

Francesco Cannone received the Laurea degrees in electronic engineering, in 2005 and the Ph.D. degree in information engineering from the Politecnico di Bari, Italy, in 2005 and 2009 respectively. Since 2009 he has been a Researcher with ETLCLAB – D.E.I – Politecnico di Bari. His main research interest is RFIC circuits and systems.

Gianfranco Avitabile received in 1992 the Laurea degree in electronics from the Florence University, Italy. He Joined soon after the Department of Electronics of University of Florence as Assistant Professor. From the 1998 he joined the Department of Electronics of the Politecnico di Bari as Associate Professor, where currently works. His fields of interest are mainly the High frequency circuits for both civil and military applications.