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GUEST EDITORIAL

Introduction to the special issue on "High performance analog circuits and design methodologies"

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This special issue in the SPRINGER Journal of Analog Integrated Circuits and Signal Processing is published with four papers. We called for papers related to "High performance analog circuits and design methodologies" mainly from those presented at the 2013 International Conference on Analog VLSI Circuits (AVIC 2013). Two papers are selected from this conference.

The Research Committee on Electronic Circuits of the Institute of Electrical Engineers of Japan (IEEJ) organized AVIC 2013 in Montreal, Canada on October 16–18, 2013, in cooperation with the IEEE Montreal Section. This conference is the successor of the former International Analog VLSI Workshop. Its purpose is to exchange information, ideas and recent research results on analog VLSI circuits and their applications.

The first paper, "IC Implementation of an Interstitial Cell-based CPG Model," by Saeki et al. suggests a central pattern generator (CPG) model in which swing and stance patterns produced by interstitial cells generate low-frequency patterns through a low-capacitance 0.18 μm CMOS process. It is demonstrated that this model method can generate five basic quadruped locomotion patterns (walk, pace, trot, bound, and gallop) at a frequency suitable for controlling a quadruped locomotion robot.

The second paper, "A Digitally Calibrated Dynamic Comparator Using Time-Domain Offset Detection," by Okazawa et al. presents a self-calibrating dynamic latched comparator that does not require additional static current or load capacitors to reduce its offset voltage. The proposed comparator uses a reconfigurable differential pair at the input stage; the configuration is determined by a digital calibration scheme that automatically matches the differential pair, resulting in a low offset voltage.

The third paper "A Chopper-Stabilized Instrumentation Amplifier Using Area-Efficient Self-Trimming Technique," by Akita and Ishida presents an area-efficient self-trimming technique for precision chopper-stabilized instrumentation amplifier. The amplifier uses a reconfigurable differential pair for the input stage and it is automatically configured to reduce the mismatch of the differential pair, suppressing the chopper ripple.

The last paper "A 0.3-V Power Supply 2.4-GHz-Band Class-C VCO IC with Amplitude Feedback Loop in 65-nm CMOS," by Yang et al. proposes a Class-C VCO IC with an amplitude feed-back loop for ultra-low-voltage application. The Class-C VCO consists of an LC-VCO circuit and an amplitude feedback loop to shift LC-VCO bias condition from initial Class-AB start-up to steady Class-C low current oscillation.

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