Analog Integr Circ Sig Process (2013) 74:1–2
DOI 10.1007/s10470-012-9995-4

GUEST EDITORIAL

Introduction to the Special Issue on 29th NORCHIP Conference

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Received: 3 September 2012 / Accepted: 19 November 2012 / Published online: 7 December 2012

This special issue of Analog Integrated Circuits and Signal Processing presents extended versions of five papers selected from the 29th NORCHIP Conference. NORCHIP is an annual conference alternating between the Scandinavian and Baltic countries. In 2011 the conference was held in Lund, Sweden, on November 14, 15. In total 53 technical papers were presented during the 2 days, in parallel oral sessions and in poster sessions. After receiving input from the session chairmen, a local committee including the guest editor identified and invited the papers believed to be of highest interest to the readers of the Journal.

In the first paper, Timo Rahkonen and Janne Aikio compare ordinary and time-varying Volterra analysis. It is shown that an ordinary time-invariant Volterra analysis with fitted polynomial models can be used in such nonlinear applications as mixers and switching power amplifiers, where time-varying Volterra analysis has often been used. The use of time-invariant Volterra with fitted polynomial coefficients is also illustrated by analyzing two example circuits using a recently developed Volterra-on-Harmonic-Balance analysis tool.

The paper by Andrea Bevilacqua and Pietro Andreani presents a wide band local oscillator generation technique based on a single LC oscillator and frequency multiplication by 3/2. The frequency multiplication is obtained by cascading a broadband injection locked modulo-two divider and a multiply-by-three circuit based on edge combining. As this does not require any additional inductors, the circuit is very compact. Still it allows the generation of all frequencies from 2.7 to 6.1 GHz with a performance suitable for cellular standards.

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Dejan Radjen, Pietro Andreani, Martin Andersson and Lars Sundström have designed a continuous-time delta-sigma modulator. They use a switched-capacitor-resistor network in the DAC to shape the feedback current pulse, resulting in reduced jitter sensitivity and slew-rate requirements of the amplifiers. The circuit has been implemented in a 65-nm CMOS process and targets low power applications. It achieves a measured SNDR of 70 dB over a 125 kHz bandwidth, consuming 380 μW from a 900 mV supply.

Francesco Centurelli, Andrea Simonetti and Alessandro Trifiletti present a common-mode feedback technique for differential difference amplifiers (DDA). They use the body terminal of the MOS transistor in a body-driven positive-feedback frequency compensation. This improves the linearity for precision DDA-based sample and hold applications. Theoretical calculations have been carried out together with circuit simulations in a 130-nm CMOS process to demonstrate the benefits.

Anders Nejdel, Markus Törmänen and Henrik Sjöland have designed a linearized receiver front-end for cellular applications in 65-nm CMOS. A complementary common-gate LNA is used, and to meet the stringent linearity requirements it employs positive feedback with transistors biased in the sub-threshold region, resulting in cancellation of the third order non-linearity. Measurements of the front-end show about 3.5 dB improvement in out-of-band IIP3 at optimum bias of the positive feedback devices in the LNA, resulting in an out-of-band IIP3 of 10 dBm.

The five papers above have been subject to normal review process, which despite the tight time schedule of the special issue has resulted in many improvements of the papers. For this I would like to thank all reviewers and authors for their efforts. I would also like to thank Professor Erik Bruun for handling the review process of paper 5. Finally I would like to express my gratitude for all the help received from the Springer staff throughout this process.

Henrik Sjöland received the M.Sc. degree in electrical engineering from Lund University, Sweden, in 1994, and the Ph.D. degree from the same university in 1997. In 1999 he was a postdoc at UCLA on a Fulbright scholarship. He has been an associate professor at Lund University since year 2000, and a full professor since 2008. Since 2002 he is also part time employed at Ericsson Research. He has authored or co-authored more than 100 international peer reviewed journal and conference papers and holds 20 patents. His research interests include design of radio frequency, microwave, and mm wave integrated circuits, primarily in CMOS technology.