

## 2.5 Gb/s CMOS preamplifier for low-cost fiber-optic receivers

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**Abstract** This paper reports an optical preamplifier intended for low-cost fiber-optic receivers. The preamplifier is based on a resistive shunt-feedback topology, is power-optimized and employs two different frequency compensation techniques, phantom zeros and shunt-peaking. The circuit is designed in a 1.8 V 0.18  $\mu\text{m}$  CMOS technology. Experimental results report a transresistance of 58  $\text{dB}\Omega$  and a bandwidth of 1.5 GHz, respectively. Eye diagrams obtained at 2.5 Gb/s show a total jitter of 18 ps and a bit error rate (BER) of  $10^{-12}$  when the input current amplitude ( $I_{\text{in}}$ ) is equal to or higher than 8.5  $\mu\text{A}$ . Higher bit rates up to 3 Gb/s also have been tested achieving a BER of  $10^{-12}$  when  $I_{\text{in}} \geq 9.5 \mu\text{A}$ . The power consumption and die active area are 23.7 mW and 0.017  $\text{mm}^2$ , respectively.

**Keywords** Fiber-optic receiver · Low-cost front-end · CMOS preamplifier · Transimpedance amplifier

### 1 Introduction

When designing fiber-optic systems suitable for local area networks (LANs), two conditions must be accomplished, low cost and high performance. Obviously this is not an easy task as such conditions are strongly dependent on technology as well as on the design of the whole optical network.

Currently, a wide variety of integration technologies is available on the market. However, if a low price is the aim, the best choice is the use of CMOS technology. The designer simultaneously benefits from the advantages of downscaling which allows for reducing the power consumption, improving the maximum operation frequency and obtaining more compact designs [1, 2].

One of the most important modules in an optical network is the receiver. The design of this module involves two aspects (1) the choice of the architecture and (2) the implementation of its various blocks. A typical receiver architecture includes a front-end for detecting and conditioning the signal, and digital circuitry to process the information. The front-end comprises three main blocks: the preamplifier (Pre), the postamplifier (Pos) and the clock and data recovery circuit (CDR), see Fig. 1.

The preamplifier converts the current generated by the photodiode (PD) into voltage. It imposes several restrictive design conditions: high gain, large bandwidth and low noise. Among all the preamplifiers reported in literature, those based on the current-mode approach and shunt-feedback transimpedance amplifiers present the best trade-off between all design conditions [3]. However, the higher power consumption and larger noise contribution of current-mode preamplifiers leave the shunt-feedback transimpedance amplifier as the preamplifier which offers the best trade-off between signal-to-noise ratio and frequency response. The topology of a shunt-feedback transimpedance amplifier employs the block diagram shown in

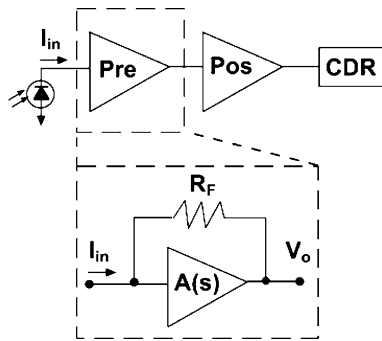
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**Fig. 1** Optical front-end receiver architecture and block diagram of a shunt-feedback transimpedance amplifier

Fig. 1. It consists of a voltage amplifier with a resistive feedback loop where  $A(s)$  represents the transfer function of the open-loop amplifier and  $R_F$  implements the feedback loop [4].

This work proposes a new shunt-feedback transimpedance amplifier (TIA). Sect. II will describe the design of the proposed preamplifier. The measurement results will be summarized in Sect. III. Finally, the conclusions will be drawn in Sect. IV.

## 2 Proposed preamplifier

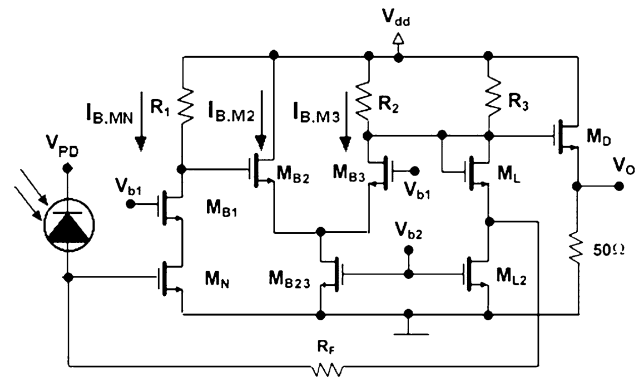
Following a structured design methodology, the optimization of the main critical performance metrics is achieved in an orthogonal fashion, stage by stage, providing advantages like simplicity and efficacy [5].

Noise, bandwidth and transresistance are the key parameters for a preamplifier. However, making the open-loop gain of the active part high enough, the transresistance depends only on  $R_F$  and can thus be set accurately [6]. Therefore, the active part should employ two stages, one optimized for noise and the other optimized for bandwidth.

We propose the preamplifier shown in Fig. 2. The first stage is a cascode topology comprising a common-source (CS) stage. The second is a source-coupled non-inverting stage, comprising a common-drain (CD) stage and a common-gate (CG) stage. The feedback network is based on a high resistivity resistor in series with a DC floating voltage source implemented with a diode-connected transistor,  $M_L$  ( $W/L = 45/0.18$ ), biased by  $M_{L2}$  ( $W/L = 70/0.18$ ) and  $R_3$  ( $420 \Omega$ ). This floating voltage source works as a level shifter setting the required DC level at the input. The last stage,  $M_D$  ( $W/L = 80/0.18$ ), is a  $50 \Omega$  output driver for test purposes.

### 2.1 Transresistance

A TIA converts the photocurrent generated by the PD into a voltage. The relationship between these two electrical magnitudes is given by the transresistance. Ideally, this



**Fig. 2** Proposed preamplifier topology

relationship must be linear and obviously, the use of passive resistors is the preferable choice here. Another possibility is to use NMOS or PMOS transistors in the linear region as they usually occupy less area. There are, however, two facts which must be taken into account (1) this possibility jeopardizes the linearity much more than with passive resistors and (2) the latest CMOS technologies not only provide conventional poly resistors, which usually need a much larger area, but also high resistivity resistors reducing the required area (and parasitic capacitance) considerably.

Once the feedback device is selected, the value of  $R_F$  must be chosen which practically equals the transresistance of the proposed TIA. One of the most important factors which should be taken into account is the range of possible photocurrents. This depends on the optical system, and more concretely, on the fiber and on the PD. A precise estimation of the amount of current is not easy. Nevertheless, a representative example is an optical system including glass fibers with lengths of around 300 m coupled with PDs like the QPDF-70 (QPhotonics) or C30616 (PerkinElmer) generating photocurrents of around  $10 \mu\text{A}$  biased with reverse voltages of 1 V (setting  $V_{PD} = V_{dd}$ ). This value of reverse voltage also guarantees large PD extrinsic bandwidths of around 8 GHz considering a load of  $50 \Omega$ . Another important factor is the output signal level which is directly dependent on the architecture. The architecture chosen here which consists of pre and post amplifiers allows the gain requirements to be split into two parts, which simplifies the design process. Taking this fact into account, the preamplifier must provide output levels of around 10 mV and the postamplifier around 100 mV, thus obtaining digital levels at the input of the CDR. From this, it follows that  $R_F$  must be in the order of 1 k $\Omega$ .

### 2.2 Noise analysis

The main noise contributors in a TIA are: the feedback resistor and obviously the active part. However, the feedback resistor has been optimized mostly for transresistance and, for

multiple Gb/s rates the noise dominant contributor is the amplifier [4]. For this reason, a detailed explanation regarding the amplifier noise optimization is required.

If, as in our case, the active part of the TIA comprises a high gain input stage, the noise is mainly determined by this first stage [5]. The device of the input stage with the strongest impact on the total noise contribution is  $M_N$ . We will therefore take a detailed look at the input referred noise generated by this input transistor.

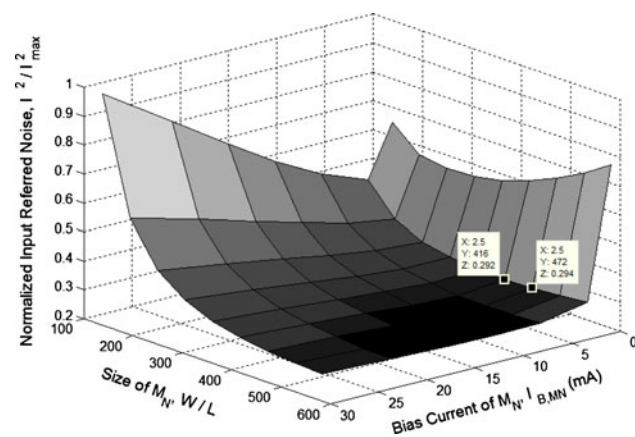
High frequency noise models for NMOS transistors incorporate three main contributors, all of which depend on the transistor geometry (W/L) and bias current ( $I_{B,MN}$ ). The first one is the thermal channel noise, which contributes most of the noise. The second one is the noise generated by the gate resistance, the origin of which is also thermal. The last contribution is induced by the coupling across the parasitic capacitances between the gate and the channel [7].

Computing the resulting expression of the input referred noise current of a NMOS transistor, and using the numerical data obtained from Cadence for each parameter, the normalized noise values as a function of W/L and  $I_{B,MN}$  are those shown in Fig. 3. These theoretical results demonstrate that if the width of the input transistor is larger than  $80 \mu\text{m}$  the noise dependence on the bias current is low. This is an interesting fact to achieve a good trade-off between noise and power consumption.

The definitive final values of  $M_N$  is  $W/L = 80/0.18$ ,  $I_{B,MN} = 2.5 \text{ mA}$ . The stage is biased with another high resistivity resistor  $R_1$  ( $400 \Omega$ ). The properties of  $M_{B1}$  are given in the following section.

### 2.3 Frequency analysis and compensation

Once the noise is optimized by proper biasing and sizing of the input transistor  $M_N$ , it is time to look into the

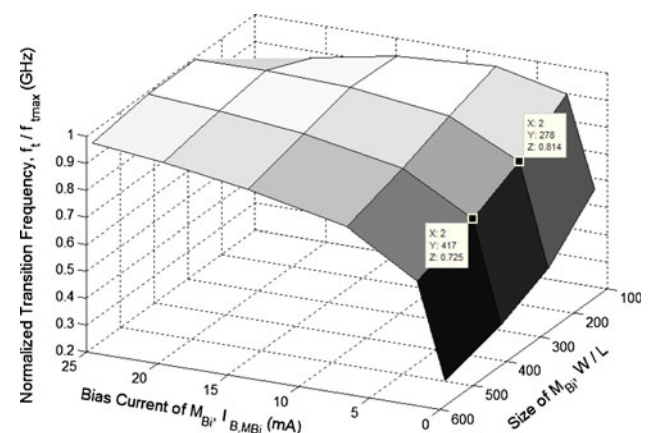


**Fig. 3** Normalized input referred noise.  $L = L_{\text{min}} = 180 \text{ nm}$  and  $I_{\text{max}} = 0.6 \text{ nA}/\sqrt{\text{Hz}}$ .  $I_{\text{max}}$  represents the maximum computed input referred noise current of a NMOS transistor at  $T = 27^\circ\text{C}$

bandwidth optimization. This goal is achieved in two complementary ways: (1) by an adequate choice of W/L and  $I_{B,Mi}$ , and (2) by considering frequency compensation.

One of the most characteristic parameters in CMOS technologies is the transistor transition frequency,  $f_t$ . This magnitude represents the maximum attainable operation frequency in a specific technology. Although the maximum oscillation frequency could be a more important parameter in a high-frequency amplifier design, the design with  $f_t$  becomes equivalent and simpler when no layout conditions are imposed. This makes the design process easier and more efficient.

The conventional definition of  $f_t$  was reported previously in [8]. A starting point for bandwidth optimization should be to set both, W/L and  $I_{B,Mi}$ , to those values at which the operating frequency coincides with the maximum value of the transition frequency,  $f_{\text{tmax}}$ . Computing the resulting  $f_t$  expression of a NMOS transistor, and using the numerical data obtained with Cadence for each parameter, the normalized  $f_t$  values as a function of W/L and  $I_{B,MN}$  are as shown in Fig. 4. These theoretical results show that if the  $I_{B,Mi}$  is higher than  $2 \text{ mA}$  the  $f_t$  improvement is low for any value of W/L and the bandwidth optimization via  $I_{B,MN}$  becomes ineffective. This analysis reveals that the best trade-off between bandwidth and power consumption is achieved by selecting the curve  $I_{B,M2,3} = 2 \text{ mA}$ . Simulations with Cadence showed optimal values of W/L ( $M_{B2}$ ) =  $W/L$  ( $M_{B3}$ ) =  $45/0.18$  and W/L ( $M_{B2,3}$ ) =  $90/0.18$ . The CG stage is biased with another high resistivity resistor  $R_2$  ( $750 \Omega$ ). The case of  $M_{B1}$  is not quite the same. The first stage must be fully optimized for noise, and this criterion prevails. For this reason the only parameter to be set is W/L because  $I_{B,MB1}$  already equals  $I_{B,MN}$ . The best frequency response obtained with iterative simulations is given by  $W/L$  ( $M_{B1}$ ) =  $45/0.18$ .



**Fig. 4** Normalized transition frequency.  $L = L_{\text{min}} = 180 \text{ nm}$  and  $f_{\text{tmax}} = 55 \text{ GHz}$

The second phase in the frequency optimization is by introducing frequency compensation. The proposal in this work is based on two different high frequency compensation techniques: phantom zeros and shunt-peaking [4, 5].

With architectures where the preamplifier is designed to have a fixed gain, the use of phantom zeros is one of the most efficient ways of frequency compensation. Essentially, a zero is created somewhere in the feedback loop at the edge of the passband. This zero is visible in the loop transfer function but not in the system transfer function. However, they are very useful because allow placing the system poles in convenient positions. The quantitative analysis of the proposed structure in the high frequency range is both highly complicated and ineffective. However, using a qualitative analysis and with the help of Cadence simulations, this work is made easier. Qualitatively, there are three critical nodes involved in the loop transfer function of the proposed structure: (1) at the input of the CS stage, (2) at the output of the CS stage and (3) at the output of the CG stage. Simulation results confirm this hypothesis showing three real dominant poles in the open-loop response of the voltage amplifier at 900 MHz, 1.5 GHz and 2.9 GHz. Therefore, at least two phantom zeros are required. Fortunately, one can be employed by including an integrated capacitor,  $C_{MIM} = 0.2$  pF, in parallel with  $R_F$  and the other by placing an inductor,  $L_{SMD1} = 43$  nH, in series with the PD. Fig. 5 shows their location.

Figure 6 gives the postlayout frequency response at each step of the design process. Initially, a peak appears in the transimpedance frequency response of the circuit without compensation. When  $C_{MIM}$  is included, the phantom-zero is designed to ensure stability. If  $L_{SMD1}$  is added to the circuit, the bandwidth is enlarged with no stability problems. In the same picture, the impact of the output stage, comprising the driver, bondpad and printed circuit board (PCB), is evaluated. These generate a high output capacitive load which reduces the bandwidth. This problem is

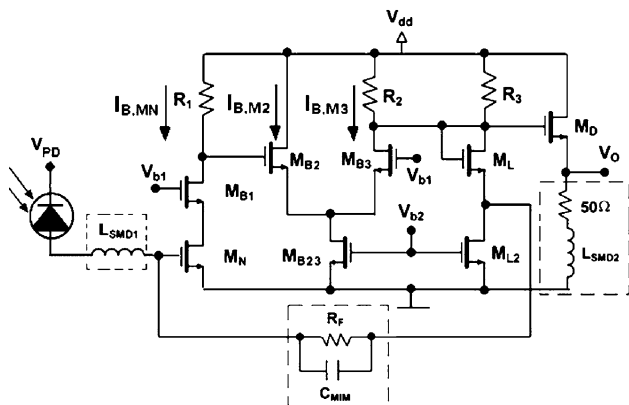


Fig. 5 Schematic of the TIA including the components used for frequency compensation

avoided by employing the shunt-peaking technique [3]. This is done with the inclusion of an inductor,  $L_{SMD2}$ , in series with the load resistor. Simulation results show that taking into account bonding and PCB parasitic devices,  $L_{SMD2}$  must equal 8.2 nH. Although this output stage deteriorates the frequency response, the definitive system will integrate all blocks in Fig. 1 without drivers. The reduction in the transresistance ( $T_R$ ) is also due to output matching.

### 3 Experimental results

The proposed preamplifier has been designed in a 0.18  $\mu$ m CMOS technology with a single supply voltage of 1.8 V. The chip photograph is shown in Fig. 7. The estimated active die area is 0.017 mm<sup>2</sup>. The prototype incorporates two electrostatic discharge (ESD) protection circuits. One is placed at the input and employs two diodes,  $D_1$  and  $D_2$ , see Fig. 8. These input diodes are needed, especially in deep-submicron technologies where the prototype can be destroyed easily due to ESD. They are designed for this purpose following a layout strategy for high-frequency I/O pads proposed in [9]. They have minimum size for a reduced parasitic capacitance (72 fF), thus protecting in an efficient way but with no visible effect on the frequency response. The other protection is placed between the power supply and ground terminals and is based on a very large grounded NMOS transistor,  $M_{ESD}$  ( $W/L = 100/1.5$ ) [10]. The bias voltages  $V_{b1} = 1.3$  V and  $V_{b2} = 0.6$  V are generated internally by using just one voltage divider branch which is shown depicted in the same picture. The die is wire bonded directly to the PCB.

Surface mounted devices (SMD) implement  $L_{SMD1}$  and  $L_{SMD2}$ . This choice is based on several practical aspects:

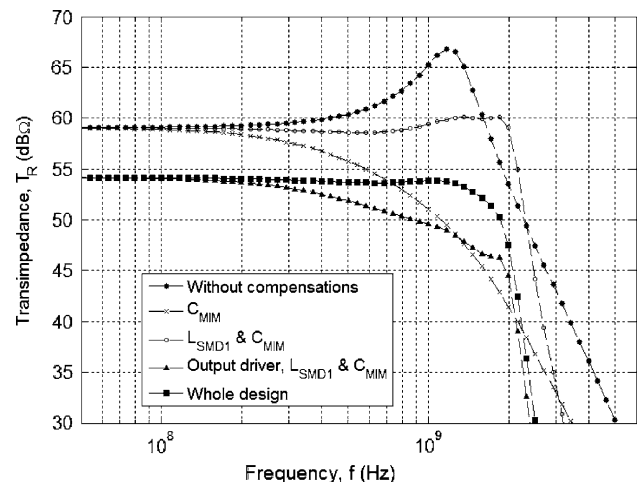
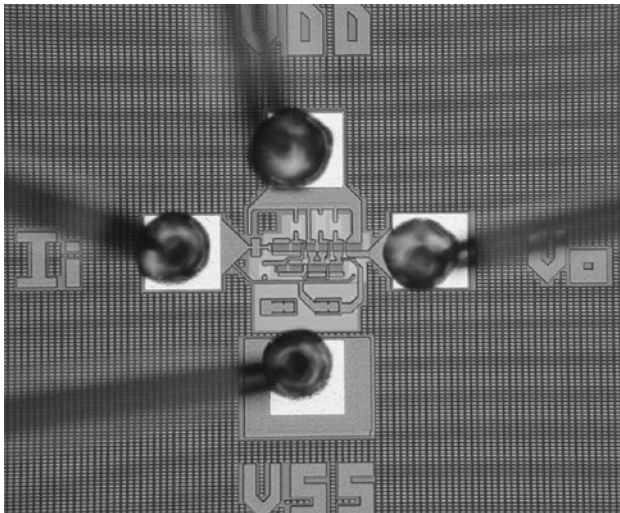
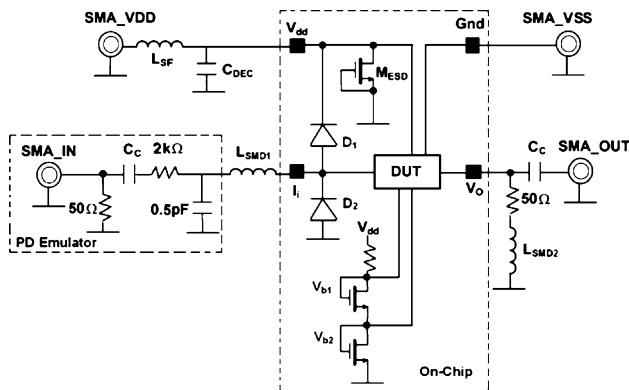


Fig. 6 Frequency response obtained when frequency compensation is employed



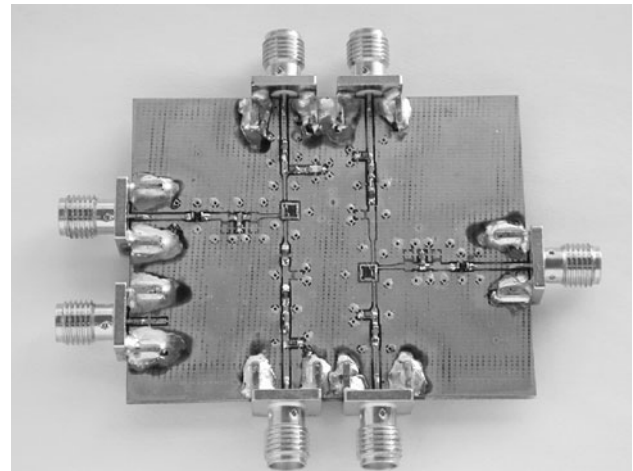
**Fig. 7** Die photo of the preamplifier. The active area equals  $130\ \mu\text{m} \times 136\ \mu\text{m}$



**Fig. 8** Schematic of the design testbench

(1) versatility of the test setup; the inductors can be changed easily by simple manipulation on the PCB and allows for including more test options monolithically, (2) lower cost of the test chips, since the sizes of the inductors are relatively high making the prototype more expensive and (3) recently published works, where high frequency performance designs are obtained with off-chip SMD inductors [11]. The main drawback when designing with this kind of devices is tolerance. Furthermore, we have checked via simulations that variations in the values of up to  $\pm 10\%$  of these inductors have a negligible effect on the frequency response.

Another important point is the strong dependence of both proposed frequency compensation techniques on the value of the PD parasitic depletion capacitance. In this work the PD has been emulated using a 0.5 pF parasitic capacitor laid out on the PCB. This value agrees with the parasitic capacitances at 1 V reverse bias in high speed photodiodes such as QPDF-70 or C30616. A 2 kΩ SMD resistor completes the PD model. This resistor is used as a



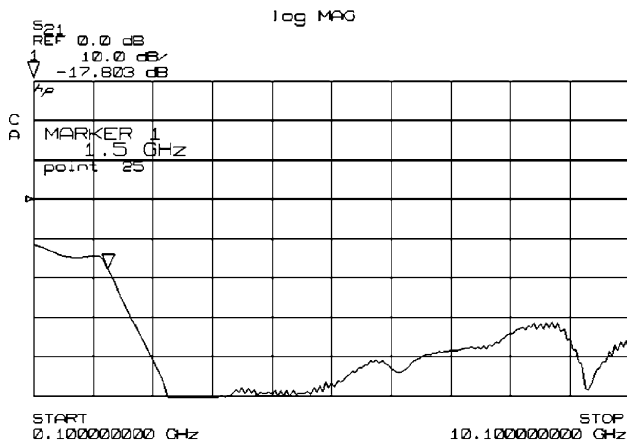
**Fig. 9** Photo of the PCB including preamplifier and calibration circuits. All circuit SMDs are 0603 encapsulated devices

V–I converter due to the fact of that our test equipment operates in voltage-mode instead of current-mode.

Two 22 nF ceramic capacitors, C<sub>c</sub>, are included for coupling. The supply filtering network involves a low-Q SMD RF choke inductor of L<sub>SF</sub> = 6.8 μH and another capacitor of 22 nF, C<sub>DEC</sub>. Fig. 9 shows a photograph of the PCB with the prototype and the external components. All DC and RF signals are introduced by using planar SMA connectors with a flat response of up to 18 GHz. This configuration reduces electromagnetic interference and minimizes insertion losses with little impact on the frequency response.

Figure 10 shows the results of an S-parameter analysis of the preamplifier measured with an HP 8510C/8517B vector network analyzer. Experimentally, the S<sub>21</sub> shows a magnitude of  $-17\ \text{dB}$  and an upper cut-off frequency of 1.5 GHz. The value of the magnitude seems low. However, the PD emulation resistor is introducing an important attenuation factor (in order to get coherent input current amplitudes) no de-embedded in the TOSM calibration process. For this reason, the test chipset and PCB include a second test circuit which allows obtaining the transresistance. This circuit provides an experimental transresistance of 58 dBΩ, validating the simulation expected value. Similarly, the comparison between the experimental and simulation results of the cut-off frequency shows good agreement. From here, an important indirect conclusion can be stated. If the experimental and simulation results with the output driver match, the experimental and simulation results without an output driver theoretically match as well. So, the real circuit bandwidth is around 2.2 GHz and this important conclusion must be taken into account in the design of the future monolithic receiver.

The eye diagrams for a 2.5 Gb/s 2<sup>31</sup>-1 pseudorandom non return to zero (NRZ) bit pattern with different input



**Fig. 10** Experimental S-parameters of the proposed circuit

currents are shown in Fig. 11. As the bit error rate tester (BERT) cannot provide output amplitudes lower than 250 mV, in order to check the sensitivity of the proposed preamplifier, attenuators of 10 dB and 20 dB (MiniCircuits S10W2 + and S20W2 +) with operating frequencies up to 18 GHz have been connected at the output of the BERT. The estimated input current amplitudes calculated from the test circuit with attenuators of 10 dB and 20 dB are 30  $\mu$ A and 10  $\mu$ A, respectively. All these eye diagrams have been obtained by using the Agilent BERT N4906A and the Agilent Infiniium DCA-J 86100C.

The results in Fig. 12 are the eye diagrams at different extreme bit rates (1 Gb/s and 3 Gb/s). In this case the eye diagrams are obtained at a constant input current amplitude of 10  $\mu$ A (20 dB attenuation). Under these conditions, the

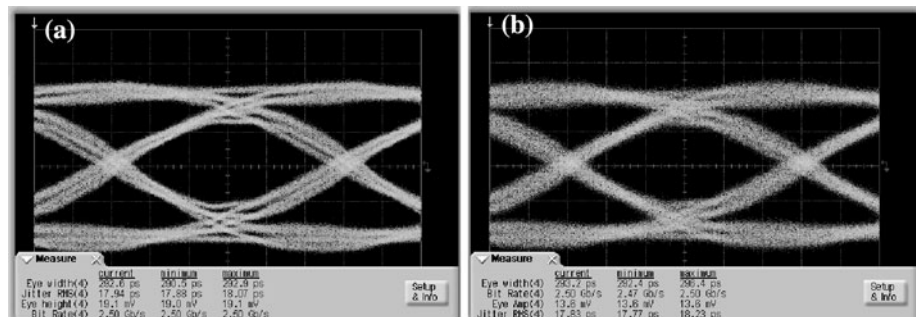
jitter is from 8 ps (when the bit rate is 1 Gb/s) up to 22 ps (when the bit rate is 3 Gb/s).

The same test equipment allows obtaining the results of Fig. 13. This plot presents the output noise distribution as a function of the 1/0 logical state. The results show an output rms noise of 267  $\mu$ V<sub>rms</sub> and 261  $\mu$ V<sub>rms</sub> when the states are 0 and 1 respectively.

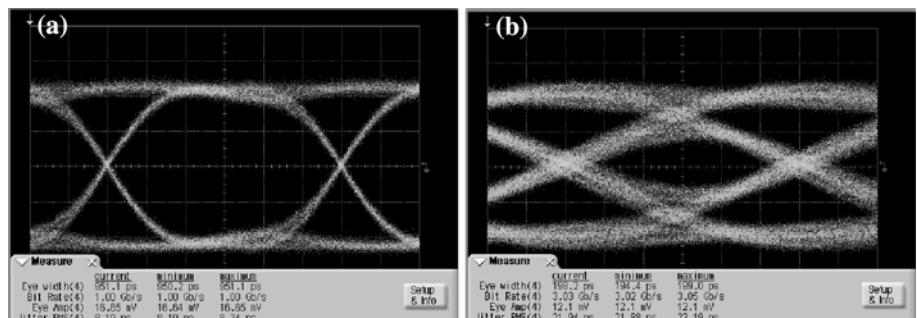
The BER response as a function of the input current is given in Fig. 14. These results show a BER = 10<sup>-12</sup> ( $I_{in} \geq 8.5 \mu$ A@2.5 Gb/s). Lower and higher bit rates have also been checked achieving a BER = 10<sup>-12</sup> ( $I_{in} \geq 5.5 \mu$ A @1.25 Gb/s) and a BER = 10<sup>-12</sup> ( $I_{in} \geq 9.5 \mu$ A@3.0 Gb/s).

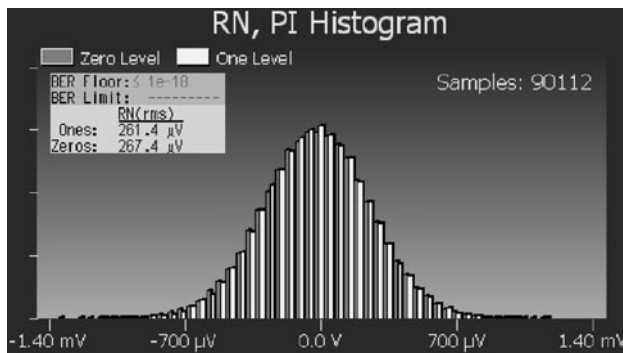
Table 1 summarizes the experimental results of the proposed topology and compares our structure with other recently published works in different CMOS technologies. The usual figure of merit in preamplifiers,  $\Gamma$ , is defined by the ratio of the product transresistance-bit rate and the product power-noise. A more advanced technology allows for reducing the power consumption and increasing the bandwidth, thus obtaining higher  $\Gamma$ . This fact must be taken into account when comparing the results of this work and those presented in [6] and [12]. The comparison shows a consistent performance evolution due to technology downscaling. Unfortunately, the authors in these two works provide no precise measurement of jitter or BER. But, taking into account the reported eye diagrams, the ratios jitter-bit rate seem to be higher than in any of our cases. On the other hand, although the topology in [13] is designed with the most recent technology, it has the lowest  $\Gamma$ . There are two reasons for this: (1) the larger power consumption caused by the use of a differential 3.3 V output driver and

**Fig. 11** Eye diagrams at 2.5 Gb/s and different input currents: **a** 30  $\mu$ A and **b** 10  $\mu$ A

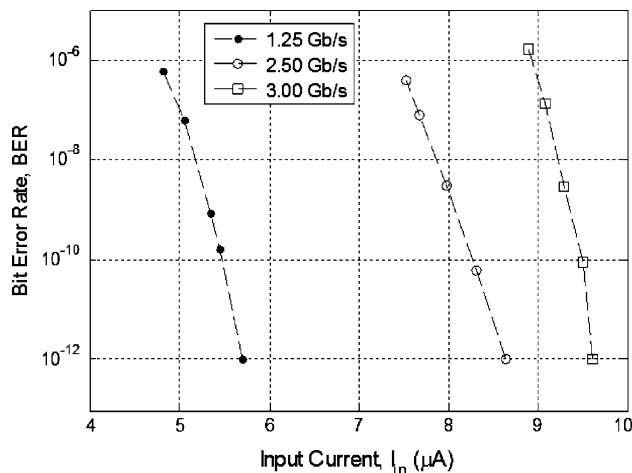


**Fig. 12** Eye diagrams at 10  $\mu$ A of input current amplitude and different bit rates: **a** 1 Gb/s and **b** 3 Gb/s





**Fig. 13** Output noise distribution as a function of the logical state. Input signal: 2.5 Gb/s NRZ bit pattern with 30  $\mu\text{A}$  input current



**Fig. 14** BER as a function of the input current and bit rate

**Table 1** Comparative analysis with other recently published works

Performance	[6]	[12]	[13]	This work
Technology (nm)	CMOS 350	CMOS 130	CMOS 90	CMOS 180
Supply voltage (V)	1.8	1.2	1.0	1.8
Power (mW)	27	2.2	184	24
Transresistance (dB $\Omega$ )	50–65	58	85	58
Bit rate (Gb/s)	1.25	8.0	2.5	2.5
Output rms noise (mV <sub>rms</sub> )	0.64	3.3	2.47	0.27
PD capacitance (fF)	500	400	500	500
Active area (mm <sup>2</sup> )	0.016	0.010	0.041	0.017
$\Gamma$ (Gb- $\Omega$ /mW-mV)	128	875	98	306

(2) the designer does not take advantage of the higher  $f_t$  of this technology. If we sum up all points in this discussion the conclusion is that the proposed design in this work exploits all the benefits of the CMOS technology employed, achieving a high performance design and obtaining a competitive block against other recently published.

## 4 Conclusions

This work has presented a preamplifier intended for fiber-optic receivers. Low-cost is one of the most important advantages of our proposed preamplifier thanks to the use of cheap CMOS technology. A good trade-off between gain, noise, bandwidth and power consumption has been achieved leading to a high performance design. These characteristics make the proposed block a preferential option for LANs where all these characteristics are critical design criteria.

More concretely, the preamplifier is based on a resistive shunt-feedback topology and employs two different frequency compensation techniques, phantom zeros and shunt-peaking. The circuit is designed in a 1.8 V 0.18  $\mu\text{m}$  CMOS process. Experimental results report a value for the transresistance of 58 dB $\Omega$  and a bandwidth of 1.5 GHz, respectively. Eye diagrams obtained at 2.5 Gb/s show a total jitter of 18 ps and a BER of  $10^{-12}$  when  $I_{in} \geq 8.5 \mu\text{A}$ . Higher bit rates of up to 3 Gb/s have also been tested achieving a BER of  $10^{-12}$  when  $I_{in} \geq 9.5 \mu\text{A}$ . The power consumption and die active area are 23.7 mW and 0.017 mm<sup>2</sup>, respectively.

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