



Development of neural networks chip generating driving waveform for electrostatic motor

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Abstract

The authors are studying hardware neural networks (HNN) to control the locomotion of the microrobot. The neural networks chip is the integrated circuit chip of the HNN. We proposed the electrostatic motor that is the new actuator of the microrobot in our previous research. The electrostatic motor used the waveform generator to generate the driving waveform. In this paper, the authors will propose the driving circuit using neural networks chip. The cell body model is the basic component of the neural networks chip that outputs 3 MHz frequency of electrical oscillated pulse waveform. Therefore, large capacitors need to connect outside of the neural networks chip to generate the low-frequency driving waveform. The proposal neural networks chip generates a long delay without using large capacitors. In addition, the neural networks chip generated a two-phase anti-phase synchronized waveform by incorporating a mechanism for adjusting synaptic weight. As a result, the proposal neural networks chip can generate the electrostatic motor's driving waveform with variable frequency. The frequency of the driving waveform could vary from 40 to 126 Hz.

Keywords Electrostatic motor · Hardware neural networks · Integrated circuit · MEMS · Microrobot

1 Introduction

Insects have an excellent function. Although insects are small bodies, they perform external recognition through vision and touch. In addition, insects respond to the external environment with excellent control. Insects have a brain, muscles, sensory organs, and energy sources in small bodies.

If the autonomous robots need to be small as insects, each component has to miniaturize. The microrobots are expected to search for a small place where people cannot enter. The centimeter-sized robot "HAMR" developed by Harvard University is equipped with a control circuit and a power supply to achieve independent walking [1]. In addition, the millimeter-sized robot developed by the University of Maryland has successfully walked using an external magnetic field [2]. However, miniaturization of a power supply, sensors, a control circuit, and actuators are a difficult subject [3].

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Programming control by microcontrollers is the dominant system for robot control. On the other hand, insects have excellent sensory information processing and body control, enabling them to adapt to various environments despite their small size [4]. Therefore, research on applying the control method of biological neural networks to robots is conducted [5]. Information processing methods that mimic living organisms have the potential to create simple and compact systems.

The authors are studying hardware neural networks (HNN) [6–10]. The neural networks chip and the body parts of the microrobot were both made by a silicon wafer. The neural networks chip can integrate directly into the body parts of the microrobot. The development of neural networks chip has an advantage because microcontrollers need to mount on a circuit board.

Previously, our constructed microrobot system succeeded to perform walking using an external power supply [7]. The neural networks chip generates the gait pattern of the microrobot. The neural networks chip is the integrated circuit chip of the HNN. A shape memory alloy (SMA) actuator is used for driving the legs of the microrobot. SMA actuator has a large generating force and is simple and easy to miniaturize. However, the power consumption was high. Therefore, we developed an electrostatic motor as a new actuator [11]. Replacing the SMA actuator with the electrostatic motor can achieve a low power consumption of 60 V drive. The microrobot can also drive by solar cells. A variable frequency square waveform is required to drive the electrostatic motor. A waveform generator has been used to generate the driving waveform of the electrostatic motor. Therefore, we proposed HNN to generate the driving waveform of the electrostatic motor to miniaturize the microrobot system [12]. In the simulation result, the HNN generated the driving waveform of the electrostatic motor. In addition, we fabricated the neural networks chip. The neural networks chip successfully generated pulses with a variable frequency (around 50–100 Hz). However, the neural networks chip could not generate a two-phase waveform with anti-phase synchronization [13].

In this paper, the authors will propose the neural networks chip that introduced a variable inhibitory-synaptic model. The two-phase waveforms can synchronize as anti-phase by adjusting the synaptic weight. In addition, we will discuss the measuring result of the neural networks chip.

2 Microrobot system

2.1 Microrobot

Figure 1 shows our previously proposed microrobot system [7]. The external dimensions are 4.6 mm × 9.0 mm × 6.4 mm.

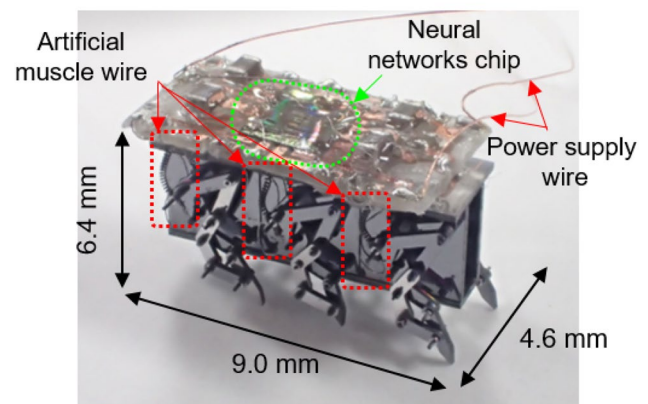


Fig. 1 Microrobot system [7]

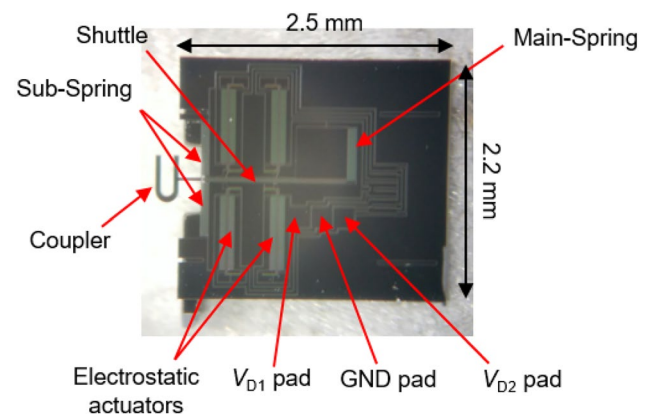


Fig. 2 Electrostatic motor [11]

Each part of the robot was manufactured using micro-electro-mechanical systems technology. The SMA actuator drives the microrobot. The neural networks chip mounted on the robot can generate a gait pattern of the microrobot. The neural networks chip realizes miniaturization and weight reduction of the microrobot.

2.2 Electrostatic motor

Figure 2 shows our previously proposed electrostatic motor [8]. The size of the electrostatic motor was 2.2 mm × 2.5 mm. The electrostatic motor consists of two pairs of electrostatic actuators, a central shuttle, arms, sub-springs, a main-spring, and three-electrode pads, V_{D1} , V_{D2} , GND. The arms transmit the force of the electrostatic actuators. The electrostatic motor produces linear motion of the shuttle by energizing the electrodes. Sub-springs and main-spring return the shuttle to the primary position. The electrostatic motor outputs more than 1.3 mN that is suitable to actuate the microrobot's legs.

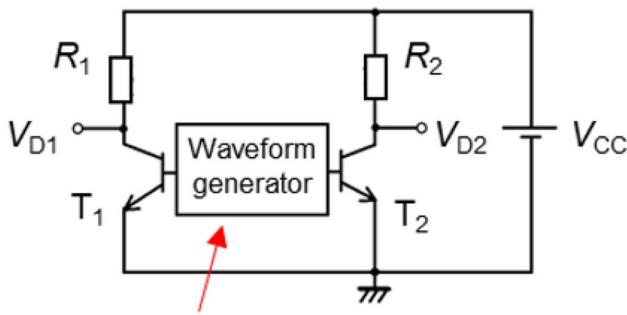


Fig. 3 Circuit diagram of driving circuit [11]

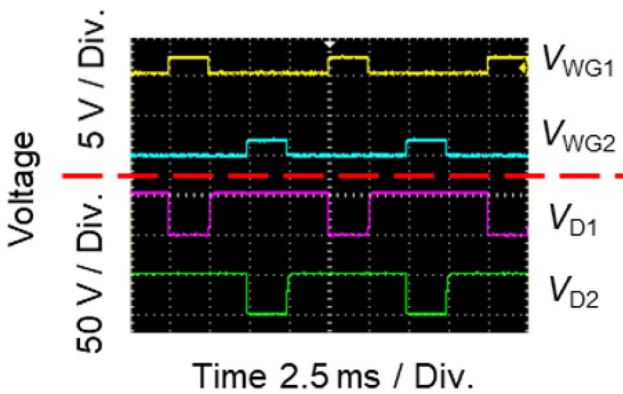


Fig. 4 Driving waveform of electrostatic motor

Figure 3 shows a circuit diagram of the driving circuit of the electrostatic motor. The circuit parameters are $R_1 = R_2 = 2.2 \text{ M}\Omega$, $V_{CC} = 60 \text{ V}$.

Figure 4 shows the driving waveform of the electrostatic motor (V_{D1} , V_{D2}). The driving waveform has a pulse width of 7.5 ms, a pulse period of 10 ms, and an amplitude of 60 V. The driving waveform is generated by switching the transistor using a waveform generator. In Fig. 4, V_{WG1} and V_{WG2} are waveforms generated by the waveform generator. The authors will replace the waveform generator with the neural networks chip in this paper.

2.3 Previous neural networks chip

Previously, we have shown that the neural networks chip can generate the drive waveform of the electrostatic motor shown in Fig. 4. using HSPICE simulations [12]. However, the fabricated neural networks chip’s measured results could not perform the two-phase anti-phase synchronized waveform. The reason is the synaptic model that synchronizes the two anti-phase outputs did not work correctly due to parasitic capacitance [13]. Therefore, in this paper, we fabricated a neural networks chip with an additional mechanism to change the synaptic model’s weight. The following sections provide details.

3 Neural networks chip

Figure 5 shows the schematic diagram of the constructed neural networks chip. The neural networks chip consists of four elements: the cell body model, excitatory-synaptic model, inhibitory-synaptic model, and variable inhibitory-synaptic model. Each component of the neural networks chip is described in Sect. 3.1.

Figure 6 shows the circuit diagram of the constructed neural networks chip. The circuit parameter is as follows. MOSFET: $M_{ax}, M_{bx} = W/L = 1.2 \mu\text{m}/8.5 \mu\text{m}$, $M_{bx} = 1.2 \mu\text{m}/10 \mu\text{m}$, $M_{cx}, M_{dx} = 10 \mu\text{m}/1.2 \mu\text{m}$, $M_{ex}, M_{fx}, M_{gx}, M_{hx}, M_{ix}, M_{jx}, M_{lx}, M_{V11}, M_{V21}, M_{V31}, M_{V41}, M_{V51}, M_{V12}, M_{V22}, M_{V32}, M_{V42}, M_{V52} = 10 \mu\text{m}/10 \mu\text{m}$, $M_{ky} = 2 \mu\text{m}/10 \mu\text{m}$, $M_{V61}, M_{V62} = 10 \mu\text{m}/20 \mu\text{m}$, capacitor: $C_{Gx} = 1 \text{ pF}$, $C_{Mx} = 0.1 \text{ pF}$, $C_{Sx} = 8 \text{ pF}$, Power-supply voltage: $V_A = 3.43 \text{ V}$, $V_{DD} = 3.36 \text{ V}$, $V_{AS} = 0.80 \text{ V}$, $V_{int} = 1.90 \text{ V}$, $V_W = 1.95 \text{ V}$ ($x = 1, 11, 12, 2, 21$, and 22 , $y = 1, 11, 2$, and 21 , $z = 11, 12, 21$, and 22).

3.1 Hardware neuron model

3.1.1 Cell body model

In Fig. 6, "Self-OSC 1, Self-OSC 2, S_{11} , S_{12} , S_{21} , and S_{22} " shows the cell body model. The circuit consists of capacitors: C_{Gx}, C_{Mx} , MOSFET: $M_{ax}, M_{bx}, M_{cx}, M_{dx}$, voltage source: V_A, V_{AS}, V_{DD} . The cell body model is an oscillation circuit that outputs pulses. The cell body model can switch between "self-excited oscillating mode" and "separately-excited oscillation mode" by varying the voltage source V_A . A self-oscillating cell body model oscillates at 3 MHz. The cell body model switches to separately-excited oscillation mode by lowering V_A to 0.5–1.5 V. The power supply voltage V_A of the separately-excited oscillation cell body model indicated as V_{AS} . The separately excited oscillation cell body model oscillates pulses according to the oscillation of other cell body models.

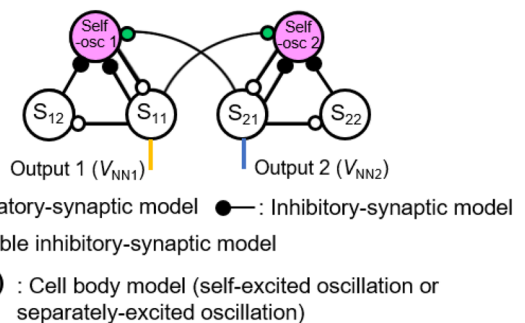


Fig. 5 Schematic diagram of the neural networks chip

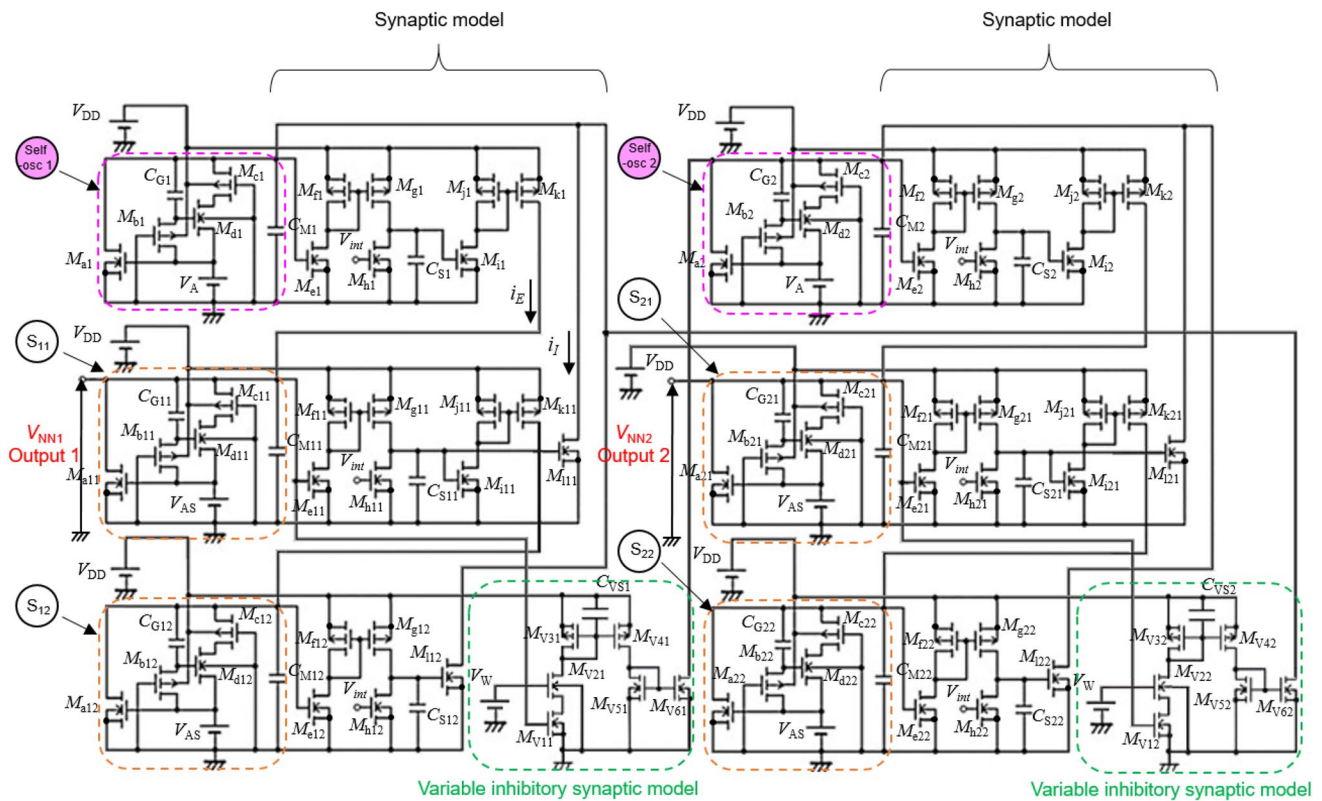


Fig. 6 Circuit diagram of the neural networks chip

3.1.2 Synaptic model

The synaptic model mimics the characteristics of the biological synapse. Synapse is a connection part between the cell body. The synaptic model consists of MOSFET: M_{ex} , M_{fx} , M_{gx} , M_{hx} , M_{ix} , M_{jx} , M_{kx} , M_{lx} , capacitor: C_{Sx} , voltage source: V_{DD} , V_{int} . In Fig. 6, " i_E " is transmitted as an output signal by an excitatory-synaptic model to the post-cell body model. By connecting the excitatory-synaptic model, the pre-cell body model excites the post-cell body model. Therefore, both cell body models will oscillate with in-phase synchronization. On the other hand, " i_I " is transmitted as an output signal by the inhibitory-synaptic model to the post-cell body model. The inhibitory-synaptic model inhibits the oscillation of the post-cell body model. Therefore, both cell body models will oscillate with anti-phase synchronization. In Fig. 6, green dotted line shows the circuit diagram of the variable inhibitory-synaptic model. The variable inhibitory-synaptic model consists of MOSFET: M_{V1} (M_{V11} , M_{V12}), M_{V2} (M_{V21} , M_{V22}), M_{V3} (M_{V31} , M_{V32}), M_{V4} (M_{V41} , M_{V42}), M_{V5} (M_{V51} , M_{V52}), M_{V6} (M_{V61} , M_{V62}), capacitor: C_{VS} (C_{VS1} , C_{VS2}), voltage source: V_{DD} , V_W . The variable inhibitory-synaptic model has the same function as the synaptic model concerning the function to inhibit. The variable inhibitory-synaptic model can vary the synaptic weight by varying the voltage V_W .

3.2 Mechanism of the hardware neural networks

If the self-oscillating cell body model (Self-OSC 1) is not connected with the other cell body model, the Self-OSC 1 oscillates at 3.0 MHz. The separately-excited oscillation cell body model S_{11} and S_{12} are the delay circuit. The delay mechanism is as follows.

1. Self-OSC 1 oscillates a pulse.
2. The pulse of Self-OSC 1 excites the S_{11} .
3. S_{11} oscillates a pulse.
4. The pulse of S_{11} inhibits the Self-OSC 1. It also excites the S_{12} .
5. S_{12} oscillates a pulse.
6. The pulse of S_{12} inhibits the Self-OSC 1.

As a result, Self-OSC 1 could not oscillate a pulse during the inhabitation from S_{11} and S_{12} .

Figure 7 shows an example of a generated waveform of neural networks chip. Figure 7 shows that the mechanism worked, the pulse period increased and the pulse width increased. In addition, S_{11} and S_{21} inhibit Self-OSC 1 and Self-OSC 2, respectively. Thus, the output of HNN V_{NN1} and V_{NN2} will be an anti-phase waveform.

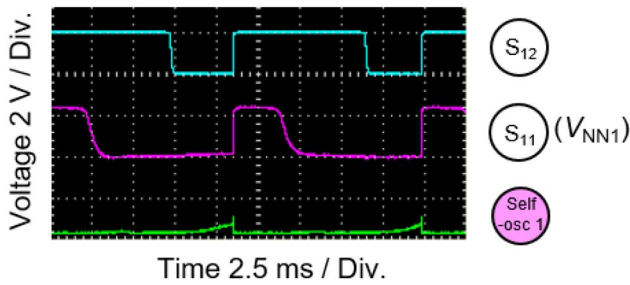


Fig. 7 Delay mechanism (example of a generated waveform of the neural networks chip)

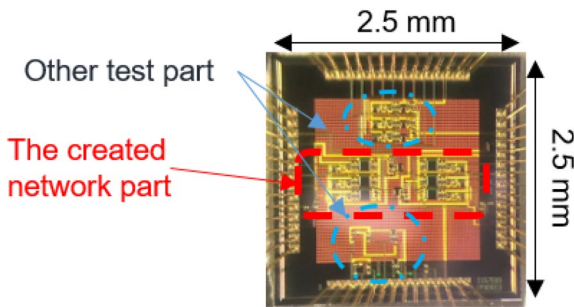


Fig. 8 Fabricated neural networks chip

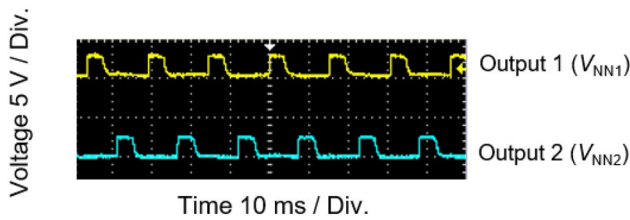


Fig. 9 Example of a generated waveform of the neural networks chip

3.3 Layout

Figure 8 shows the photograph of the fabricated neural networks. A red dotted line indicates the constructed HNN, where the other part is the test element. An IC chip’s size is 2.5 × 2.5 mm. 14 electrode pads used as V_A , V_{AS} , V_{DD} , V_{int} , V_W , V_{NN1} (output 1), V_{NN2} (output 2), and GND for the created network part.

4 Measurement result

Figure 9 shows the example of the generated waveform of neural networks chip. The voltage of the circuit is as follows. $V_A = 3.43$ V, $V_{AS} = 0.80$ V, $V_{DD} = 3.36$ V, $V_{int} = 1.90$ V, $V_W = 1.95$ V. Both of the waveform

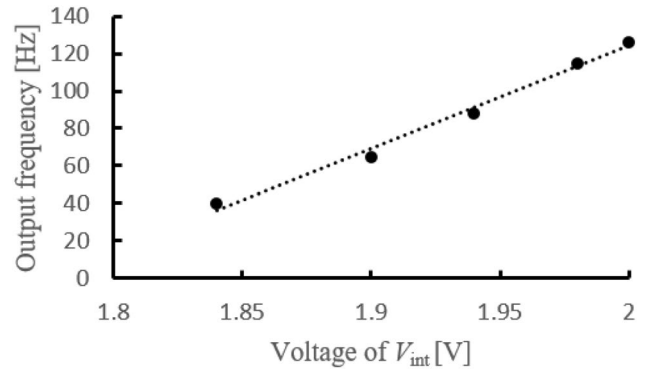


Fig. 10 Output-frequency characteristic of neural networks chip (Varying V_{int})

Table 1 Characteristics of V_{int} and V_W that output anti-phase synchronization

V_{int} (V)	V_W (V)	Frequency (Hz)
1.84	1.83	40
1.90	1.95	65
1.94	2.05	87
1.98	2.18	114
2.00	2.29	126

frequencies are 65 Hz. As shown in Fig. 9., the neural networks chip output a two-phase waveform with anti-phase synchronization.

Figure 10 shows an output-frequency characteristic of neural networks chip by varying V_{int} . The plots show the example measurement points. The frequency can be varied linearly from 40 to 126 Hz. In Fig. 10, the voltage of the circuit is as follows. $V_A = 3.43$ V, $V_{AS} = 0.80$ V, $V_{DD} = 3.36$ V, $V_{int} = 1.90$ V. V_{int} is a voltage that determines the degree of delay in the synaptic model with a pulse delay function. Each plot in Fig. 10 is data when antiphase-synchronized waveforms are generated by adjusting the voltage V_W of the variable inhibitory-synaptic model.

Table 1 shows the characteristics of V_{int} and V_W in Fig. 10. A varying only voltage of V_{int} does not output an anti-phase synchronized waveform. By adjusting V_W as shown in Table 1, the two pulse outputs synchronize with anti-phase. The accuracy required for the voltage V_W is ± 10 mV.

As a result of the neural networks chip measurement, the fabricated neural networks chip generated a two-phase waveform with anti-phase synchronization. The output frequency can be varied from 40 to 126 Hz by changing V_{int} . When the frequency is varied, a two-phase waveform with anti-phase synchronization can be generated by adjusting the voltage V_W .

5 Conclusion

In this paper, the authors developed the neural networks chip that incorporates a mechanism to adjust the synaptic weight. As a result, the proposal neural networks chip generated the electrostatic motor's driving waveform with variable frequency. The frequency of the driving waveform could vary from 40 to 126 Hz.

In the future, we will experiment with driving the electrostatic motor using the neural networks chip. In addition, we will propose the microrobot system using the electrostatic motor.

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