First comparison of the electrical properties of two grid emulators for UVRT test against field measurement

Anica Frehn¹ · Soroush Azarian² · Gesa Quistorf² · Stephan Adloff³ · Fritz Santjer⁴ · Antonello Monti¹

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Abstract

The technical rules for connecting turbines to the medium, high or extra-high voltage grid in Germany require the certification of the UVRT characteristics of wind turbines. The state-of-art voltage divider-based test equipment, also named UVRT-Container, is well equipped for executing UVRT tests in field. To conduct the UVRT in field the full wind turbine should be already installed. A second option to perform UVRT tests are system level test benches. They enable the testing of the nacelle. The components that are not actually present, such as the turbine tower or the blades, are emulated via a mechanical hardware in the loop (HiL) system. In this work, for the first time, the performance of two different grid simulators installed at the DyNaLab at Fraunhofer IWES and at the CWD at RWTH Aachen University is compared with a field measurement of the same type of wind turbine. Thus, not only a system test bench measurement is compared to a field measurement. Rather, two system test benches with individual technical approaches are additionally compared with each other. The focus of this work is to investigate the characteristics of the grid simulators within the steady-state range of the UVRT tests to replicate identical fault shapes on the test benches and in the field.

Erstmalige Gegenüberstellung der elektrischen Eigenschaften zweier Netzemulatoren und deren Vergleich mit einer Feldmessung bei der Durchführung von UVRT Tests

Zusammenfassung

Die technischen Regeln für den Anschluss von Anlagen an das Mittel-, Hoch- oder Höchstspannungsnetz in Deutschland erfordern die Zertifizierung der UVRT-Eigenschaften von Windenergieanlagen. Stand der Technik ist die Durchführung der UVRT Tests im Feld mit einer passiven, spannungsteilerbasierten Prüfeinrichtung (auch UVRT Container genannt). Hierfür ist vorab die komplette Windenergieanlage im Feld zu installieren. Eine zweite Möglichkeit zur Durchführung von UVRT-Tests sind Prüfstände auf Systemebene. Sie ermöglichen die Prüfung der Gondel. Die nicht tatsächlich vorhandenen Komponenten, wie der Turbinenturm oder die Rotorblätter, werden über ein mechanisches Hardware in the Loop (HiL)-System emuliert. Es erfolgt nicht nur ein Vergleich zwischen Prüfstand- und Feldmessung, vielmehr werden zusätzlich zwei Systemprüfstände mit individuellen technischen Ansätzen gegenübergestellt. Hierzu werden erstmals die Leistung von zwei verschiedenen Netzemulatoren, die am DyNaLab des Fraunhofer IWES und am CWD der RWTH Aachen University installiert sind, mit einer Feldmessung desselben Anlagentyps verglichen. Der Fokus dieses Papers liegt auf der Untersuchung der Eigenschaften der Netzemulatoren im stationären Bereich der UVRT-Tests, um identische Fehlerformen auf den Prüfständen und im Feld nachzubilden.

✉ Anica Frehn
afrehn@eonerc.rwth-aachen.de

¹ Center for Wind Power Drives, RWTH Aachen University, Aachen, Germany

² DyNaLab Bremerhaven, Fraunhofer Institute for Wind Energy Systems, Bremerhaven, Germany

³ Wobben Research and Development GmbH Aurich, Aurich, Germany

⁴ UL International GmbH, Wilhelmshaven, Germany

1 Introduction

Fault Ride Through (FRT) is one of the most critical electrical tests for wind turbine grid compliance testing. A voltage divider based method called UVRT container is the state of the art for performing UVRT tests in the field. The point of common coupling (PCC) of the wind turbine is located at the medium voltage grid [2, 3]. System test benches provide the functionality to perform the electrical tests required for certification in a laboratory environment using multi-megawatt grid simulators. In addition, grid simulators used at the test benches provide the capability to investigate research topics related to new grid integration challenges and requirements. System test benches provide the opportunity to accelerate testing and reduce time to market. Field testing relies significantly on environmental conditions that cannot be controlled. Instead, system test beds create a fully controlled environment through the use of a hardware-in-the-loop (HiL) platform [4].

System test benches are equipped with controllable converter-based grid simulators to expose the wind turbine nacelles to various grid events, such as voltage dips, frequency changes, and so on. On the other hand, it is important to represent grid parameters that are comparable to field measurements. For UVRT tests, not only the dip depth, the change in voltage angle and the duration of the fault need to be simulated at the test bench, but also the grid parameters at the wind turbine PCC. These are simulated in power hardware-in-the-loop (PHiL) setups.

This paper shows for the first time a comparison of two different test benches with a field measurement. The two test benches are the DyNaLab at Fraunhofer IWES in Bremerhaven and the CWD at RWTH Aachen. Both test benches have the possibility to set an artificial grid impedance at the PCC of the wind turbine. While the impedance specification at the DyNaLab maps the behavior of the UVRT container, at the CWD only the field impedance during the fault is specified. The correct specification of the phase angle jump during two-phase voltage dips is the second important factor that has to be considered

in order to reproduce the FRT behavior on test benches. The comparison of the measurements shows that under the above mentioned conditions it is possible to reproduce the UVRT behavior of the Enercon E-115 E2 measured in the field on both test benches.

2 Test setup and requirements.

The UVRT tests are performed according to the requirements of IEC 61400-21-1 and FGW TR3 Rev. 25. The field measurement can be considered as state of the art. The voltage dips in the field are generated using the voltage divider-based test equipment [5]. Both test benches use an inverter-based grid simulator to generate the voltage dips. In this section, the two test benches are introduced and their distinguishing features are highlighted. Subsequently, the Enercon E-115 E2 is described as device under test (DUT). Finally, the requirements for UVRT testing according to [2] and [3] are presented.

2.1 Field measurement

The reference for the comparison is the measurement of the WEC in the field. For the UVRT tests, a voltage dip generator based on the voltage divider principle (UVRT container) is connected between the turbine and the PCC. The PCC voltage is 20 kV. The pre-fault and post-fault grid impedance is 1.75Ω with a grid impedance angle of 73.3° .

The objective of the paper is to compare the UVRT tests at three test facilities (field, DyNaLab, CWD) under identical grid parameters. For this reason, the impedance resulting from switching on the series and short-circuit impedances of the UVRT container is the input variable for the virtual impedance specification at the two test benches. The set series and short-circuit impedances at the UVRT container are shown in Table 1 as a function of the dip depth.

Table 1 Serial and short circuit impedances at the UVRT container

Fault type	Voltage level in pu	Serial impedance R in Ω	Serial impedance jX in Ω	Short circuit impedance R in Ω	Short circuit impedance jX in Ω
3 ph	0.00	1.63	26.94	0.01	0.01
	0.25	1.72	26.96	0.77	9.49
	0.47	1.60	26.97	1.64	25.52
	0.73	1.61	27.05	4.51	77.98
2 ph	0.00	1.47	27.15	0.01	0.01
	0.25	1.47	27.25	0.81	9.51
	0.47	1.40	26.91	1.61	25.41
	0.73	1.31	27.05	4.51	77.98

Fig. 1 CWD RWTH Aachen test setup

Fig. 2 Fraunhofer IWES DyNaLab test setup

2.2 Test benches

The main functions of the electrical power system in the laboratory environment are, firstly, the conversion of the electrical power supplied by the grid into mechanical power and thus the rotation of the DUT and, secondly, the controlled recovery of the energy generated by the DUT (minimization of electrical consumption). Both test benches operate according to a comparable scheme. A direct drive supplies the wind turbine with the necessary torque. The medium-voltage side of the wind turbine is connected to the grid simulator. On the one hand, this provides the artificial, electrical grid. On the other hand, the power is fed back via the DC link to which both the grid simulator and the converter of the direct drive motor are connected.

CWD at RWTH Aachen University

Fig. 1 shows the test setup at the 4 MW system test bench at CWD, RWTH Aachen University. The prime mover has a rated output power of 4 MW at a torque of 3.4 MNm. It is connected to the Load Application System (LAS) with five additional degrees of freedom. The wind turbine is operated in a Hardware-in-the-loop (HIL) manner, to allow the wind turbine's main control to operate as in the field [4]. The medium voltage output side of the transformer of the DUT is either connected to the public grid or to the grid simulator. The public grid has a nominal voltage of 10 kV. The nominal voltage at the grid simulator is 20 kV. The maximum short circuit power of the grid simulator is 17 MVA (21 MVA) with a maximum output power of 6 MW [6].

Table 2 Data of the DUT

Manufacturer	Enercon GmbH
Type	E-115 E2
Nominal apparent Power S_N	3200 kVA
Nominal Active Power P_N	3200 kW
Nominal reactive power Q_N	2050 kvar
Nominal Voltage at low voltage side U_N	400 V
Rated Current $I_N = \frac{S_N}{\sqrt{3}U_N}$	4619 A
Maximum overcurrent $I_{\max}$	1.2 I_N
Grid Voltage at PCC U_G	20 kV

DyNaLab at Fraunhofer IWES

An overview about the electrical power system at the DyNaLab at Fraunhofer IWES is shown in Fig. 2.

The prime mover with an output power of 10/15 MW supplies the required torque to the DUT in mHiL (mechanical Hardware-in-the-Loop) configuration [7]. The medium voltage side of the DUT transformer is connected to the junction box. This is also the location of the sensors for medium voltage side current and voltage measurement. DyNaLab offers the possibility to test on the grid simulator as well as on the public grid. The dynamic grid tests are performed with the grid simulator. It has a short-circuit power of 44 MVA and a maximum output power of 15 MW. Various grid voltages between 10 and 36 kV can be emulated. The Enercon E-115 E2 is connected to a PCC voltage of 20 kV.

2.3 Device under test

The DUT is an Enercon nacelle type E-115 E2. The E-115 E2 has a rated power of 3.2 MW and consists of a syn-

Fig. 3 Voltage dip tolerance [2]

chronous generator, which is driven by the rotor via a direct drive. Since the speed of the synchronous generator is equal to the rotor speed, the output of the synchronous generator is adapted to the output frequency and output voltage via an IGBT full converter and a transformer. The same nacelle is used on both test benches. It is initially located at DyNaLab and will be transported to the CWD in Aachen after the test series at IWES. The field measurements will be carried out with a similar type of nacelle. Table 2 shows the relevant data of the E-115 E2.

2.4 Standards and technical guidelines

National and international standards provide guidelines for measuring and evaluating the electrical characteristics of wind turbines. In this chapter, a short overview of the international standard IEC 61400-21-1 [2] and the German national guideline FGW TR3 [3] is presented.

Both [2] and [3] define the same tolerance for the positive sequence voltage during a UVRT test, which is shown in Fig. 3.

The evaluation of positive and negative sequences shall be carried out by calculating the fundamentals Fourier coefficient over one fundamental period [2, 3]. The evaluation is always performed using the measured phase-to-neutral voltage. If the phase-to-phase voltage is measured, [2] provides an equation for calculating phase-to-neutral voltage. According to [2] the minimum sample rate of measurement should be 2 kHz. Where [3] suggest 3 kHz. In practice the sample rate of measurement is set to be minimum 10 kHz.

Both standard and guideline have defined the power phasor diagram. Positive direction of instantaneous voltage and current shall be considered. Both active and reactive power are positive for evaluation. The sign convention is called generator connection [2, 3].

3 Requirements for grid simulators to perform UVRT tests

To emulate a realistic voltage dip in laboratory environment, the grid simulator must fulfill special requirements. In addition to the standard test conditions of [3], the following requirements apply to LVRT tests [3]:

- Voltage dip tests for two- and three-phase dips up to a dip depth of less than 5% U_n .
- Performing voltage tests according to the limits specified in FGW TR3 regarding the fault depth and the corresponding fault duration.
- Short circuit ratio of at least $2 S_N$ at the WEC before the voltage dip
- The X/R ratio of the impedances used must be at least 3

Fig. 4 Variable R and X impedance emulation

- The voltage in the positive sequence of the open circuit test must conform to Fig. 3
- The test equipment must be designed to accept the maximum peak short-circuit current of the WEC
- The test equipment must be capable to perform two-phase tests with different phase conductors.

In addition to the requirements already described in the standards and technical guidelines, the emulation of the grid impedance and the mapping of two-phase faults are identified as further specifications in the CertBench research project. CWD and DyNaLab test bench are equipped with two different grid simulators and two different virtual impedance emulation methods.

3.1 Virtual impedance emulation

Virtual impedance emulation by use of multi-megawatt converter-based grid simulator has been reported in [8].

The impedance can be emulated in a closed loop system. Fig. 4 shows the single-phase equivalent circuit, which is intended to demonstrate the virtual grid impedance matching. In this case the nominal grid voltage is set to be U_{grid} , the emulated impedance will result in additional voltage in closed loop system U_Z .

$$U_Z = I_{pcc} \cdot \sqrt{(Z_x^2 + Z_R^2)} \quad (1)$$

Then the resulted voltage seen by DUT will be

$$U_{Pcc} = U_{grid} - U_Z \quad (2)$$

The behavior of the UVRT container was reproduced on the DyNaLab test bench. Fig. 5 demonstrates the impedance profile at the connection point of the WEC using the UVRT container. An identical characteristic was implemented at the DyNaLab. The impedance control enables dynamic changes in the closed-loop system.

Fig. 5 UVRT-container voltage dip behavior respect to impedance change, according to [8]

Fig. 6 Type “C” phase-to-phase voltage dip phasor diagram according to [9]

Fig. 7 Exemplary voltage curve of a UVRT test

In this test method, the impedance, voltage magnitude and phase angle profile are provided to the main controller of the grid simulator in a step time of 1 ms.

The virtual impedance specified at the PCC of the two test benches is calculated from the grid impedance and the shunt and series impedances of the UVRT container. This results in different impedances for each dip depth. The val-

ues for the impedance simulation can be obtained from Chap. 2.1. The tests at the DyNaLab test bench reproduce the behaviour of the UVRT container by dynamically adjusting the impedance during the UVRT test. At the CWD, on the other hand, the fault impedance is specified once at the beginning of the test so that the grid impedance is constant during the test.

Fig. 8 Voltage dip duration—no load

3.2 Mapping of phase-to-phase faults

In addition to the change in voltage magnitude, the asymmetrical voltage dips also lead to a phase angle jump. Depending on the voltage dip level, the corresponding phase angle is also set due to the characteristics of the UVRT container.

Possible grid faults can be divided into seven basic categories [9]. Unbalanced faults can cause unequal voltage amplitudes as well as unequal phase shifting of the individual phases. Depending on the type of fault and possible vector group effects, two-phase faults correspond to types “C” to “G”. Phase-to-phase faults are usually represented on the medium-voltage side using type “C”. The phase diagram of this fault type is shown in Fig. 6. Depending on the faulted phase, three scenarios can be reproduced for this voltage dip type. Fault on phase “a” & “c” or phase “a” & “b” or phase “b” and “a”.

The grid simulators can adjust the phase angle of the voltage. This change is not made by connecting the shunt impedances, as is the case with UVRT containers. The grid simulator controller must specify this angle together with the dip depth. Therefore, in order to emulate the realistic voltage dip, the phase angle jump must be calculated beforehand. The faulty phases in the tests of the E-115 E2 are “a” and “c”. Therefore, in addition to the voltage level, the correct phase angle jump needs to be examined during the evaluation. Chap. 4.2 presents the result and the calculation method of the phase angle jump.

4 Results

The evaluation of the UVRT tests can be divided into two parts. This paper shows the so called steady-state fault area, the dynamic transition is not investigated in detail. Fig. 7 shows an exemplary UVRT test. The stationary fault area of the UVRT test is the area in which all transient compensating effects are completed. According to [3], this is the range 100 ms after the fault occurs to 20 ms before the fault is declared. In the static area the following parameters are compared:

- Fault duration
- Positive and negative voltage value
- Voltage angle and amplitude
- Positive and negative sequence reactive current (k-factor)

4.1 Fault duration

The fault duration comparison for three-phase UVRT tests between the two test benches and the field is shown in Fig. 8. The test benches are able to replicate the voltage dip duration with a higher accuracy. In some cases, the fault is cleared in the field one period before the specified set point. In comparison, the maximum deviation at the test benches is 10 ms.

4.2 Voltage magnitude and phase angle

First, a comparison of the measurements with a decoupled wind turbine is performed, also called no-load tests [3]. The positive sequence voltage in the steady-state fault range is shown in Table 3. Table 4 shows the negative sequence

Table 3 Positive sequence voltage in the steady state fault range for the no-load tests

Setpoint			Feld		IWES		CWD	
	U_{set}	U_{pos}	U_{pos}	ΔU	U_{pos}	ΔU	U_{pos}	ΔU
3ph	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
	0.25	0.25	0.26	0.01	0.25	0.00	0.26	0.01
	0.47	0.47	0.49	0.02	0.47	0.00	0.46	0.01
	0.73	0.73	0.74	0.01	0.74	0.01	0.73	0.00
2ph	0.00	0.500	0.51	0.01	0.50	0.00	0.51	0.01
	0.25	0.625	0.65	0.02	0.63	0.01	0.62	0.00
	0.47	0.735	0.77	0.03	0.75	0.01	0.73	0.00
	0.73	0.865	0.90	0.03	0.88	0.02	0.86	0.00

Table 4 Negative sequence voltage in the steady state fault range for the two-phase no-load tests

Setpoint			Feld		IWES		CWD	
	U_{set}	U_{neg}	U_{neg}	ΔU	U_{neg}	ΔU	U_{neg}	ΔU
2ph	0.00	0.500	0.51	0.01	0.50	0.00	0.49	−0.01
	0.25	0.375	0.39	0.02	0.37	−0.01	0.38	0.00
	0.47	0.265	0.28	0.01	0.25	−0.01	0.27	0.00
	0.73	0.135	0.14	0.01	0.12	−0.02	0.14	0.00

Table 5 Positive sequence voltage in pu for three-phase faults under full load

U_{set}	Feld		IWES		CWD	
	U_{pos}	U_{pos}	U_{pos}	ΔU	U_{pos}	ΔU
0.00	0.00	0.02	0.02	0.01	0.01	0.01
0.00	0.00	0.02	0.02	0.21	0.01	0.01
0.25	0.32	0.32	0.00	0.32	0.00	0.00
0.25	0.32	0.32	0.00	0.32	0.00	0.00
0.47	0.55	0.55	0.00	0.54	−0.01	−0.01
0.47	0.56	0.55	−0.02	0.54	−0.02	−0.02
0.73	0.80	0.80	0.00	0.76	−0.04	−0.04
0.73	0.80	0.80	0.00	0.76	−0.04	−0.04

Table 7 Negative sequence voltage in pu for two-phase faults under full load

Setpoint	Feld		IWES		CWD	
	U_{set}	U_{neg}	U_{neg}	ΔU	U_{neg}	ΔU
0.00	0.500	0.50	0.48	−0.02	0.49	−0.01
0.00	0.500	0.50	0.48	−0.02	0.49	−0.01
0.25	0.375	0.36	0.35	−0.01	0.34	−0.02
0.25	0.375	0.36	0.35	0.00	0.34	−0.01
0.47	0.265	0.23	0.23	−0.01	0.22	−0.01
0.47	0.265	0.24	0.23	−0.01	0.22	−0.01
0.73	0.135	0.11	0.10	−0.01	0.11	0.00
0.73	0.135	0.11	0.10	−0.01	0.11	0.00

Table 6 Positive sequence voltage in pu for two-phase faults under full load

Setpoint		Feld	IWES		CWD	
U _{set}	U _{pos}	U _{pos}	U _{pos}	Δ U	U _{pos}	Δ U
0.00	0.500	0.50	0.51	0.01	0.51	0.01
0.25	0.500	0.50	0.51	0.01	0.51	0.01
0.47	0.625	0.69	0.67	−0.02	0.66	−0.03
0.73	0.625	0.67	0.67	−0.01	0.66	−0.01
0.00	0.735	0.80	0.80	0.00	0.77	−0.03
0.25	0.735	0.80	0.80	0.00	0.77	−0.03
0.47	0.865	0.92	0.93	0.01	0.88	−0.04
0.73	0.865	0.92	0.93	0.01	0.88	−0.04

voltage for the corresponding tests. Since the negative sequence voltage is zero for three-phase tests, only the two-phase no-load measurements are shown in Table 4. The dip depth is always indicated as the remaining phase-to-phase voltage between the two affected phases [3]. However, the positive and negative sequence components are relevant for the evaluation and comparison. Therefore, the first step is to calculate the expected positive and negative sequence voltage from the given residual phase-to-phase voltage. The tables contain the calculated expected nominal value, the values of the field measurement and the two test bench measurements, as well as the deviation of the measured values from the nominal value ΔU . The two test benches and the field measurements show the expected values in the positive and negative sequence voltages. The maximum deviation is 0.03 pu for the two-phase field tests with a dip depths of 0.47 and 0.73 pu, respectively. The tolerance limit of 0.05 pu from the FGW TR3 is thus fulfilled for all three test facilities.

Table 8 Phase angle jump comparison for phase-to-phase fault at no load condition

Set point voltage	Calculated	IWES			CWD			Feld		
		U _a	U _b	U _c	U _a	U _b	U _c	U _a	U _b	U _c
0	60.00	60.28	−0.02	60.40	60.41	0.02	60.10	58.36	0.50	59.10
0.25	36.58	35.64	0.02	36.22	36.83	0.27	36.19	40.00	2.50	35.00
0.47	20.86	19.93	0.25	20.12	19.24	0.14	18.82	18.40	−2.10	21.14
0.73	8.35	7.55	−0.30	7.47	8.23	0.10	7.39	7.43	1.60	8.40

Fig. 9 Two-phase fault phase angle jump for faulted phase U_a, U_c—no load condition **Fig. 10** Two-phase fault phase angle jumps for un-faulted phase U_b—no load condition

The measurements in the partial load range are carried out at different power outputs of the DUT. Therefore, it cannot be recognized whether existing differences are due to the test equipment or to the different power output of the

wind turbine. For this reason, only the full load tests are considered in the further discussion. Table 5 shows the comparison of the positive sequence voltage of the three-phase full load measurements. Two measurements are shown in comparison for each dip level, since [3] requires two measurements per voltage level. In this case, ΔU means the deviation between the test bench measurements and the field measurement. Especially at the low dip depths, a good agreement between the three test systems is observed. The deviation here is a maximum of 0.02 pu. At the dip depth of 0.73 pu, the CWD shows a higher deviation from the field measurement. This deviation amounts to 0.04 pu.

Table 6 shows the comparison of the two-phase full load tests. Up_{os} is the calculated no-load rated value of the positive sequence system. ΔU describes the deviation between the field measurement and a test bench measurement. The behavior is comparable to the three-phase full load tests. The maximum deviation between a test on the test bench and the test in the field is again reached at a dip of 0.74 pu at the CWD. The negative sequence voltage, shown in Table 7, shows a very good agreement between the three test systems. The maximum deviation is 0.02 pu.

Fig. 11 Reactive current behavior of the wind turbine in the positive sequence system during three-phase UVRT tests

Fig. 12 Reactive current behavior of the wind turbine in the positive sequence system during two-phase UVRT tests

4.3 Phase angle jump

The asymmetrical voltage dip leads to a phase angle jump of the faulty phases due to a change in the impedance. The jump in the phase angle can be calculated according to Eq. 3.

$$\alpha = \arctan\left(\frac{1}{U_{\text{retained}} \cdot \sqrt{3}}\right) - 30^\circ \quad (3)$$

In this case, U_{retained} is the voltage drop from phase to phase and α the jump of the phase angle at no load. Using

the voltage divider based test equipment, the angle change occurs due to the connection of the impedances. The nominal change of the angle α is calculated in advance at the two test benches and specified as a reference value. Table 8 shows the comparison between the calculation and the measurements.

Fig. 9 and 10 show the phase angle jump at the two test benches and in the field for the phase-to-phase voltage. Both the angle jump of the faulty phases (U_a , U_c) and of the non-faulted phase (U_b) are presented. The emulated phase angle jump with the grid simulators corresponds to

Fig. 13 Reactive current behavior of the wind turbine in the negative sequence system during two-phase UVRT tests

the measured phase angle change. Both test benches can accurately emulate the phase angle jump.

4.4 Reactive current support

In addition to the resulting voltage behavior, a comparison of the reactive current behavior of the system is carried out for the three test facilities. Fig. 11 shows the reactive current behavior in the positive sequence for three-phase UVRT tests. The required k-factor with the corresponding tolerance limits is also shown [1]. All three test facilities are within the tolerance band. Only when the residual voltage drops to 73%, a deviation between the three test facilities can be detected. At the CWD the resulting voltage is 4% lower than in the field measurement.

In the case of two-phase faults, an evaluation of the reactive current behavior in the negative sequence system (Fig. 13) is carried out in addition to the evaluation of the positive sequence reactive current behavior (Fig. 12). If the voltage drops to 0 pu, all three test devices are beyond the tolerance range. VDE-AR-N 4120 defines that no reactive current injection is required for faults with a residual PCC voltage of less than 0.15 pu. The remaining tests are entirely within the tolerance limits. The DUT shows identical behavior in the positive and negative sequence voltage regardless of the test equipment. The deviations of the resulting positive sequence voltage at the 0.73 pu dip of up to 4% are the reason for the low reactive current injection fluctuations at this dip depth.

5 Conclusion

The comparison with field test results allow the conclusion that test benches equipped with a grid simulator are able to emulate voltage dip behavior if proper test procedure is followed. The voltage and grid characteristics must be precisely interpreted before the test is carried out in order to emulate a voltage dip that is close to the state of the art. An essential differentiating characteristic between the test bench tests and the field measurement with UVRT container is the grid impedance, which is set at the PCC of the DUT. The impedance at the test bench consists of the physically installed components of the grid simulator, such as the transformers or the filter elements. This differs very significantly from the impedances that result because of the voltage divider-based UVRT container in the field. Therefore an artificial grid impedance is specified at the test benches by means of the control of the grid simulators, which can be implemented in a PHiL setup. This paper shows that the two grid simulators can reproduce the behavior of the voltage dip in comparison to the field for quasi steady-state conditions. In the next step, the dynamic range (first 20ms after the voltage dip) is investigated to prove the effectiveness of this method, with emphasis on the validation of the impedance emulation methods.

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References

1. VDE-AR-N 4120 (2018) Technische Regeln für den Anschluss von Kundenanlagen an das Hochspannungsnetz und deren Betrieb (TAR Hochspannung)
2. IEC 61400-21-1 (2019) Wind energy generation systems—part 21-1: measurement and assessment of electrical characteristics—wind turbines
3. FGW TR3 (2018) Bestimmung der elektrischen Eigenschaften von Erzeugungseinheiten und -anlagen, Speicher sowie für deren Komponenten am Mittel-, Hoch- und Höchstspannungsnetz
4. Jassmann U (2018) Hardware-in-the-loop wind turbine system test benches and their usage for controller validation. Dissertation. RWTH Aachen University, Aachen
5. Helmedag AS (2014) System level multi-physics power hardware in the loop testing for wind energy converters. Dissertation. RWTH Aachen University, Aachen
6. Averous NR, Berthold A, Schneider A, Schwimmbeck F, Monti A, De Doncker RW (2016) Performance tests of a power-electronic-converter for multi-megawatt wind turbines using agrid emulator. The science of making torque from wind. *J Physics* 753(7):072015. <https://doi.org/10.1088/1742-6596/753/7/072015>
7. Neshati M, Zuga A, Jersch T, Wenske J (2016) Hardware-in-the-loop drive train control for realistic emulation of rotor torque in a full-scale wind turbine nacelle test rig. In: European Control Conference (ECC)
8. Azarian S, Jersch T, Khan S (2019) Comparison of impedance behavior of UVRT-container with medium voltage grid simulator in case of unsymmetrical voltage dip. In: CWD 2019 Aachen
9. Bollen MH (1999) Understanding power quality problems, voltage sags and interruptions. IEEE press series on power engineering (Chapter 4). IEEE Xplore (Online service), John Wiley & Sons, New York, Hoboken, New Jersey, Piscataway, New Jersey