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CORRECTION

Correction: Improved analog and AC performance for high frequency linearity based applications using gate-stack dual metal (DM) nanowire (NW) FET (4 H-SiC)

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The original version of this article unfortunately contained error in first author's name and affiliation of authors.

In this article author's name Neeraj was incorrectly written as Neeraj Neeraj.

The affiliation details for all the authors were incorrectly given as IGDTUW, Kashmere Gate, New Delhi, India but should read as given below

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