

Analysis of a high-performance ultra-thin body ultra-thin box silicon-on-insulator MOSFET with the lateral dual-gates: featuring the suppression of the DIBL

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Abstract An inspiring UTBB SOI MOSFET structure with enhanced immunity to the drain-induced barrier lowering (DIBL) is analyzed. The structure includes the dual-gates in the lateral direction. The voltage difference is applied between the dual-gates, through which the electrostatic potential and the energy band along the channel are modified and the electrical performance is boosted. The electrical characteristics are investigated by measuring the electron concentration, the conduction band energy level, and the potential at the front-surface. The impact of the negative voltage bias applied to the right gate on the performance of the new device is studied, and compared to that of the conventional ultra-thin body ultra-thin box silicon-on-insulator (UTBB SOI) devices. The results reveal that the undesirable DIBL values are lower in this innovative device than that in the conventional UTBB SOI MOSFET.

1 Introduction

The ultra-thin body ultra-thin box (UTBB) SOI MOSFET with the lightly-doped channel is demonstrating a high advantage for ultimate MOSFET scaling because of its dramatic suppression of short-channel effects (SCEs) (Young 1989; Grenouillet et al. 2013), and its superiority of low-power high-speed application (Haond 2014; Stephane and Thomas 2016). The SCEs, which mainly includes the threshold voltage roll-off, the drain induced barrier lowering (DIBL), and the subthreshold swing degradation, is the major barrier for MOSFET downscaling. Therefore, based on the UTBB SOI technology, a number of methods have been proposed to further reduce the SCEs, by employing the channel engineering, the source/drain engineering (Yamada et al. 2013b, c; Srivastava et al. 2016), the back-biasing technique (Burignat et al. 2010; Karatsori et al. 2015), the thickness modulation of the buried oxide layer (Yamada et al. 2013a), and the gate voltage difference engineering (Anvarifard et al. 2009; Anvarifard and Orouji 2013; Lahgere et al. 2015).

The DIBL characterizes the physical phenomena that in the short channel devices operating in the subthreshold region, the potential barrier between the source and the channel is lowered because of the bias voltage applied to drain. And it causes excess carriers injecting into the channel and resulting in an increased subthreshold current. The DIBL can be evaluated as the gate threshold voltage shift due to the drain voltage variation (Colinge and Colinge 2002; Arshad et al. 2012; Mutlu and Rahman 2000). Based on the innovative concept of the lateral dual-gates to shield the drain voltage and reduce the DIBL, in this paper, the carrier density, the energy band, and the potential along the channel are investigated quantitatively. Moreover, the resultant magnitude of the DIBL, by setting

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the optimum voltage difference on the dual-gates, is compared to that of a conventional UTBB SOI device. Then, the impact of the negative voltage bias of the right gate (Gate_Control) on the DIBL is explained, in the scenario of the UTBB MOSFET with a lightly-doped silicon film. And the channel length is 22–46 nm. The results of this work are instructive for design and application of the novel UTBB SOI devices.

2 Proposed device

The schematic cross-sectional view of a n-channel UTBB SOI MOSFET with the lateral dual-gates for modeling and simulation is shown in Fig. 1. The x - and y -axes of the 2D structure are taken along the source-channel and gate-to-gate-oxide interfaces, respectively. The two poly-gates are named as Gate_Main and Gate_Control, respectively. And there is a small gap between the gates, which is filled by SiO₂. In this work, the total channel length is 22–46 nm. The lengths of the Gate_Main and the Gate_Control are equal. The length of the small gap is set to be the constant 2 nm. The lengths of the Gate_Main, the Gate_Control, and the split are denoted by L_M , L_C , L_S , respectively. That is, $L_M = L_C$, and $L_S = 2$ nm. V_{G_M} and V_{G_C} are the voltage biases applied to the Gate_Main and the Gate_Control, accordingly. Their voltage difference is named as V_{diff} . It is concluded from this study that when Gate_Main dominates the device to work in the sub-threshold region, the negative offset voltage on the Gate_Control can play an important role in reducing the DIBL. And the simulation results from Synopsys TCAD have been thoroughly analyzed. The symbols (t_{oxf} , t_{si} , t_{oxb} , t_{sub} , and x_d) used in Fig. 1 are the thicknesses of the gate-

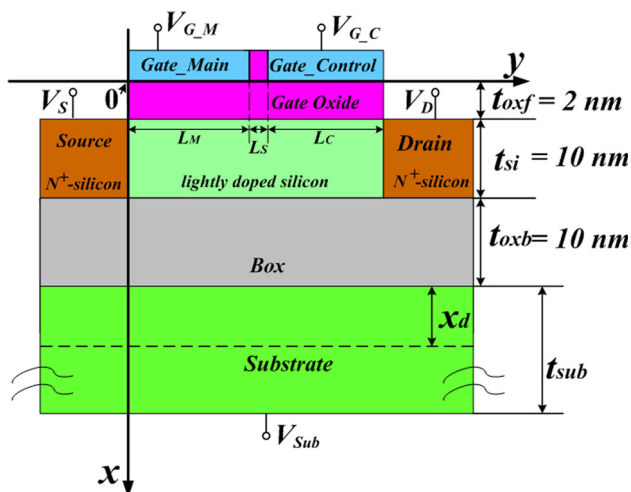


Fig. 1 Cross-sectional view of the n-channel UTBB SOI MOSFET with lateral dual-gates

oxide, silicon film, buried-oxide, substrate, and depletion region in the substrate, respectively. V_D , V_S , and V_{Sub} are the bias voltages applied to the drain, the source, and the substrate, respectively. The source voltage V_S is connected to the ground, so V_{Sub} is also called as V_{BS} . And ψ_{sub} is the potential at the substrate/buried-oxide interface. The typical parameters are summarized in Table 1.

To analyze the impact of voltage difference engineering on electrical performance, it is essential to compare the new structure with the conventional UTBB SOI structure with the same dimensional parameters, doping concentration, according to Table 1. For the new device, the voltage on the Gate_Main is defined as threshold voltage. For both the new and the conventional structures, the threshold voltage values are extracted from numerical simulation outputs by industrial standard linear-extrapolation techniques, in which V_{TH} is obtained by linearly extrapolating the I_d -versus- V_g characteristics to the V_g -axis at some small V_{DS} (Krutsick et al. 1987).

3 Analysis of electrical characteristics

Figure 2 shows the electron concentration along the front-channel of both structures in a log scale with different V_{G_C} , at the constant $V_{G_M} = 1.2$ V, $V_{DS} = 1.2$ V, and $V_{sub} = 0$ V. And the gate voltage of the conventional UTBB SOI device is also set to the constant 1.2 V. In spite of no direct voltage bias on the gap, it is observed that the electron concentration under the gap is none-zero under all dependent voltage difference conditions. And the electron concentrations under the gap and the interfaces of the two different gates are continuous. The electron concentration below the Gate_Control with the various V_{G_C} bias condition is always smaller than that for the conventional UTBB SOI structure. And the electron concentration below

Table 1 The typical parameters of the n-channel UTBB SOI MOSFET with lateral dual-gates

Parameter	Value
Total channel length L ($L_M + L_C + L_S$)	22–46 nm
Length of Gate_Main L_M	10–22 nm
Length of Gate_Control L_C	10–22 nm
Length of gate gap L_S	2 nm
Source/drain doping	$2 \times 10^{20} \text{ cm}^{-3}$
Lightly-doped silicon film N_A	$5 \times 10^{14} \text{ cm}^{-3}$
Gate-oxide thickness t_{oxf}	2 nm
Silicon film thickness t_{si}	10 nm
Buried-oxide t_{oxb}	10 nm
Gate work-function	4.8 eV
Dual-gates voltage difference V_{diff}	$V_{diff} = V_{G_M} - V_{G_C}$

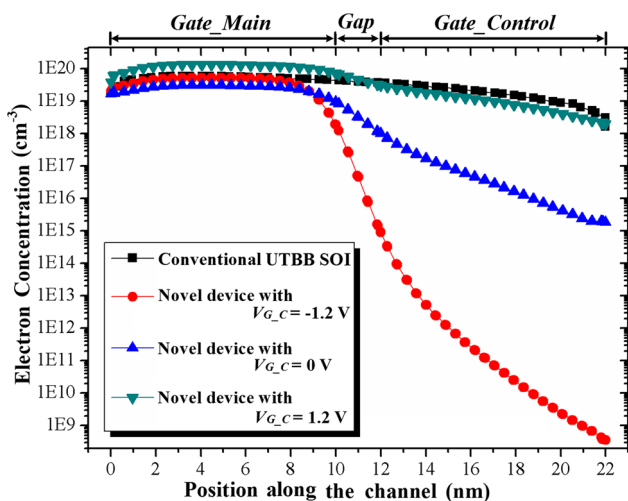


Fig. 2 Comparison the electron concentration along the front-channel of the proposed structure to that of the conventional UTBB SOI device on a log scale, with different voltage biases on V_{G_C} . Other parameters are $V_{G_M} = 1.2$ V ($V_{GS} = 1.2$ V), $V_{DS} = 1.2$ V, $V_{Sub} = 0$ V, and $L = 22$ nm

the Gate_Control decreases rapidly and greatly from 10^{19} to 10^8 cm^{-3} when V_{G_C} reducing from 1.2 to -1.2 V. Figure 3 exhibits the electron concentration along the front-channel of the new structure in a log scale with the different V_{DS} . In Fig. 3, V_{G_M} is 0.5 V, and V_{G_C} is -1.2 V. No matter V_{DS} is 0.5 or 1.4 V, the surface electron concentrations beneath the gap and the Gate_Control all drop sharply. And the value of electron concentrations beneath the Gate_Control for $V_{DS} = 0.5$ V and $V_{DS} = 1.4$ V are quite close. So it can be deduced that the

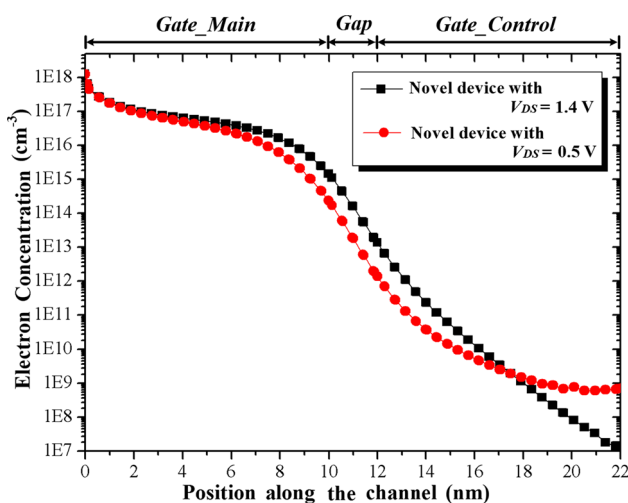


Fig. 3 Comparison the electron concentration along the front-channel of the proposed structure on a log scale, with different voltage biases on V_{DS} . Other parameters are $V_{G_M} = 0.5$ V, $V_{G_C} = -1.2$ V, $V_{Sub} = 0$ V, and $L = 22$ nm

deep negative V_{G_C} can shielded the impact of V_{DS} 's increment.

Corresponding to the surface charge in Figs. 2 and 3, the variation of the conduction band energy along the front-surface under different voltages are shown in Figs. 4 and 5. Some common characters are observed from Figs. 4 and 5 that the conduction band is bent to go up in the middle under the gap and the Gate_Control. Because the states of the carrier (in the accumulation, the depletion, or the inversion) beneath the gap and the Gate_Control are inconsistent with the state created by V_{G_M} beneath the Gate_Main. The variation of conduction band energy along the front-channel of both structures with the different V_{G_C} , at the constant V_{DS} of 1.2 V and V_{G_M} of 1.2 V, is shown in Fig. 4. It can be seen that with V_{G_C} gradually decreasing from 1.2 to -1.2 V, the conduction band beneath the Gate_Control moves gradually away from the Fermi level, as the electron concentration gradually decreases in the right channel region, which leads to a greater degree of curvature for the conduction band under the Gate_Control. Then, the variation of conduction band energy along the front-channel for the new structure with the different V_{DS} , at the constant V_{G_M} and V_{G_C} , is shown in Fig. 5, in which situation V_{G_M} is just a little higher than the threshold voltage, whereas the deep minus V_{G_C} is much smaller than the threshold voltage. It is observed that even though the varying V_{DS} can affect conduction band at any position along the channel, and can adjust the steepness of the gradients of the bending for the conduction band, there are still the uphill curves from the start of the gap towards the

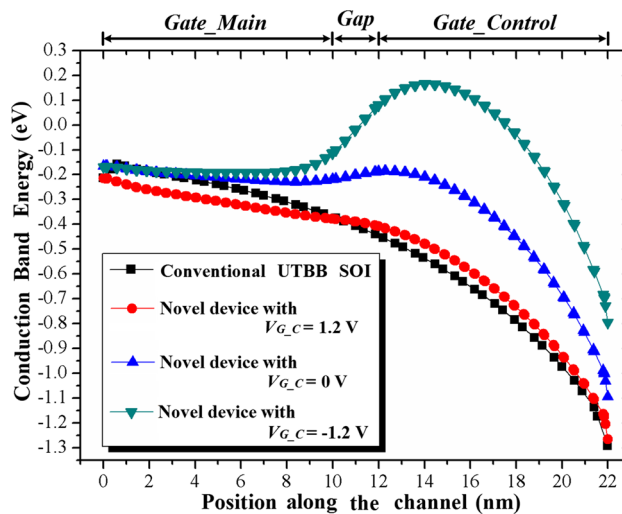


Fig. 4 Comparison the variation of conduction energy band along the front-channel of the proposed structure to that of the conventional UTBB SOI device with different voltage biases on V_{G_C} . Other parameters are $V_{G_M} = 1.2$ V ($V_{GS} = 1.2$ V), $V_{DS} = 1.2$ V, $V_{Sub} = 0$ V, and $L = 22$ nm

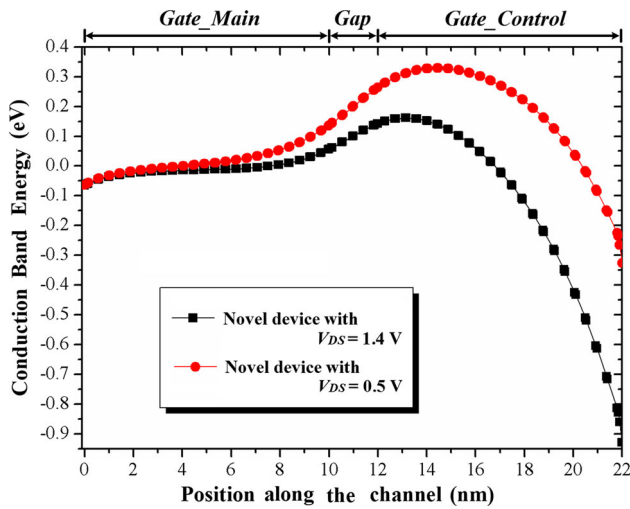


Fig. 5 Comparison the variation of the conduction energy band along the front-channel of the proposed structure with the different voltage biases on V_{DS} . Other parameters are $V_{G_M} = 0.5$ V, $V_{G_C} = -1.2$ V, $V_{Sub} = 0$ V, and $L = 22$ nm

middle area beneath the Gate_Control, which can in turn exert great resistance for the electron moving to the drain.

In same voltage bias scenario as in Figs. 5 and 6 characteristics the variation of the front-surface potential as the function of the position along channel with different V_{DS} . And the front-surface potential distribution just under the gap, which is part of Fig. 6, is zoomed-into further highlight in Fig. 7. As shown in Fig. 6, the potential variation under Gate_Main, especially the difference of the potentials at the source/channel interface is tiny enough to be ignored under various biases on V_{DS} . Because the deep minus voltage on Gate_Control can make the drain

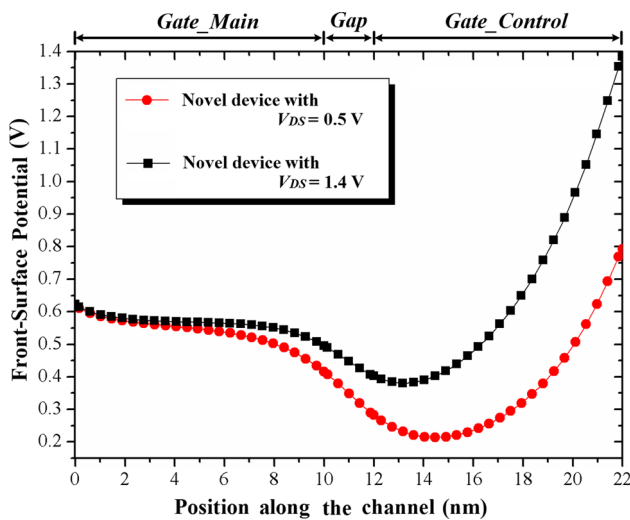


Fig. 6 Comparison the variation of front-surface potential of the proposed structure with the different voltage biases on V_{DS} . Other parameters are $V_{G_M} = 0.5$ V, $V_{G_C} = -1.2$ V, $V_{Sub} = 0$ V, and $L = 22$ nm

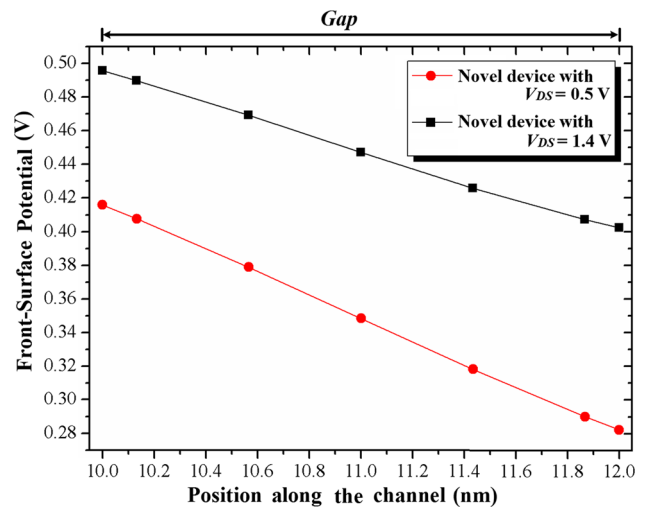


Fig. 7 To zoom-in the front-surface potential distribution of the proposed structure beneath the gap with the different voltage biases on V_{DS} . Other parameters are $V_{G_M} = 0.5$ V, $V_{G_C} = -1.2$ V, $V_{Sub} = 0$ V, and $L = 22$ nm

voltage’s influence become less on the left side of the channel. Also as highlighted in Fig. 7, the front-surface potential distribution under the gap is a linear function. Moreover, in the case of different V_{DS} , the linear slope can be considered approximately equal. Other than a step function of front-surface potential proposed by (Anvarifard et al. 2009), we observed from Fig. 6 that the front-surface potential is a continuous function. The channel can be divided into three regions, namely, Channel_Main, Channel_Gap, and Channel_Control. Either the Channel_Main or the Channel_Control is controlled by its corresponding gate. The surface potentials of the Channel_Main and Channel_Control all fit with the parabolic approximation theory (Young 1989; Suzuki and Pidin 2003), but with different curvature. In addition, it is observed from Fig. 7 that surface potential of the Channel_Gap is a linear function. And the boundary surface potential values at the interfaces of Gate_Main to gap, and Gate_Control to gap are continuous without the mutation point.

Then, Fig. 8 gives further comparison of the horizontal potential along the front-surface, the back-surface, and 2 nm below the front-surface for the proposed structure. Then the horizontal potential distribution just under the gap, which is part of Fig. 8, is zoomed-into highlight in Fig. 9. It is different from the front-surface potential mainly controlled by the lateral dual-gates on the topside that the back-surface potential is mainly controlled by the continuous substrate voltage. Thus, the back-surface potential is one single parabolic. From the front-surface to the back-surface perpendicularly, the influence of the top lateral dual-gates on the potential distribution inside the silicon film gradually decreases. Just as highlighted in

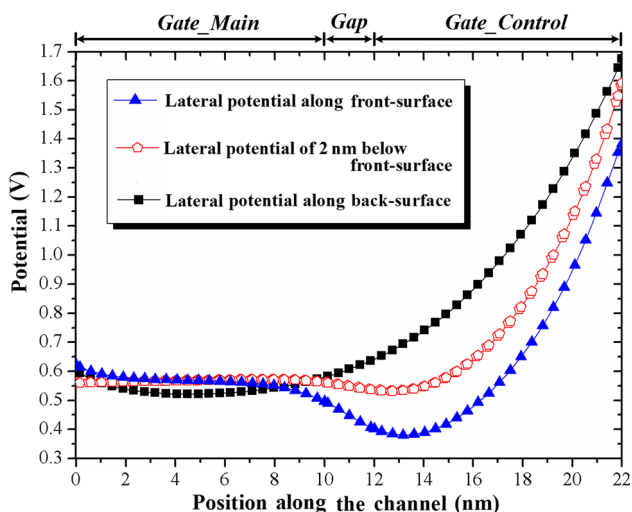


Fig. 8 Comparison the lateral potential along the front-surface, the back-surface, and 2 nm below the front-surface, for the proposed structure. Other parameters are $V_{G,M} = 0.5$ V, $V_{G,C} = -1.2$ V, $V_{Sub} = 0$ V, $V_{DS} = 1.2$ V, and $L = 22$ nm

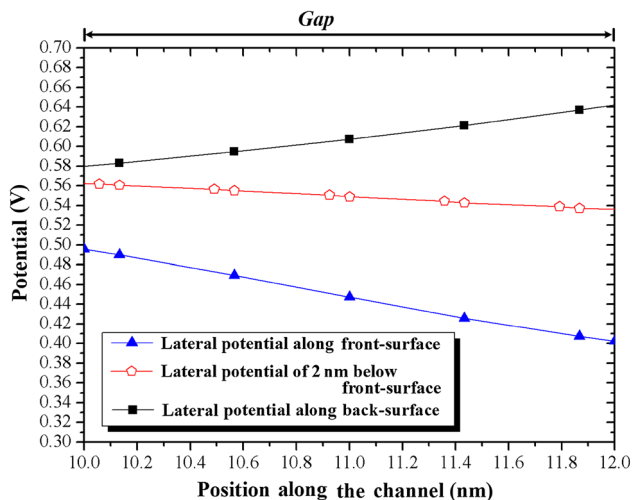


Fig. 9 To zoom-in the potential distribution of the proposed structure beneath the gap along the front-surface, the back-surface, and 2 nm below the front-surface, for the proposed structure. Other parameters are $V_{G,M} = 0.5$ V, $V_{G,C} = -1.2$ V, $V_{Sub} = 0$ V, $V_{DS} = 1.2$ V, and $L = 22$ nm

Fig. 9, along the boundary of the gap, the potential values at front-surface, the back-surface, and 2 nm below the front-surface are different. And the slopes of the potential distributions beneath the gap are also different. As a result, the vertical potential distributions along the edges of the gap inside the silicon film are changing with an unfixed trend, according to the various front/back voltage coupling conditions.

To exemplify the impact of Gate_Control on the channel current, in Fig. 10, we examine the I_{DS} -versus- $V_{G,M}$ characteristic in $V_{G,C} = -1.2$ V, and compare it to the normal

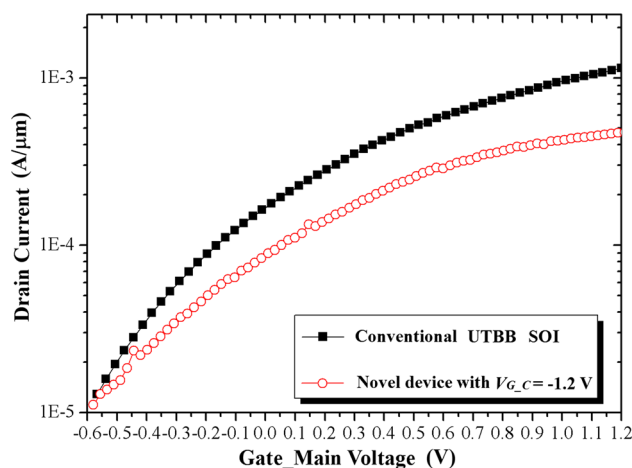


Fig. 10 Comparison of the I_{DS} -versus- $V_{G,M}$ for the proposed structure, in $V_{G,C} = -1.2$ V, to the I_{DS} -versus- V_{GS} for the conventional UTBB SOI device. Other parameters are $V_{DS} = 1.2$ V, $V_{Sub} = 0$ V, and $L = 22$ nm

I_{DS} -versus- V_{GS} curve of the conventional UTBB SOI device. The currents are in log scale in Fig. 10. The conclusion drawn from Fig. 10 is consistent with the conclusion from the previous diagrams of the conduction band energy and the potential that with higher energy barrier introduced by $V_{G,C}$, the drain current of the new device is less in all states than that of the conventional device. Therefore, this feature can be optimally explored in the standby mode to achieve as low dissipation power as possible by setting the $V_{G,C}$ to be far below the threshold voltage. In this work, in the discussions of the threshold roll-off in Fig. 11 and the DIBL in Figs. 12, 13, and 14, $V_{G,C}$ is set to be -1.2 V, which is negative of the 1.2 V power supply. And all the threshold voltage values of the novel device are extracted from the I_{DS} -versus- $V_{G,M}$ curves under such $V_{G,C}$ bias.

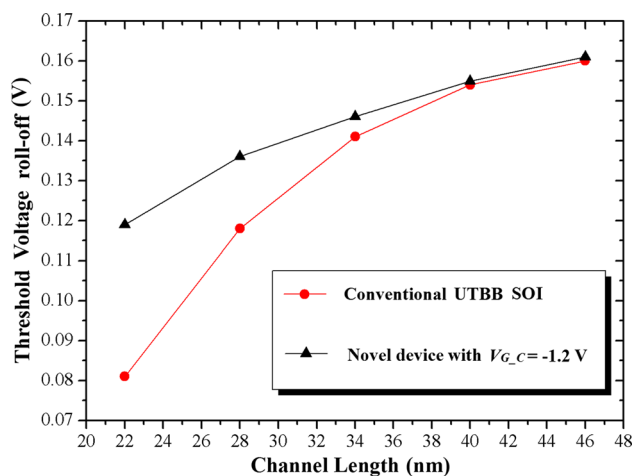


Fig. 11 Comparison of the threshold voltage roll-off variation as the function of the channel length for the proposed structure, with $V_{G,C} = -1.2$ V, to that for the conventional UTBB SOI device. Other parameters are $V_{DS} = 0.05$ V, $V_{Sub} = 0$ V, and $L = 22-46$ nm

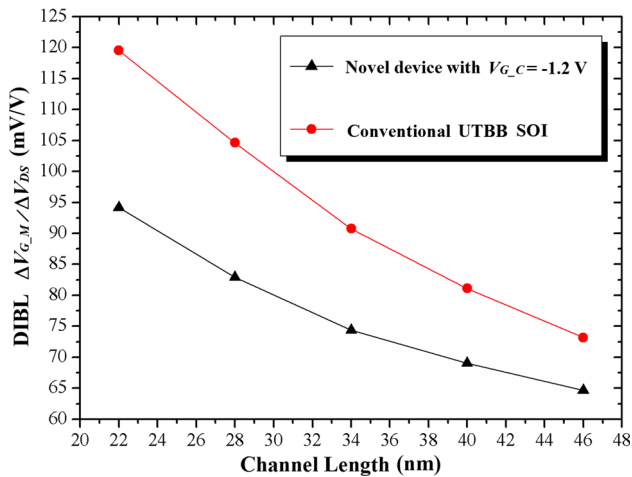


Fig. 12 Comparison of the variation of the DIBL as the function of the channel length for the proposed structure, with $V_{G_C} = -1.2$ V, to that for the conventional UTBB SOI device. Other parameters are $V_{Sub} = 0$ V, and $L = 22$ – 46 nm

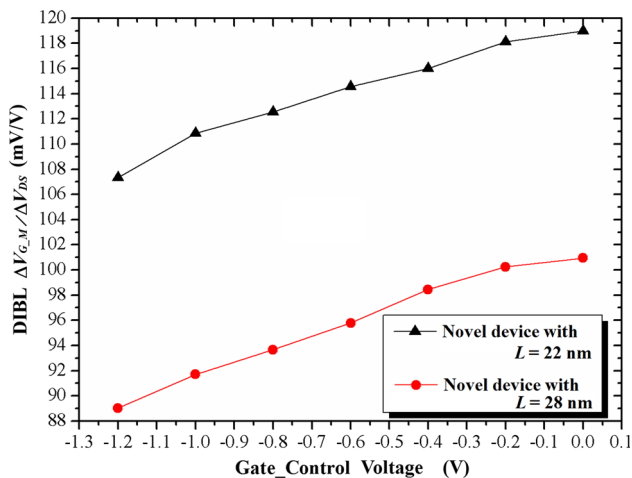


Fig. 13 Comparison of the variation of the DIBL as the function of V_{G_C} for the proposed structure with different channel length. Other parameters are $V_{Sub} = 0$ V

The threshold voltage roll-off as a function of channel length is depicted and compared to the conventional UTBB SOI device in Fig. 11. It is observed as the channel length shrinks, the threshold voltage decreases for either the new or the conventional devices. But the unique shielding drain voltage feature of the negative V_{G_C} permits the tuning of threshold voltage for a considerable range of channel length under the nanometer region for the new structure. As a result, the shrinking of the channel length gives an exponential roll-off behavior (Shee et al. 2014) for the conventional device. Comparatively, the threshold is higher in every channel length node for the new device. And the trend of threshold voltage roll-off with the channel length decrease is slower for the new device. This is

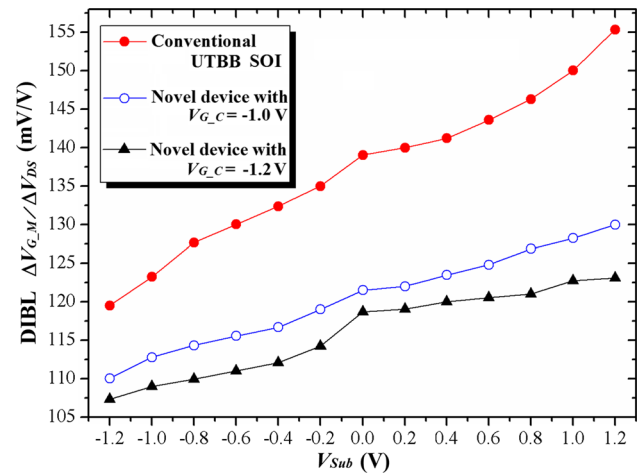


Fig. 14 Comparison of the variation of the DIBL as the function of V_{Sub} for the proposed structure with different V_{G_C} , to that for the conventional device. Other parameters are $V_{G_C} = -1.2$ and -1.0 V, and $L = 22$ nm

another superior of the new structure over the conventional UTBB SOI structure.

Figures 12, 13 and 14 analyze the extracted DIBL values under the different conditions. The magnitude of DIBL (in mV/V) is defined as the gate threshold voltage shift due to a drain voltage variation between the linear voltage ($V_{DS1} = 0.05$ V) and the saturation voltage ($V_{DS2} = 1.2$ V) (Colinge and Colinge 2002; Singh et al. 2017). In Eq. (1), V_{TH_LINEAR} is the linear threshold voltage, and $V_{TH_SATURATE}$ is the saturation threshold voltage:

$$DIBL = \frac{V_{TH_LINEAR}|_{V_{DS1}} - V_{TH_SATURATE}|_{V_{DS2}}}{V_{DS2} - V_{DS1}} \quad (1)$$

The comparison of the DIBL's variation as the function of the channel length for the proposed structure to that for the conventional UTBB SOI device is shown in Fig. 12. And the analyses for the new devices are in case that $V_{G_C} = -1.2$ V. It is observed that DIBL values for either the new or the conventional devices become higher with the channel length shrinking. But the tendency of the DIBL's increment for the new device is slower. And it is clear that the new device globally possesses the lower DIBL values in every channel length node than the conventional devices. Therefore, the capability of suppressing the DIBL is much more enhanced in the new devices. Then the comparison of the variation of the DIBL as the function of V_{G_C} for the proposed new structure with different channel length is plotted in Fig. 13. The trends in Fig. 13 are well aligned with the conclusions shown in Fig. 2 and 4. First of all, the negative voltage offset on Gate_Control can raise the energy barrier along the channel to the drain. As a result, the impacts of the V_{DS} on both the source/channel's conduction band and the channel electrons are

partially blocked. Under such a function, as V_{G_C} becomes even negative, the effect of shielding is more obvious. As a result, for the new structure device, the DIBL value decreases with V_{G_C} decrease. Moreover, with the same V_{G_C} , the DIBL for 28 nm is smaller than that for 22 nm. When $V_{DS} = 0.05$ V, the threshold voltage on Gate_Main is 0.16 V for $L = 28$ nm, and 0.13 V for $L = 22$ nm, respectively. It can be concluded from Fig. 13 that for the 1.2 V power supply design, the optimal gate voltage difference is: $V_{G_M} = 0$ V, $V_{G_C} = -1.2$ V (which does not need to introduce the charge pump to further decrease the negative voltage on V_{G_C}). Under these circumstances, the new device works in the subthreshold region, the variation of drain voltage is shielded by V_{G_C} to a greater degree, and the DIBL is minimized. Figure 14 compares of the variation of DIBL as the function of V_{Sub} for the proposed structure with different V_{G_C} to that for the conventional device. It is seen that as the new structure having the lateral dual-gates only on the top, the effect of Gate_Control's shielding influence of V_{DS} is smaller toward the back-surface. Thus, with the increscent V_{Sub} , the back channel current enlarges gradually, and the DIBL enlarges accordingly for both the conventional device and the new device. Nevertheless, with the negative Gate_Control, the variation of the DIBL as the function of V_{Sub} is still lower than that of the conventional device. Therefore, the lateral voltage difference of the dual-gates on the topside also has the capability to dynamically alleviate the impact of substrate voltage on the DIBL, to a certain extent.

4 Conclusion

In this paper, we have demonstrated that the specified UTBB SOI structure with the voltage difference on lateral dual-gates is superior to the traditional UTBB SOI device for the diminished DIBL effect. And the negative voltage offset on the right gate (Gate_Control) can weaken the impact of the drain voltage on source/channel interface potential. Therefore, the DIBL is suppressed to a extent. Moreover, a conclusion is drawn from the numerical simulation that despite being controlled by the different gate voltages, the front-surface potential of this UTBB SOI device is a continuous function, rather than a step function proposed by (Anvarifard et al. 2009). This device structure is valid not only for UTBB SOI transistors, but also generally useful for the vertical independent double-gate and gate-all-around devices featuring a lightly-doped channel. At this stage, as the definite boundary conditions along the dual-gates' gap inside silicon film have not be derived yet, the complete potential distribution model is beyond the scope of this study, and will be developed in near future

based on a more reasonable boundary condition approximation along the lateral dual-gates' gap inside silicon film.

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