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Abstract In high-energy physics experiments, tracking and vertexing is nowadays mostly done using semiconductor detectors. Among the employed detectors are hybrid pixel sensors, passive sensors and recently also depleted monolithic active pixel sensors (DMAPS), which integrate the particle sensor with front-end electronics. Currently, the dominant material for the production of such sensors is silicon. However, the use of silicon carbide is currently being investigated. In this work we report on our progress on the development of silicon-based DMAPS. Further, we present two approaches for reading out passive silicon carbide detectors at particle rates from the kHz to the GHz range.

 $\label{eq:constraint} \begin{array}{l} \mbox{Keywords} \ \mbox{Beam monitor} \cdot \mbox{High energy} \cdot \mbox{Detector} \cdot \\ \mbox{Sensor} \cdot \mbox{Silicon carbide} \cdot \mbox{Asic} \cdot \mbox{CMOS} \cdot \mbox{Radiation} \\ \mbox{hardness} \cdot \mbox{Ionizing radiation} \cdot \mbox{Maps} \cdot \mbox{DMAPS} \cdot \mbox{Strip} \\ \mbox{sensor} \end{array}$

Detektorentwicklung für die Teilchenphysik

Zusammenfassung In Experimenten der Hochenergiephysik werden Detektoren zur Verfolgung von Partikeln sowie zur Bestimmung der Kollisionspunkte meist aus Halbleitern gefertigt. Dazu zählen unter anderem hybride Pixeldetektoren, passive Halbleiterdetektoren und seit Kurzem monolithische, aktive Pixelsensoren (MAPS). Bei letzteren sind die teilchendetektierenden Elemente sowie die Ausleseelektronik auf einem einzigen Chip untergebracht. Das dominierende Material für die Herstellung solcher Detektoren ist Silizium. Derzeit wird für einige Anwendungen aber auch die Verwendung von Karborund untersucht. In dieser Arbeit berichten wir zunächst über unsere Fortschritte in der Entwicklung von MAPS. Anschließend stellen wir zwei Methoden vor, mit denen passive, aus Karborund gefertigte Detektoren ausgelesen werden können. Beide eignen sich für die Vermessung von Ionenstrahlen mit Teilchenraten im Bereich von wenigen kHz bis in den GHz-Bereich.

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Schlüsselwörter Teilchendetektor · Hochenergie · Sensor · Karborund · Siliziumcarbid · Ionisierende Strahlung · Monolithische aktive Pixelsensoren · Streifendetektor

1 Introduction

Particle detectors have evolved over decades. While at first particle tracks were recorded using cloud chambers, several technologies have replaced them since then. One of the main drivers of this development has been the search for rare events requiring the fast recording of detector interactions. Up to now this has been attained by high spacial accuracy and discrimination of tracks based on the location of the collision. Currently, research is moving towards introducing temporal discrimination of particle tracks. To attain highest spacial accuracy as well as enable fast readout and storage of recorded information, semiconductor based detectors are employed. Among them are hybrid pixel sensors (HPS), passive sensors, monolithic active pixel sensors (MAPS) and depleted monolithic active pixel sensors (DMAPS).

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In HPS the sensing element and the readout electronics are processed on separate substrates and then bonded together. They provide a larger flexibility in terms of processing of the radiation sensing element and thus offer the highest performance. However, processing sensor and readout circuit separately and bonding them together afterwards increases process complexity which reduces yield and reliability. Still, due to their superior performance HPS are currently the dominant technology for tracking in particle collision experiments. They are employed in the tracker of the CMS [1], ATLAS [2] and the BELLE-2 [3] experiment. Currently, this dominance is challenged by a new generation of MAPS and DMAPS, whereby MAPS have already being deployed in ALICE ITS2 [4] and STAR [5]. MAPS and DMAPS integrate the sensing element and readout electronics into the same die. This reduces the manufacturing complexity, cost and material budget. Given their advantages, DMAPS can be expected to replace HPS in most applications.

At an increased distance from the collision point (after the tracker) the vertex detector is located. Here, ATLAS, BELLE-2 and CMS employ passive strip detectors. These have significantly lower manufacturing costs than MAPS or HPS. Due to their simplicity, they additionally offer a high manufacturing yield and can cover large areas. However, due to the desire to increase the occupancy in experiments, there is ongoing work to replace the strip detectors with pixel sensors.

Significant R&D effort is invested at the moment to improve DMAPS, since it can be expected that these will eventually replace both HPS and passive strip sensors in many applications. One example is the BELLE-2 VXD upgrade, where the optimized Belle II pixel sensor (OBELIX) DMAPS is one of the candidate detectors for replacing both the pixel detector and the silicon vertex detector with one unified detector [6] (Other examples include the ALICE ITS3 [7] and a range of HV-CMOS projects [8, 9]).

In regard to substrate materials, silicon is currently dominant for semiconductor detectors. Its main advantages are the availability of low cost wafers and high performance semiconductor processes. However, from a physical perspective silicon is not an ideal detector material since, for example, the dark current at room temperature is high. This renders the detection of small signals a challenging task. Thus, alternatives are under investigation, where silicon carbide is (SiC) a very promising candidate [10]. SiC is currently being adopted by an increasing number of semiconductor companies such that high quality substrates are available at moderate costs [11, 12]. Furthermore, foundry services for such substrates are becoming available [13]. As a detector, compared to silicon, SiC promises better time resolution due to its larger saturation velocity $(200 \,\mu m \, ns^{-1} \, versus)$ $100 \,\mu m \, ns^{-1}$ for Si) [14]. Further, due to its low leakage currents after exposure to radiation, it promises to reduce power consumption [14, 15]. As a consequence,

SiC is currently gaining substantial attention from the research community [16].

In this work we summarize our contribution to the development of silicon DMAPS which has been described in more detail in [17] and [6]. Further, we present a novel readout frontend for SiC detectors. In the realm of DMAPS we have contributed to the end of column (EOC) circuit of the RD50-MPW3 ASIC [17]. Further, we are working on the on-chip data processing in the Optimized Belle II pixel sensor (OBELIX) geared towards the Belle 2 experiment [6]. In the realm of silicon carbide we are working on a primary beam monitor consisting of passive SiC strip detectors. For the readout of SiC strip detectors we present an optimized transimpedance amplifier (TIA) circuit. Parts of the presented work were previously published in [18].

2 Depleted Monolithic Pixel Sensors (DMAPS)

2.1 RD50-MPW3

The DMAPS sensor developed withing the RD50 collaboration is implemented in the Lfoundry 150 nm (LF15A) process. A cross-section through the process is given in Fig. 1. The sensor uses a fully depleted substrate for particle detection. The depletion is attained by applying a high voltage between the front side electronics and a backside electrode attached to the thinned-down substrate. Charge collection is performed using the large collection electrode approach. The depletion zone is isolated from the readout electronics via a very deep n-well which can be positioned below a deep p-well enabling isolation of both n-mos and p-mos transistors. This is one of the features of the LF15A process [17].

The pixel size of the chip is $62 \times 62 \mu m^2$. The output of a large collection electrode is amplified using a charge sensitive amplifier and shaped. A comparator is used to detect a particle transition. In the case of such an event the status of the global clock is stored in the in-pixel random access memory (RAM) to enable time stamping and time-over-threshold (ToT) measurements. Pixels are read out via a shared column bus, where the in-pixel logic enables pixel masking to prevent dead pixels from blocking the column bus. Each column has an EOC circuit in which events are stored and made available for readout via a wishbone



Fig. 1 Cross section of the LF15A process employed for RD50-MPW3 chip. A very deep n-well implantation acts as collection electrode for charges generated by particle transitions. An additional deep p-well isolates the CMOS transistors

bus. The time resolution of the application specific integrated circuit (ASIC) is 40 ns [19].

The EOC features two readout modes: The first mode uses a simple priority logic, where pixels with a higher address are prioritized. As a consequence those with lower addresses are more susceptible to loosing events in high-occupancy situations. Therefore, an alternative mode, the so-called FREEZE mode, was implemented where the readout of each pixel is frozen until the whole double column has been read out which leads to equal treatment of all pixels. The data from an event generated in a pixel consist of timestamps for the leading and trailing edges and the pixel address [17].

2.2 OBELIX

The OBELIX sensor is implemented in the TowerJazz 180 nm process. In contrast to the RD50-MPW3 ASIC the design utilizes a small collection electrode [20]. The OBELIX sensor is one of four proposals for the (partial) replacement of the VTX detector of the BELLE-2 experiment. OBELIX is derived from the existing TJ-Monopix2 chip. The sensor will feature a pixel pitch between $30-40 \,\mu\text{m}$ and a timestamp accuracy of 25 ns. In contrast to TJ-Monopix2, OBELIX will have a triggered readout architecture enabling a trigger rate of up to $30 \,\text{kHz}$. [6]

3 Moving from Silicon to Silicon Carbide

3.1 Silicon Carbide (SiC) Particle Sensors

SiC has the favorable property that its dark current does not substantially increase after an exposure to ionizing radiation. We measured the current through $3 \times 3 \text{ mm}^2$ SiC particle detectors containing a 50 μ m thick epitaxial layer before and after neutron irradiation with fluences up to $10^{16}n_{eq}/cm^2$ [21]. The measurement results of un-irradiated and irradiated detectors are given in Fig. 2. They reveal, that the dark current remains below 1 pAmm⁻² in all cases. A comparison to the current spike generated when a single particle passes through the detector (at least $0.5 \,\mu\text{A}$) shows, that the dark current is negligible even for large detector areas. Consequently, the readout circuit does not need current compensation when accessing the detector. It further enables, if desired, a DC coupling between detector and readout circuit.

This property enabled us the development of sensors that can detect both single particles and particle fluxes, where single particles can not be discriminated anymore. We are aiming to deploy such a device at Medaustron, a cancer treatment center, which provides various particle rates: In the kHz range particle detector tests are run, whereby detectors such as the RD50-MPW5 are exposed to beams of varying intensity and energy to verify their performance. In this mode, single particle counting is realized by detect-



Fig. 2 Dark current through a $3 \times 3 \text{ mm}^2$ SiC detector pad for a neutron fluence of $10^{16} n_{eq}/\text{cm}^2$. The dark current remains below 1 pAmm⁻² under all circumstances

ing current spikes. Particle-rates in the GHz range are used for patient treatment and biological research. Non-SiC based beam monitors currently in operation at Medaustron are only able to operate either at clinical rates or in single particle detection mode up to approx. 5MHz, while the novel SiC based monitors will be able to handle both simultaneously.

Due to process limitations, i.e., the absence of advanced complementary metal-oxide-semiconductor (CMOS) processing options, SiC is still restricted to passive sensors, e.g., strip detectors, or HPS. Nevertheless, for passive sensors suitable processes, for example the dedicated process for SiC detectors developed by CNM are already available [22]. The process developed by CNM consists of a single p-implant into the n-substrate and a single metal layer. Consequently, only five masks are required, leading to low costs for prototype production. A cross-section through the process is given in Fig. 3. Together with CNM we have designed several test vehicles for radiation hardness studies and numerous prototype strip detectors for our beam monitor.



Fig. 3 Cross section through a pad detector manufactured using the CNM SiC process. The process only needs 5 masks resulting in acceptable prototyping costs

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Fig. 4 Charges measured while a SiC pad detector was bombarded with protons having an energy of 62.4 MeV. One ADC count corresponds to 5.5 aC. The Langauss fit corresponds to the expected charge spectrum in the absence of noise. The discrimination of single particles is possible

3.2 SiC Sensor Readout

Two approaches can be followed when building a particle detector that can work from the kHz to the GHz range. The first approach is to split the frequency range in parts. For low frequencies, the detector counts events from single particles impinging onto the detector. For higher frequencies, the current through the detector is measured. The detector current is proportional to the particle fluence of the beam. The second approach relies on counting particles over the full range of frequencies. This requires a sufficiently fast front-end for detector readout. We followed both approaches.

For building a readout system that counts particles at low fluences and measures current at high fluences, we employed the AD8488 frontend for X-Ray panels. This integrated circuit (IC) provides current integrators for 128 channels which have a selectable gain and a nominal equivalent noise charge (ENC) below 1000 elementary charges. For single particle detection, the gain of the AD8488 is set to it's maximum. For each sample, based on the measured charge we determine if a particle was present or not. At higher particle rates such as clinical rates, the measured charge is taken as a measure for the number of particles passing during the sample integration time. Fig. 4 shows a histogram of detected charges in single particle detection mode. One ADC count corresponds to 5.5 aC. It was measured using a SiC pad detector with a 50 μm thick active zone was hit by protons with an energy of 62.4 MeV (corresponding to 5 minimum ionizing particles, MIP). A Landau distribution convoluted with the Gaussian distribution of the noise (Langauss) was fitted to the histogram. The Langauss fit corresponds to the expected charge spectrum in the absence of noise. It can be observed that the signal to noise ra-



Fig. 5 Profile of the 252.7 MeV proton beam at clinical intensities. The profile has been acquired using a Si strip detector

tio (SNR) is not yet ideal and MIPs would be undetectable. However, when replacing the SiC pad with a thicker device the signal level is increased. If we simultaneously accept that only a fraction of particles can be detected, it is possible to employ the sensor for single particles detection. Specifically, we are aiming for detectors having a nominally 100 μ m thick active layer. The SNR for MIPs on this new detectors substrates is expected to be in range between 5 and 6.

The readout circuit was also tested in conjunction with a strip detector. Since our SiC strip detectors are still being manufactured, we used a Si strip having a thickness of 300 µm and a fill-factor of 50%. Fig. 5 shows the measured cross section through the beam, resolved in space and time at a sampling rate of 37 kHz. The nominal average particle rate was 1.6 GHz. The readout was performed using the same front-end as for the single particle case but with reduced sensitivity. It must be noted that after one day of performing measurements using the Si strip detector, the radiation led to a dark current as large as the signal from the high intensity beam, driving the system into saturation. Under the envisioned operating conditions for our SiC sensors we expect a sensor lifetime of more than 2 years.

For counting particles even at higher fluences we are developing a TIA based readout frontend. Commonly detectors are read out by utilizing a charge sensitive amplifiers (CSA) in the input stage. CSA have favourable noise characteristics. For a typical detector capacitance between 1 and 4 pF equivalent noise charges (ENC) below 100 electrons are documented in the literature [23]. However, the limited bandwidth of CSA make them unfavourable for our application. We expect pulses of a duration of 0.4 ns per particle for a 100 µm thick sensor. Attaching a CSA to such a detector would limit the speed of our frontend. Consequently, we opted for using a transimpedance amplifier (TIA) based readout front-end and optimized it for our SiC strip detectors. Given the limitations of processing technology available for SiC, the TIA is implemented on silicon.

The overall circuit of the detector and the main parasitic components are given in Fig. 6. The detector is connected between the input of the TIA and a high voltage supply (HV). The connection between the de-



Fig. 6 Integration of the TIA with the detector (*top*) and small signal simulation model used for the detector (*bottom*). The detector is supplied with a high voltage to fully deplete the n-EPI layer of the PIN-Diode. Impinging particles generate carriers in the depleted part of the diode. The generation of carriers is modelled as current source I_D (*bottom right*). The main parasitic component included into simulations is the diode capacitance C_D . The current pulses from the diode are amplified using the TIA and recorded using an oscilloscope

tector and the TIA will be established by directly bonding the SiC detector to the silicon TIA, minimizing parasitic resistance and inductance. When simulating the detector the detector was thus modelled as current source (I_D) with a parallel capacitance (C_D) without taking into account parasitic inductances.

We chose a TIA design based on the "inverter with active common-drain feedback" (ICDF) circuit presented in [24]. Compared to the traditional regulated cascode (RGC)-TIA circuit, the ICDF has a larger gain in the feedback path. This reduces the input impedance and suppresses noise. A similar approach was used in [25], where the amplification was improved by introducing two cascodes in the inverter.

The TIA (circuit level implementation shown in Fig. 7) was implemented in a 130 nm silicon CMOS process (Skywater SKY130A). The Skywater SKY130A process was selected due to its compatibility with open source electronic design automation (EDA) tools. The design was developed using exlusively open source EDA tools to reduce tooling costs. Transistor sizes are provided in Fig. 1. Our design goal was to achieve a sufficient bandwidth for detecting the expected current pulses from a 100 μ m thick SiC sensor (at least 1.2 GHz over all temperatures and corners) while simultaneously minimizing noise and input impedance.

To attain these design goals, a combination of the circuits given in [24] and [25] was implemented. Compared to [25] the smaller process node made the addition of two cascode transistors to the inverter unfavourable. Instead, only one cascode was introduced to the n-channel part of the inverter, while the cascode was omitted for the p-mos transistor. When connecting the gate of the cascode transistors directly to VDD and GND, as shown in [25], simulations revealed



Fig. 7 Schematic of the TIA. The circuit combines elements of the circuits presented in [24] and [25]. Similarly to [25], the ICDF presented in [24] was augmented by one cascode transistor in the inverter. In contrast to [25] for the used process node only one cascode transistor is more favorable than two

that process variations cause significant changes in the operating points of M3 and M4. To suppress this effect we introduced a biasing circuit (see Fig. 8). For the process corners with nominal and high threshold voltages, the circuit sets the gate voltage of M3 close to VDD. For process corners where M3 has a low threshold voltages, the gate voltage of M3 is reduced, limiting the transverse current and keeping the drain source voltage of M3 and M4 within acceptable limits. The chosen sizes are again given in Table 1.

The TIA features two outputs: Out1 and Out2 (cf. 7). The authors in [24] used Out1 as the signal was larger.



Fig. 8 Biasing circuit for the cascode transistor and second copy of the TIA. The biasing circuit counters the impact of temperature and process variations. The second copy of the TIA provides a reference voltage for the output differential amplifier enabling DC current measurements

Transistor	Width	Length	Transistor	Width	Length
	/µm	/µm		/µm	/µm
M1, M1B	120	0.15	M6, M6B	240	0.15
M2, M2B	360	0.15	M7	14	0.15
M3, M3B	80	0.15	M8	40	0.15
M4, M4B	80	0.15	M9	240	0.5
M5, M5B	240	1	M10	240	0.15

Table 1Transistor Dimensions

In our design the trans-conductance of M1 was increased to account for the larger input capacitance, reducing the amplitude at Out1. Thus, in our design we employ the output Out2. We chose to employ R1 as transimpedance determining element instead of a transistor as done in [24] and [25]. While a transistor



Fig. 9 GDS layout of two TIA channels. One biasing circuit supplies both channels. Each TIA channel is composed of two copies of the TIA and a differential output driver. One of two TIAs is attached to the detector, while the other provides a zero-current output voltage as reference for the differential output driver. The submitted chip contains 9 times 2 channels totaling to 18 channels with an average channel pitch of $250 \,\mu\text{m}$ matched to a SiC strip detector



Fig. 10 Post layout simulation of the bandwidth of the complete TIA including output driver over process corners, device mismatch and temperatures. The input was loaded with a 3 pF capacitor

promises to increase the usable bandwidth, precision resistors reduce the process dependence of the transimpedance. Since our design is not primarily optimized for bandwidth and the use of a resistor did not result in any reduction of bandwidth, we opted for this variant. The chosen value for R1 was $1.9 \text{ k}\Omega$.

We also intend to measure DC currents. For this purpose a copy of the TIA were implemented. The copy provides the output voltage of the TIA when no input current is applied. A series of differential amplifiers is used to match the signal to the intended output impedance of 50Ω . Similarly to [24], the differential amplifier chain has 3 stages. It adds up to 10 dB of gain to the TIA and has a nominal output impedance of 50Ω . The copy of the TIA was integrated together with the biasing circuit and is shown in Fig. 8. The TIA output for the input of the differential amplifier is given at Out_ref. The Bias voltage for the main TIA is provided at Bias2.

The overall gds layout is shown in Fig. 9. For frequencies up to 1.2 GHz the input impedance is below 40Ω for all temperatures. Thus, an input capacitance of up to 3 pF can be permitted. Post layout simulations show that the bandwidth of the TIA including the output driver is between 1.2 and 1.8 GHz depending on process variations and temperature when loaded with a 3pF detector capacitance and no output load. The temperature and process dependence of the bandwidth is given in Fig. 10. The simulated input referred noise is shown in Fig. 11. Below 1.2 GHz it is below $30 \text{ pA} \sqrt{\text{Hz}}$, while a minimum of $10 \text{ pA} \sqrt{\text{Hz}}$ is achieved for frequencies between 10 MHz and 200 MHz. The detector capacitance significantly increased the input referred noise. When no detector capacitance is included in the simulation, the input referred noise was below 15 pA $\sqrt{\text{Hz}}$. The power consumption of the overall circuit was simulated to be below 72 mW including the output driver. One TIA consumes 18 mW or less.



Fig. 11 Post layout simulation of the input referred noise of the implemented TIA. The input was loaded with a 3 pF capacitor. The noise is below $30 \text{ pA} \sqrt{\text{Hz}}$ for frequencies up to 1.2 GHz with a minimum of $10 \text{ pA} \sqrt{\text{Hz}}$ between 10 MHz and 200 MHz

	Companson of ICDF-TAS				
Reference	[25]	[24]	This work		
BW/GHz	6	7	1.2		
Noise/pA $\sqrt{\text{Hz}}$	23	22 to 31	10 to 30		

When integrating the TIA into a detector system, we expect to implement 512 TIA channels, resulting in a total power consumption of 4.6W.

4 Conclusion

We have reported on our activities on the development of particle detectors. In the domain of DMAPS we have contributed the EOC circuit to the RD50-MPW3 ASIC and are currently working on the on-chip digital processing circuit for the OBELIX pixel sensor.

Given the attractive properties of SiC as a detector material we are working on SiC based detectors. As a first application we are using SiC for a primary beam monitor. In this specific application SiC outperforms Si due to its negligible dark current even if exposed to radiation. In our case, detectors can tolerate fluences of up to $10^{16}n_{eq}/cm^2$ while still maintaining dark current levels 3 orders of magnitude smaller than the signal generated by particles.

We are developing two analog front-ends for reading out SiC strip detectors. One frontend uses an offthe-shelf IC for X-Ray panels which counts single particles at low fluences and measures a detector current proportional to the fluence at higher fluences. For counting particles at all expected fluences, we chose to implement a TIA for amplifying the signals from the detector. We expect the detector to emit pulses of approx. 0.4 ns and thus optimized the bandwidth of the TIA to a bandwidth of 1.2 GHz. Due to it's low input impedance we chose a ICDF-TIA topology for the TIA. For frequencies up to 1.2 GHz, the TIA exhibits an input impedance of 40Ω . We expect the TIA to be loaded with a detector capacitance of up to 3pF. When loaded with a 3pF detector, the noise is below 30 pA $\sqrt{\text{Hz}}$ for frequencies up to 1.2 GHz. It reaches a minimum of $10 \text{ pA} \sqrt{\text{Hz}}$ between 10 MHz and 200 MHz. A comparison to other ICDF-TIAs is given in Table 2.

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Andreas Gsponer, was born in Visp, Switzerland, in 2000. He studied experimental physics at the University of Bern, working on novel beam monitors for medical applications in his bachelor's thesis and searches of the neutron EDM in his master's thesis. Since 2022, he has been pursuing a Ph.D. at the Institute for High Energy Physics (HEPHY) of the Austrian Academy of Sciences (OEAW) in Vienna. His work includes the experimental measurement and characteriza-

tion of advanced silicon carbide detectors, with a focus on radiation hardness.



Patrick Sieberer, was born in 1994 in Scheibbs, Lower Austria. After finishing the doctoral thesis in Technical Physics about 'CMOS detectors for high energy physics' at TU Wien and HEPHY, he moved to Paul Scherrer Institut (PSI) in Switzerland to work on detectors for x-ray applications. His interest in ASIC design already evolved during a oneyear long research stay at CERN as part of his master thesis on detector readout systems. While focussing on digital design dur-

ing the doctoral thesis, he his now designing analog circuits and working as ASIC designer for different kinds of (experimental) CMOS detectors.



Maximilian Babeluk, was born in 1996 in Vienna, Austria. After graduating at a high school with focus on medical- and healthcare-engineering, he studied physics at the Technical University of Vienna. He completed his master of sciences with a thesis about the process quality control of outer tracker silicon sensors for the CMS phase 2 upgrade in October 2021, Currently, he is employed as PhD student at the Institute of High Energy Physics of the Austrian Academy of Sci-

ences to contribute to the design and testing of the OBELIX depleted monolithic active CMOS pixel sensor for the Belle II VTX Upgrade.



Thomas Bergauer, was born in Lower Austria in 1975. After studying technical physics at the Vienna University of Technology, he became a research associate at the Institute of High Energy Physics at the Austrian Academy of Sciences. He has headed the "Semiconductors" working group there since 2008 and the Department of Detector Development since 2019, where he is responsible for operating the experimental facilities. In this role, he has successfully ac-

quired a number of third-party funds and supervises students as part of their Bachelor's and Master's theses and dissertations. The developments of his working group are used in the CMS experiment at CERN, the Belle-II experiment at KEK and for medical applications at the MedAustron Ion Therapy Center.