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GriDConv – control, design, and experimental verification of a lab-scale high-voltage DC-DC converter

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Abstract The advent of the Modular Converter technology allows building multi-terminal high-voltage DC grids. In order to interconnect DC grids with different voltage levels, highly efficient and compact high-voltage DC-DC (HVDC) converters are required. This paper presents the control and design of a transformerless high-voltage DC-DC converter, which has been designed and built within the framework of the research project *GriDConv* at the Graz University of Technology. The converter basically consists of high-voltage half-bridges in combination with a series of submodules with full-bridge technology. A dedicated control strategy for the converter is developed, which allows advantageous soft switching of the high-voltage half-bridges, which considerably reduces switching losses of the half-bridges. In addition, a balancing strategy for the individual cell voltages as well as a control of total cell voltage are presented. The developed control strategies are discussed in detail and, in the end, verified through experiments on a constructed 50 kW lab-scale hardware demonstrator.

Keywords High-voltage direct current system, HVDC · Power electronics · DC-DC converter · Multilevel converter · Converter control

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GriDConv – Regelung, Design und experimentelle Verifikation eines Hochspannungs-DC-DC-Wandlers im Labormaßstab

Zusammenfassung Die Entwicklung der Modular Multilevel Converter-Technologie erlaubt es, Hochspannungs-Gleichstromnetze mit mehreren Zu- und Abgängen zu realisieren. Um DC-Netze mit unterschiedlichen Spannungswerten verbinden zu können, werden hocheffiziente und hochkompakte Hochspannungs-DC-DC-Wandler benötigt. Diese Arbeit behandelt den Entwurf und die Regelung eines Hochspannungs-DC-DC-Wandlers ohne Transformator, welcher im Zuge des interdisziplinären Forschungsprojekts „GriDConv" institutsübergreifend an der Technischen Universität Graz entwickelt wurde. Der DC-DC-Wandler besteht aus verschachtelten Hochspannungshalbbrücken in Kombination mit in Serie geschalteten Submodulen in Vollbrückenausführung. Eine Regelungsstrategie wird entwickelt, welche vorteilhaftes weiches Schalten der Halbbrücken und somit eine beträchtliche Reduktion deren Schaltverluste erlaubt. Darüber hinaus wird eine Regelungsstrategie zur Symmetrierung der Submodulspannungen sowie die Regelung der Gesamtspannung der in Serie geschalteten Zellen vorgeschlagen. Die vorgeschlagenen Regelungsstrategien werden im Detail untersucht und schlussendlich durch Messungen an einem skalierten 50-kW-Labordemonstrator verifiziert.

Schlüsselwörter
Hochspannungsgleichstromübertragung, HGÜ, HVDC · Leistungselektronik · DC-DC-Wandler · Multilevelkonverter · Regelung von Konvertersystemen

1 Introduction

High-Voltage DC (HVDC) technology emerged to be a great alternative to classical AC transmission systems for energy transmission over large distance, connection of offshore wind parks and interconnection of asynchronous AC power systems [1–3]. Whereas HVDC-transmission systems based on Line Commutated Converters (LCC) only allow point-to-point connection the application of either Voltage Source Converters (VSC) or Modular Multilevel Converters (MMC) in general allow to build multi terminal HVDC-grids [4]. Multi-terminal DC-grids on high-voltage or medium-voltage level are usually designed independently of each other, i.e. voltage levels of different grids may be quite different. To connect different HVDC-grids with different voltage levels highly efficient DC-DC converters are therefore required to adapt the different voltage levels. The required DC-DC converters come along with the possibility to actively control the power flow between the two grids and the possibility for fault isolation. Next to the requirement of high efficiency also other very stringent demands for these DC-DC converters exist such as high reliability, small physical size, bidirectional power flow and DC-fault blocking capability as well as low cost.

DC-DC converters for HVDC-grids can in general be separated in isolated and non-isolated approaches. A comprehensive overview of different concepts for both isolated and non-isolated approaches can be found in [5]. Isolation of the DC-grids may be required for grounding or safety reasons and allow connection of DC-grids with different grounding configurations. Isolated HVDC-DC converters are beneficially implemented using a Dual Active Bridge (DAB) approach where the primary and secondary switches are implemented using MMC bridge-legs in combination with a medium frequency transformer for isolation [6, 7]. The design of the applied high-power high-voltage transformer with non-sinusoidal voltage and current waveform is a challenging task and the resulting transformer is bulky, expensive and reduces efficiency of the DC-DC converter.

In applications where no isolation between the DC-grids is required a DC-DC converter without isolation can be used where a higher efficiency can be achieved by smaller size of the converter. Also for non-isolated DC-DC converter for interconnection of HVDC-grids several topologies have been presented [5, 8]. A family of very promising topologies without transformer have been presented in [9] and further discussed in [10]. In course of an interdisciplinary research project "griDConv" at the Faculty of Electrical and Information Engineering (ETIT) at Graz University of Technology (TU-Graz) with the collaborating institutes Electric Drives and Machines Institute, Institute of Electrical Power Systems, Institute of High Voltage Engineering and System Performance, Institute of

Electronics and Institute of Automation and Control one of the basic approaches given in [9] has been analyzed in detail and a lab-scale hardware demonstrator has been designed and constructed. Details on the selected topology as well as the constructed lab-scale converter can be found in [11].

In this work control and design of the lab-scale high-voltage DC-DC converter is presented where especially soft-switching of the high-voltage half-bridges as well as cell voltage balancing is addressed in detail. In Sect. 2 the converter topology, the basic operating principle as well as the converter design is discussed. The commutation process of high-voltage half-bridges is analyzed in Sect. 3, where an algorithm for soft-switching is introduced and corresponding experimental results are presented to verify the proper operation of the approach. Sect. 4 deals with the control and balancing of the DC-link voltages accompanied by experimental results taken from the constructed lab-scale demonstrator and in Sect. 5 final conclusions are derived.

2 Converter Topology and Operating Principle

As outlined above, the converter shall enable power exchange between two high-voltage DC-grids, with different voltage levels. The terminal connected to the grid with the higher nominal voltage is referred to as the input (index 1) and the other terminal, connected to the grid with lower nominal voltage, is referred to as the output terminal (index 2) of the converter – even though, bidirectional power flow is mandatory.

The selected converter topology is depicted in Fig. 1 and consists of three identical legs a, b and c. Each leg comprises a half-bridge (symbolized as an alternating switch in Fig. 1), a stack of N_{FB} series connected full-bridge modules (variable voltage source in Fig. 1) and an inductor. The half-bridge is connected to the input terminal (v_{HV1}) and its switched node current feeds the output terminal via the modules stack and the inductor.
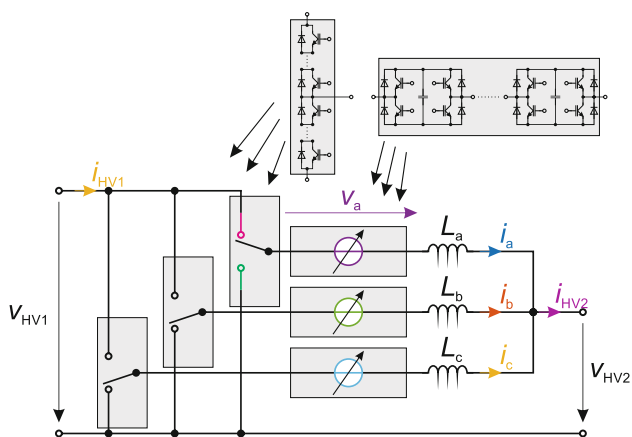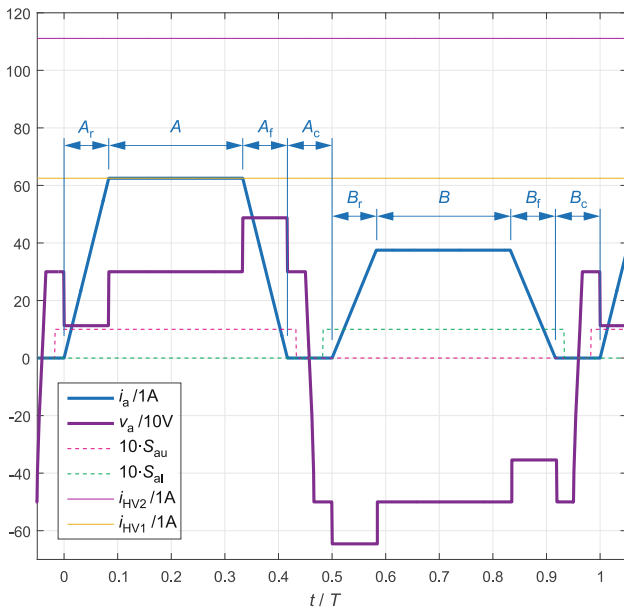

Fig. 1 Principle circuit diagram of the High-Voltage DC-DC converter

Fig. 2 Principle voltage and current waveforms for leg a of the High-Voltage DC-DC converter from top to bottom: Leg current i_a, voltage output of the adjustable voltage source v_a, upper and lower switch control signals S_{au} and S_{al}, output and input terminal currents i_{HV2} and i_{HV1}. The magnitudes represent the nominal operating point of the lab scale converter demonstrator as listed in Table 1: $v_{HV1} = 800\,V$, $i_{HV1} = 62.5\,A$, $v_{HV2} = 500\,V$ and $i_{HV2} = 100\,A$

Thus, the current flowing into the input terminal (i_{HV1}) equals the sum of the upper switch currents of the three half-bridges, and the current flowing out of the output terminal (i_{HV2}) equals the sum of the three inductor currents. Constant (DC) converter input and output currents can be achieved with three periodic waveforms of the inductor currents, being identical in shape and shifted in time by one third of the period. If each of the inductors carries the input current for one third of the period, while the according alternating switch is in the upper position, the two other alternating switches need to be in the lower position and the according inductor currents need to sum up to the output current. Thus, the inductor current can be set to the output current minus the input current ($i_{HV2} - i_{HV1}$) for another third of the period. The remaining third of the period can be distributed for ramping the currents down to zero and allow for soft-switching of the half-bridges. Off course, in order to maintain constant input and output currents, the inductor currents need to synchronously ramp up to the desired values, resulting in the waveforms shown in Figs. 2 (for one leg) and 3 (for the three legs).

The demand for constant input and output current, together with the smooth transition of input and output currents from one leg to the other, followed by a soft transition of the half bridge switching state results in a minimum number of three legs. E.g. while leg a provides constant input current, leg b reduces and leg c increases its current, maintaining a constant
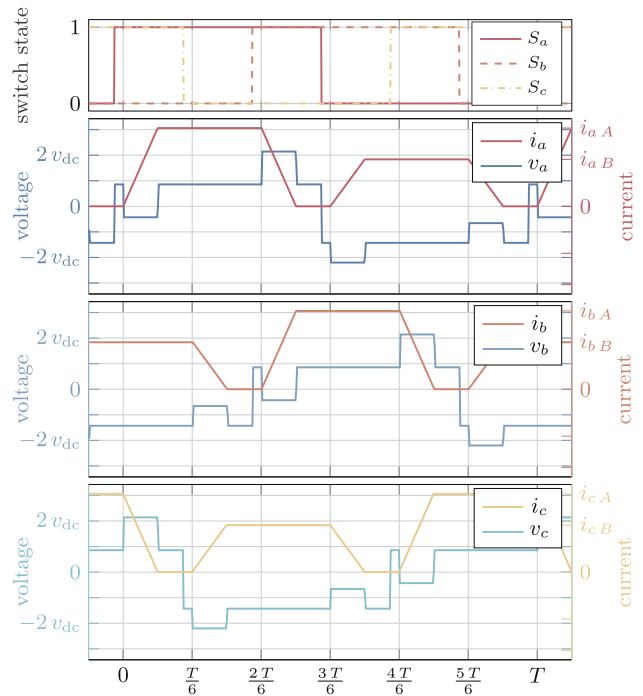
Fig. 3 Idealized voltage and current waveforms for the three legs of the converter, together with the switching states of the three half-bridges. As in Fig. 2, the magnitudes represent the nominal operating point of the lab scale converter demonstrator as listed in Table 1: $v_{HV1} = 800\,V$, $i_{HV1} = 62.5\,A$, $v_{HV2} = 500\,V$ and $i_{HV2} = 100\,A$. However, the timing is modified for constant magnitude of di/dt, resulting in different length of the time intervals with zero leg current

sum. Then leg b can initiate the soft transition of the half bridge (rising slope) and is able to take over the input current from leg a afterwards. With zero current, leg a initiates its negative transition of the half bridge switching state and can afterwards take over the current from leg c accordingly.

Adding one more leg to the topology would introduce an additional time interval with zero current for each leg and by that reduce the component utilisation and increase cost, without according gain in functionality or performance.

Neglecting any losses, the input and output currents are related to the according terminal voltages by the power transfer

$$p_{HV1} = i_{HV1} \cdot v_{HV1} = i_{HV2} \cdot v_{HV2} = p_{HV2} \quad (1)$$

$$i_{HV2} = i_{HV1} \frac{v_{HV1}}{v_{HV2}}. \quad (2)$$

According to the definition of input and output voltage levels, the output current magnitude is always bigger than the input current magnitude. The inductor current amplitudes can be derived using

$$\begin{aligned} i_{jA} &= i_{HV1} \\ i_{jB} &= i_{HV2} - i_{HV1} \end{aligned} \quad (3)$$

Table 1 Constant voltage levels of the adjustable voltage sources and leg currents within one operation cycle

Int.	Voltage level	Leg current
A_r	$v_{HV1} - v_{HV2} - L\frac{i_{HV1}}{t_{Ar}}$	$0 \rightarrow i_{HV1}$
A	$v_{HV1} - v_{HV2} = v_{jA}$	$i_{HV1} = i_{jA}$
A_f	$v_{HV1} - v_{HV2} + L\frac{i_{HV1}}{t_{Af}}$	$i_{HV1} \rightarrow 0$
B_r	$-v_{HV2} + L\frac{i_{HV2} - i_{HV1}}{t_{Br}}$	$0 \rightarrow i_{HV2} - i_{HV1}$
B	$-v_{HV2} = v_{jB}$	$i_{HV2} - i_{HV1} = i_{jB}$
B_f	$-v_{HV2} - L\frac{i_{HV2} - i_{HV1}}{t_{Bf}}$	$i_{HV2} - i_{HV1} \rightarrow 0$

with i_{jA} and i_{jB} being the inductor current values in leg $j \in \{a, b, c\}$ during the time intervals A and B, as indicated in Fig. 2. The time intervals for ramping up to and down from these currents are indicated as A_r, B_r, A_f and B_f in Fig. 2. Thereby, the time intervals marked by A_r and A sum up to one third of the signal period T. The same holds true for the intervals indicated by B_r and B ($t_{Ar} + t_A = t_{Br} + t_B = \frac{T}{3}$). The remaining parts of the half periods $t_{Ac} = \frac{T}{2} - t_{Ar} - t_A - t_{Af} = \frac{T}{6} - t_{Af}$ and $t_{Bc} = \frac{T}{2} - t_{Br} - t_B - t_{Bf} = \frac{T}{6} - t_{Bf}$ are available for switching the half-bridge from the upper to the lower (t_{Ac}) and from the lower to the upper (t_{Bc}) position respectively. These commutation processes will be described in detail in Sect. 3.

Dedicated voltage waveforms have to be generated across the inductors in order to force the currents to follow their reference signals. Neglecting losses again, these voltage waveforms differ from zero only during the rising and falling slopes of the inductor currents (i.e. intervals A_r, A_f, B_r, B_f). A current control, acting on the adjustable voltage sources will therefore establish voltage waveforms for the controlled voltage sources as shown in Fig. 2. The voltage levels that need to be generated by the adjustable voltage sources in the individual intervals are listed in Table 1. As can be seen from Fig. 2 and Table 1, there is no odd symmetry in the voltage waveform, nor an even symmetry in the current wafeform in a general load situation. Only if the output voltage equals one half of the input voltage ($v_{HV2} = \frac{1}{2} v_{HV1}$), then positive and negative voltage amplitudes show equal magnitudes and the current amplitudes in both half periods match each other.

As long as the inductor current remains constant, the voltage of the adjustable voltage source only needs to compensate for the difference of the input and output voltage (A) or the negative output voltage level (B) respectively. The steep voltage slopes in the intervals with zero inductor current indicate the change of the switching state of the half-bridge.

As the individual full-bridge modules are equipped with DC-link capacitors without any power source connected, the adjustable voltage sources are capable of supplying reactive power only. Thus, the energies and therefore voltages of the individual module capacitors need to be balanced within one operating cycle. For a given direction of power flow (e.g. from input to output, as indicated in Fig. 1) the direction of the inductor current remains constant (and positive, according to the definition in Fig. 1). The output voltage of the modules stacks represented by the variable voltage sources, however, need to change their polarity twice within one period. This results in reactive power flow for these variable voltage sources. Integrating the instantaneous power in one of the adjustable voltage sources over one operation cycle, using the waveforms shown in Fig. 2 and the current and voltage levels, given in Table 1, results in:

$$W_j = \int_{t=0}^{T} i_j \cdot v_j dt = i_{jA}\left[\frac{1}{2}t_{Ar}\left(v_{jA} - L\frac{i_{jA}}{t_{Ar}}\right)\right.$$
$$+ t_A v_{jA} + \frac{1}{2}t_{Af}\left(v_{jA} + L\frac{i_{jA}}{t_{Af}}\right)\right]$$
$$+ i_{jB}\left[\frac{1}{2}t_{Br}\left(v_{jB} - L\frac{i_{jB}}{t_{Br}}\right) + t_B v_{jB} + \frac{1}{2}t_{Bf}\left(v_{jB} + L\frac{i_{jB}}{t_{Bf}}\right)\right]$$

with W_j denoting the energy, that is consumed by voltage source $j \in \{a, b, c\}$ within one signal period T. With the rise and fall times being equal within one section ($t_{Ar} = t_{Af} = t_{As}$ and $t_{Br} = t_{Bf} = t_{Bs}$), this results in

$$W_j = i_{jA}(t_{As} + t_A)v_{jA} + i_{jB}(t_{Bs} + t_B)v_{jB}$$
$$= \frac{T}{3}\left(i_{jA} v_{jA} + i_{jB} v_{jB}\right) \tag{5}$$
$$= \frac{T}{3}\left[i_{HV1}(v_{HV1} - v_{HV2}) + (i_{HV2} - i_{HV1})(-v_{HV2})\right]$$

which equals zero, as the input power equals the output power. Thus, the voltage and current levels for the waveforms, shown in Figs. 2 and 3 are defined, which enable constant power transfer between input and output ports of the converter, while maintaining reactive power flow inside the full-bridge modules stacks (controlled voltage sources).

2.1 Converter Design

The voltage levels to be provided by the full-bridge modules stacks (variable voltage sources) are given in Table 1. The maximum and minimum values appear in intervals A_f and B_f respectively, which typically will show lower magnitudes than the voltage v_{HV1} at the input terminal. However, in order to enable the topology to isolate faults on both sides and enabling black start from both sides, the maximum voltages, the full-bridge modules stacks need to supply, equal the input terminal voltage.

Considering a DC-link voltage of v_{dc} one full-bridge module can output $-v_{dc}$, 0 or $+v_{dc}$, and the maximum voltage, a stack of N_{FB} modules can supply, is $N_{FB} \cdot v_{dc}$. Thus, a minimum value for the number of needed modules can be defined as

$$N_{FB\,min} = \frac{v_{HV1\,max} + L\frac{i_{HV1\,max}}{t_{Af}}}{v_{dc\,min}} \tag{6}$$

Assuming, a few modules might fail (and be short circuited) between maintenance intervals, this minimum number of full-bridge modules within one stack can be increased to allow for redundancy and thus, enable uninterrupted operation.

Each half-bridge is built from two switches, which comprise N_{HB} semiconductor switches each. The minimum Number of these series connected semiconductors can be derived from the maximum voltage at the input terminal and the maximum allowable continuous operating voltage $v_{SC\,max}$ of the individual semiconductor switches:

$$N_{HB\,min} = \frac{v_{HV1\,max}}{v_{SC\,max}}. \tag{7}$$

As the current rating of the semiconductors, used in the full-bridge modules, is close to the one for the half-bridges, the same type of semiconductor switches might be used in both places. Assuming the same utilisation of the maximum blocking voltage in both places, the number of semiconductor switches, to implement the switches in the half-bridges $N_{HB\,min}$ will be slightly lower than the minimum number of full-bridge modules $N_{FB\,min}$ in one leg. Thus, the overall number of semiconductor switches needed for this topology is given by

$$N_{SC\,tot} = 3 \cdot (2 \cdot N_{HB} + 4 \cdot N_{FB}) \tag{8}$$

Due to the switching nature of the full-bridge modules, the adjustable voltage sources can only provide voltage magnitudes in integer multiples of the DC-link voltage (v_{dc}) – magnitudes in between can only be averaged in time over a switching period (T_s), with $f_s = \frac{1}{T_s}$ denoting the effective switching frequency. The effective switching frequency results from the number of available modules (N_{FB}) and the module switching frequency. With hundreds of modules, connected in series, the effective switching frequency may be rather high, even if the individual modules are switching only twice in a signal period ($f_s = N_{FB} \cdot f_{s\,FB} = \frac{N_{FB}}{T}$). Comparing the resulting AC-signals of the voltage source and the inductor current to those of a two level half-bridge, one can estimate an upper bound of the inductor current ripple (peak to peak value):

$$i_{L\,pp\,max} = v_{dc} \frac{T_s}{4\,L} \tag{9}$$

As explained above the adjustable voltage sources implemented by the stacks of full-bridges need to handle reactive power. Thus, their DC-link capacitors need to absorb energy in one part of the waveform period T, release it in another part and store it in between. The corresponding voltage ripple, caused by evenly distributing the stored energy among the N_{FB} modules, can be calculated by using (5):

$$\begin{aligned}
\Delta W_c &= \frac{C}{2} \left(v_{dc\,max}^2 - v_{dc\,min}^2 \right) \\
&= \frac{C}{2} (v_{dc\,max} - v_{dc\,min}) \cdot (v_{dc\,max} + v_{dc\,min}) \\
&= C \cdot \overline{v_{dc}} \cdot \Delta v_{dc} = i_{HV1} \cdot (v_{HV1} - v_{HV2}) \frac{T}{3\,N_{FB}} \\
&= (i_{HV2} - i_{HV1}) \cdot v_{HV2} \frac{T}{3\,N_{FB}}
\end{aligned} \tag{10}$$

with $\overline{v_{dc}} = \frac{v_{dc\,max} - v_{dc\,min}}{2}$ denoting an average value between minimum and maximum DC-link voltage.

The design might start at the maximum input voltage demand ($v_{HV1\,max}$) and the decision on the technology for the semiconductor switches used in the full-bridge modules. The module DC-link voltage is derived from the allowed blocking voltage utilisation of these semiconductor switches which can then be used in (7) to gain a first estimate for the number of full bride modules needed in a stack, neglecting the inductive voltage drop. With the demand for an upper bound of the current ripple the product of the leg inductance and the effective switching frequency ($L \cdot f_s$) can be derived by application of (9). Using the effective switching frequency ($f_s = \frac{N_{FB}}{T}$) in (10), the product of the DC-link capacitance, the voltage ripple and the effective switching frequency ($C \cdot \Delta v_{dc} \cdot f_s$) can be derived. Increasing the effective switching frequency would result in smaller passive components (three leg inductors and N_{FB} DC-link capacitors) but would also increase the switching losses and reduce system efficiency. An upper bound to this effective switching frequency may be given due to delays and jitter in the switching signals as well as in the switching processes of the semiconductor switches and by the bandwidth limits of the leg current measurements together with the according signal processing.

For applications with lower terminal voltages (e.g. medium voltage converter or Lab scale demonstrator) the number of full-bridges in one stack might be too low for achieving smooth leg current waveforms when switching the full-bridges only twice in a leg current period. In such cases, pulse width modulation can be applied in order to increase the effective switching frequency and maintain smooth current waveforms again. Assuming interleaved operation and symmetrical pulse width modulation for the N_{FB} full-bridges, the effective switching frequency is given by:

$$f_s = 2\,N_{FB} \cdot f_{PWM} \tag{11}$$

The period for the leg currents is then decoupled from this value and can be optimized separately.

The parameters for the constructed 50 kW lab-scale demonstrator described in [11] are summarized in Table 2.

A picture of the setup is given in Fig. 4. Please note that the lab-scale hardware demonstrator is used to

Table 2 Design parameters for the lab scale converter demonstrator described in [11]

First input voltage	v_{HV1}	800 V
First input current	i_{HV1}	62.5 A
Second input voltage	v_{HV2}	500 V
Second input current	i_{HV2}	100 A
Number FB modules per leg	N_{FB}	3
Nominal FB DC-link voltage	v_{dc}	350 V
Number HB modules	N_{HB}	2
DC-link capacitance FB	C	$2 \cdot 1.4$ mF
Leg inductance	L	3 mH
PWM switching frequency	f_{PWM}	10 kHz
Waveform period	T	5 ms
Half-bridge switching frequency	f_{HB}	200 Hz

verify the operating principle of the converter topology and is therefore neither optimized for power density nor efficiency. Implementing three full bridges per leg allows for demonstrating redundancy operation, as described above, by deactivating one of the full bridge modules and shorting its outputs.

Each power switch or switching cell is mounted on a dedicated heat sink where the three-columns represent the three bridge-legs of the converter. Four heat sinks are stacked for each branch where the upper lines represent the corresponding half-bridges and the three lines below are used to implement the three full-bridge modules. For the half-bridges, almost the same structure as for the full-bridge modules was used, with the difference that the four IGBTs are connected in series to achieve a higher blocking voltage. The upper and lower switch of the alternating switch in Fig. 1 is therefore formed by two IGBTs. The leg inductors, the input and output terminals as well as the PCB for measuring the leg currents and in- and output voltages are located at the bottom of the structure. The FPGA-based control board together with another board for in- and output current measurement are mounted at right hand side of the converter.
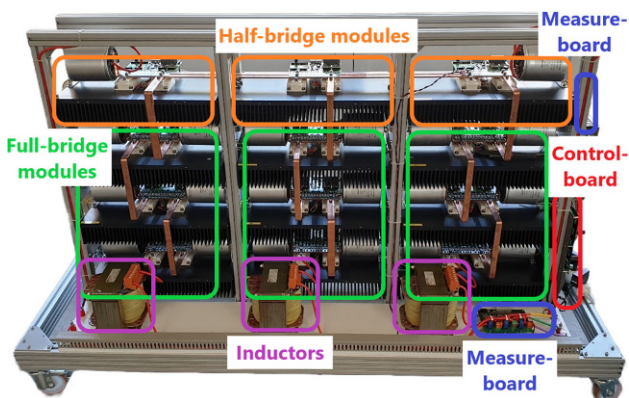

**Fig. 4** Image of the built 50 kW lab-scale converter demonstrator with $v_{HV1} = 800$ V and $v_{HV2} = 500$ V

3 Soft-Commutation of the High-Voltage Half-Bridges

To achieve scalability of the topology with respect to in- and output voltage as claimed in Sect. 2, several switching elements (e.g. IGBTs) have to be connected in series for the implementation of the input half-bridges to be able to block the input voltage v_{HV1}. Special measures must be taken to ensure a uniform distribution of the voltage across the individual semiconductor devices during commutation due to device-related variations in the unavoidable component capacitances. An unbalanced distribution of voltages would otherwise lead to the destruction of components and the subsequent failure of the converter.

To prevent this, a novel commutation strategy has been developed. This ensures that the commutation of the current from the series connection of the lower switches to the upper switches and vice versa is always performed in a soft-switching manner via the anti-parallel diodes. Thus, the voltage distribution during the switching process is only determined by the parasitic capacitances of the diodes. Deviations in the turn-on and turn-off speed of the individual IGBTs (e.g. due to component variation or varying driver delays) then also have no effect on the commutation process. By application of the soft commutation concept of the current the voltage distribution can be additionally balanced by external capacitors without increasing the switching losses of the half-bridge. This allows the series connection of several hundred components in real setups in order to be able to block voltages of hundreds of kilovolts.

The proposed method is discussed by an example commutation of the current in leg a, i_a, from the upper switching element to the lower switching element. This process, which is shown in Fig. 3 in the interval $\frac{2T}{6} < t < \frac{3T}{6}$, and a zoomed view of a commutation sequence is given in Fig. 5. It additionally includes
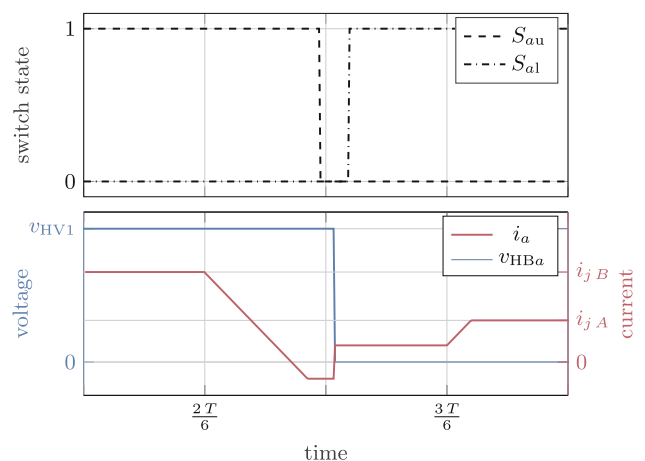
Fig. 5 Idealized waveforms of the electrical quantities and gating signals in leg a during a soft-switching commutation process
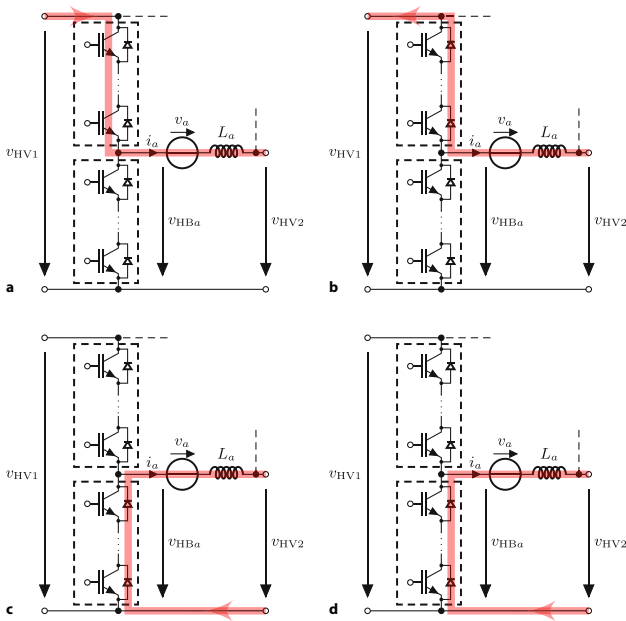
Fig. 6 Circuit diagram of leg a with commutation of the current i_a from the upper to the lower switch. **a** Initial state before commutation ($S_{au} = 1$, $S_{a1} = 0$, $i_a > 0$). **b** Commutation to body diodes ($S_{au} = 1$, $S_{a1} = 0$, $i_a < 0$). **c** Soft commutation to lowerswitches ($S_{au} = 0$, $S_{a1} = 0$, $i_a > 0$). **d** Soft turn-on of lower switches ($S_{au} = 1$, $S_{a1} = 0$, $i_a < 0$)

the gating signals for the series connection of the involved semiconductor devices S_{au} (upper devices) and S_{al} (lower devices). Fig. 6 depicts the corresponding current flow in leg a during the commutation at different time intervals.

1. At the beginning of the transition, the upper switch is turned on ($S_{au} = 1$) and $i_a = i_{HV1}$. Starting from time $t = \frac{2T}{6}$, i_a is ramped down by the current controller by corresponding control of the series connected full-bridge modules to a slightly negative current offset level compared to the waveform in Fig. 3.
2. As soon as $i_a < 0$A the current commutates from the upper IGBTs to their anti parallel diodes. The potential at the switch node of the half-bridge remains the same as the input potential of the upper voltage side ($v_{HBa} = v_{HV1}$). From this point on, S_{au} can be turned off softly with the current continuing to flow through the diodes.
3. If i_a is now brought to a slightly positive offset value via the current controller, the diodes of the upper switches start to block and the current causes the output capacitances of the upper devices, and potential external balancing capacitances to be charged. Simultaneously the relevant capacitances of the lower devices are first discharged via i_a. As soon as $v_{HBa} = 0$V, i_a commutates to the diodes of the lower switches.

4. At the end of the process, S_{al} is turned on with zero voltage (soft turn-on). The current continues to flow through the diodes as long as $i_a > 0$A.

The commutation process from the lower to the upper switching element in leg a during the interval $\frac{5T}{6} < t < T$ is performed in a similar manner. It should further be noted that the soft-switching commutation process is in principle independent of the inverter load conditions as it is actively initiated by the current controller and the full-bridge modules.

3.1 Lab-Scale Converter Implementation

The commutation scheme presented in the previous section was implemented and tested in the demonstrator. As the controllable voltage sources of the inverter are operated with PWM, as already described in Sect. 2, some precautions must be taken to ensure an error-free commutation process. Due to the existing current ripple, the commutation process initiated via the current control cannot be carried out with PWM operation, as the current would commutate back and forth around the actual commutation point resulting in a bouncing of v_{HBj} ($j \in \{a, b, c\}$) between v_{HV1} and 0 V. Therefore, the control is deactivated shortly before the planned commutation time. Depending on the measured voltages (input voltage, output voltage and DC-link voltage), a sufficient discrete number of modules are switched to positive or negative voltage so that a voltage $v_{Lj\,min}$ remains applied to the inductor in the respective leg. This causes the current through the inductor to change linearly by at least
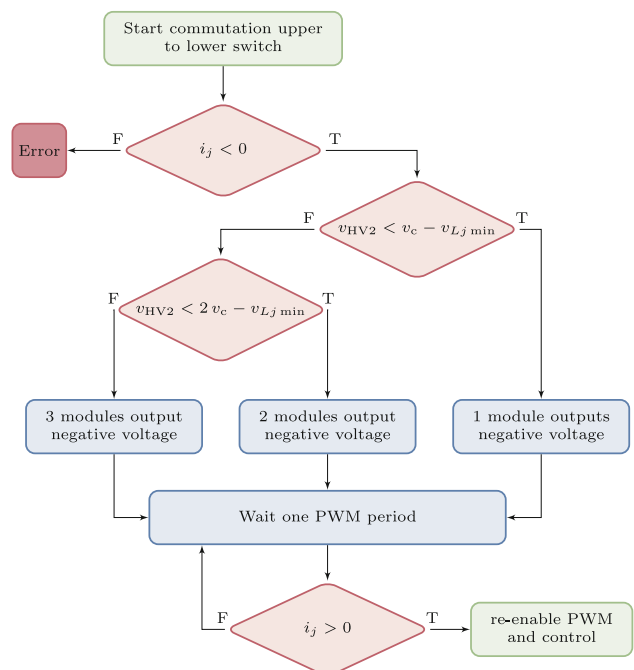

Fig. 7 Decision tree implemented in the control system for the commutation process from an upper to a lower switch

$\frac{v_{Lj\,\min}}{L}$. Once the current has commutated, the current control and PWM are re-enabled. Other safety measures implemented include detection of whether the current is actually positive before commutation and monitoring of $v_{\mathrm{HB}j}$. The basic structure of the implemented decision tree for the commutation from an upper to a lower switch can be seen in Fig. 7. For the commutation from a lower to an upper switch, the same principle with reversed current and module voltage polarity can be applied.

3.2 Experimental Results

A measured commutation process in leg a according to the presented scheme is shown in Fig. 8. The adjusted current offset around the junction was set to 5 A and $i_{a\,A} \approx 55\,\mathrm{A}$ and $i_{a\,B} \approx 25\,\mathrm{A}$ at $v_{\mathrm{HV1}} = 800\,\mathrm{V}$. It can be observed that the current ripple disappears shortly before the commutation time at 0.8 ms (deactivation PWM and control) and the current starts to increase linearly. As soon as the current has changed to a positive value and the voltage at the output node of the half-bridges has dropped to about 0 V, the commutation is completed and the control and the PWM are activated again. The measured Waveform shows good
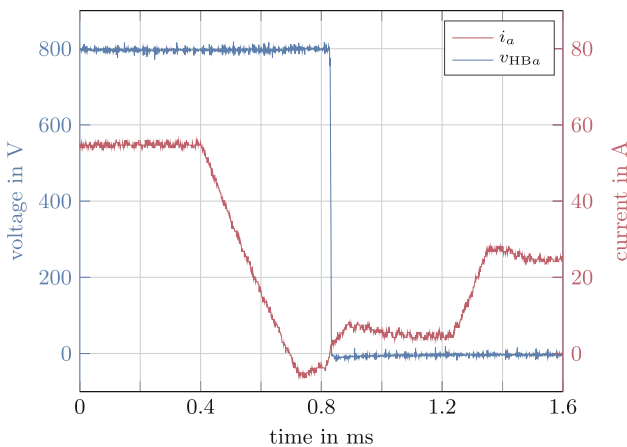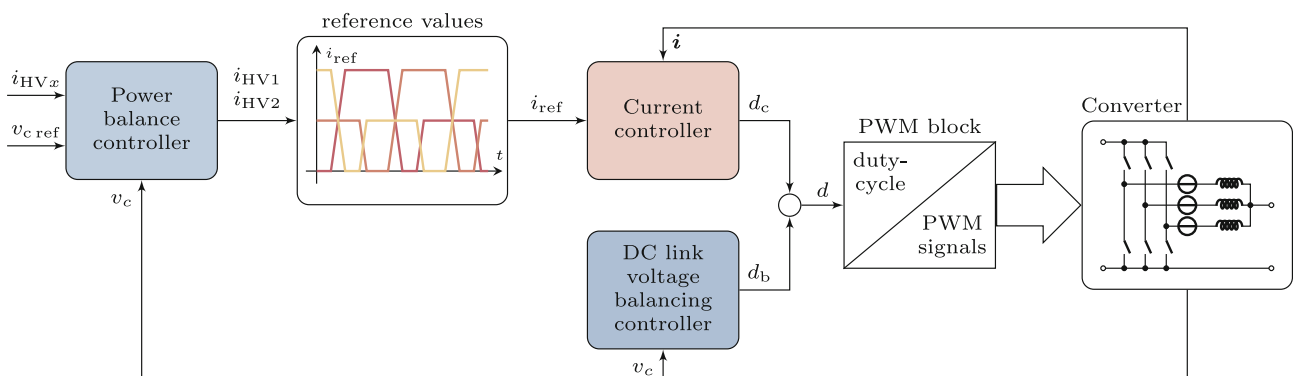
agreement with the expected behaviour depicted in Fig. 5. Only small deviations of the ideal waveform occur due to an overshoot of the leg current.

4 Control of the Module DC-Link Voltages

The requirements in terms of current control have already been discussed in [11] where simulation results have been presented only. For a practical realization of the concept, further aspects have to be considered:

- The proposed calculation of the input currents i_{HV1} and i_{HV2} is based on the desired power flow and the measured input voltages v_{HV1} and v_{HV2}. However, the losses of the inverter yield a slow discharge of the DC link capacitors. This obviously needs to be avoided in a practical realization of the converter. Hence, it must be taken into account in the current calculation (see Sect. 4.1).
- An unbalanced distribution of the DC link voltages of each leg occurs, e.g. due losses in the semiconductors or differences in the individual DC link capacitors. Consequently, the current control strategy in [11] is extended by a balancing algorithm which is discussed in Sect. 4.2.

The overall control concept is depicted in Fig. 9.

4.1 Control of the Average DC Link Voltage

The output current $i_{\mathrm{HV}x}$ is defined at the converter terminals where power is fed into the grid. Furthermore, it's sign is determined by the power flow through the inverter. The current at the other terminal is labelled by $i_{\mathrm{HV}y}$ and is specified such that that the power fed into the converter equals its output power plus the system losses. Otherwise these losses would be covered by the energy stored in the DC link capacitors, which would result in their discharge. To prevent this, three auxiliary controllers (*Power balance controllers*) are introduced with the task of controlling the power

Fig. 8 Measured commutation process of the demonstrator in leg a from $v_{\mathrm{HB}a} = 800\,\mathrm{V}$ to $0\,\mathrm{V}$ with current levels of the trapezoidal waveform $i_{a\,A} \approx 55\,\mathrm{A}$ and $i_{a\,B} \approx 25\,\mathrm{A}$

Fig. 9 Basic block diagram of the control system

balance of an individual leg. The power dynamics of leg $j \in \{a, b, c\}$ is assumed to be captured by

$$v_{\mathrm{HV}y} \cdot i_{\mathrm{HV}y} = v_{\mathrm{HV}x} \cdot i_{\mathrm{HV}x} + N \frac{dw_j}{dt}, \tag{12}$$

where N is the amount of series connected modules in the considered leg. Each module features a DC link capacitor with capacitance C as main energy storage element where

$$w_j = \frac{1}{N} \sum_{k=1}^{N} \frac{C v_{\mathrm{c}jk}^2}{2} \tag{13}$$

represents the average energy stored in the capacitors. Regarding $i_{\mathrm{HV}y}$ as the control signal and exploiting the known quantities $v_{\mathrm{HV}x}$, $v_{\mathrm{HV}y}$ and $i_{\mathrm{HV}x}$ motivates the choice

$$i_{\mathrm{HV}y} = \frac{v_{\mathrm{HV}x}}{v_{\mathrm{HV}y}} i_{\mathrm{HV}x} + \frac{N}{v_{\mathrm{HV}y}} p_j \tag{14}$$

for rendering dynamics (12) as

$$\frac{dw_j}{dt} = p_j. \tag{15}$$

For achieving power balance of an individual leg, the average energy w_j is controlled such that the error

$$e_j = w_{j\,\mathrm{ref}} - w_j \tag{16}$$

converges to zero exponentially, where $w_{j\,\mathrm{ref}}$ represents a constant energy demand of the DC link capacitors. In this paper this is implemented using a PI-type controller

$$p_j = k_{\mathrm{p}} \cdot e_j + k_{\mathrm{i}} \int_0^{\mathrm{t}} e_j(\tau)\, d\tau, \tag{17}$$

with the positive constants k_{p} and k_{i}. Note that for practical reasons it is convenient to express $w_{j\,\mathrm{ref}}$ in terms of the desired DC link voltage $v_{\mathrm{c\,ref}}$, i.e.,

$$w_{j\,\mathrm{ref}} = \frac{C v_{\mathrm{c\,ref}}^2}{2}. \tag{18}$$

The computation of $i_{\mathrm{HV}y}$ given in (14) is used to generate the reference current waveforms $\boldsymbol{i}_{\mathrm{ref}} = \begin{bmatrix} i_{a\,\mathrm{ref}} & i_{b\,\mathrm{ref}} & i_{c\,\mathrm{ref}} \end{bmatrix}^{\mathrm{T}}$ described in Fig. 3.

To determine the current levels i_{jA} and i_{jB} for the computation of $\boldsymbol{i}_{\mathrm{ref}}$ the converter power flow direction was defined to be positive from left to right, according to Fig. 1. Therefore, if $i_{\mathrm{HV}x}$ is positive, it becomes the reference value of the current on the lower voltage side i_{HV2} and if it is negative, it is the reference value of the current on the upper voltage side i_{HV1}. The relationships between i_{jA} and i_{jB} for calculating the reference currents are

$$i_{jA} = i_{\mathrm{HV1}} \tag{19}$$

$$i_{jB} = i_{\mathrm{HV2}} - i_{\mathrm{HV1}} \tag{20}$$

From these correlations, the power flow direction dependent computation of i_{jA} and i_{jB} can be performed for each leg:

$$\begin{aligned} i_{jA} &= \begin{cases} i_{\mathrm{HV}y} & \forall\ i_{\mathrm{HV}x} \geq 0 \\ i_{\mathrm{HV}x} & \forall\ i_{\mathrm{HV}x} < 0 \end{cases} \\ i_{jB} &= \begin{cases} i_{\mathrm{HV}x} - i_{\mathrm{HV}y} & \forall\ i_{\mathrm{HV}x} \geq 0 \\ i_{\mathrm{HV}y} - i_{\mathrm{HV}x} & \forall\ i_{\mathrm{HV}x} < 0 \end{cases} \end{aligned} \tag{21}$$

In the control block diagram in Fig. 9 this case selection and calculation is carried out by the *reference values* block.

4.2 Balancing of Module DC Link Voltage

To prevent an unbalanced distribution of the DC link voltages within the individual legs an additional controller (*DC link voltage balancing controller*) is introduced. By changing the average output voltage of the full-bridge modules of a single leg by variation of the PWM duty cycle, the energy supplied to and released from the modules can be adjusted. The objectives for the design of this controller are:

- The output continues to track the current reference waveforms, which are obtained through the current control.
- The N DC link voltages $v_{\mathrm{c}jk}$ with $k = 1, \ldots, N$ of leg j converge to the average $\overline{v}_{\mathrm{c}j}$ of the leg DC link voltages, i.e., a balance between the voltages is maintained.

Therefore, the error

$$\boldsymbol{e}_j = \begin{bmatrix} \overline{v}_{\mathrm{c}j} \\ \overline{v}_{\mathrm{c}j} \\ \vdots \\ \overline{v}_{\mathrm{c}j} \end{bmatrix} - \begin{bmatrix} v_{\mathrm{c}j1} \\ v_{\mathrm{c}j2} \\ \vdots \\ v_{\mathrm{c}jN} \end{bmatrix} \tag{22}$$

is defined. It turned out by simulation studies and experimental results that a proportional controller can manage the balancing task. Hence, taking into account the sign of the current in the respective leg j, the current controller output duty cycle $d_{\mathrm{c}j}$ of this leg is enhanced by the balancing control action which yields the duty cycle vector

$$\boldsymbol{d}_j = d_{\mathrm{c}j}\, \boldsymbol{n} + k_{\mathrm{b}} \operatorname{sgn}(i_j)\, \boldsymbol{e}_j. \tag{23}$$

Therein, the positive parameter k_{b} represents the balancing controller tuning parameter and $\boldsymbol{n} = \begin{bmatrix} 1 & 1 & \ldots & 1 \end{bmatrix}^{\mathrm{T}}$ with dimension $N \times 1$. The overall output duty cycle vector

$$\boldsymbol{d} = \begin{bmatrix} \boldsymbol{d}_{\mathrm{a}} & \boldsymbol{d}_{\mathrm{b}} & \boldsymbol{d}_{\mathrm{c}} \end{bmatrix}^{\mathrm{T}} \tag{24}$$
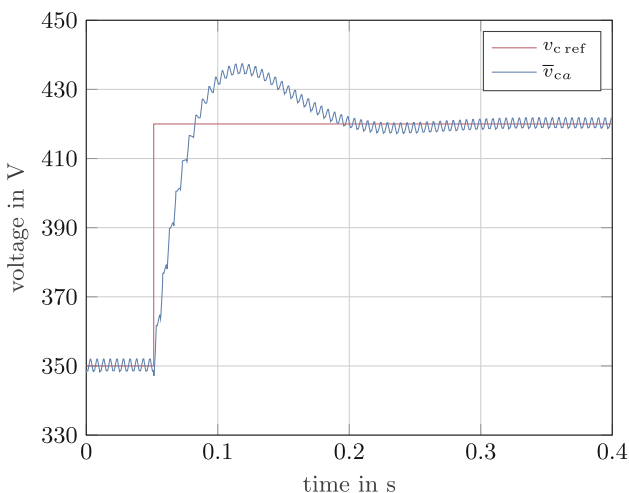
now contains a separate duty cycle signal for each module. It is noteworthy that this algorithm allows a straightforward implementation of the balancing controller in an FPGA based hardware.
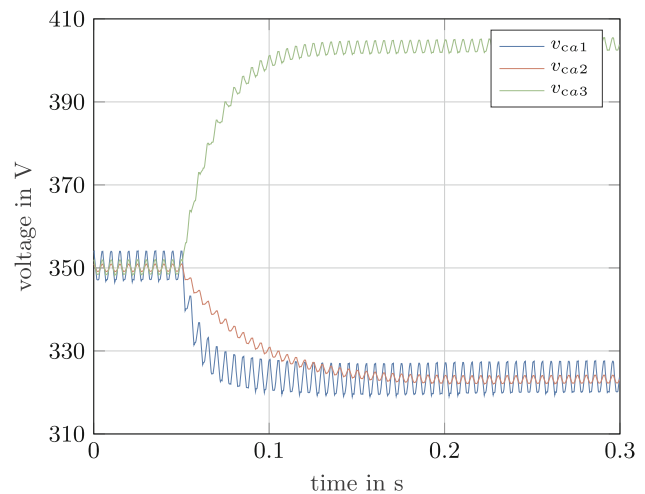
4.3 Simulation Results

For the development of the demonstrator, the Matlab/Simulink Model of the converter presented in [11] was extended by the concepts described in Sect. 4.1 and Sect. 4.2. The basic block diagram of the control system has already been depicted in Fig. 9.

A demonstration of the control algorithm for the average values of the DC link voltages via the simulation model is shown in Fig. 10 where the step response of the average value of the DC link voltages of leg a, $\overline{v}_{ca}$ to a change from 100% to 120% of the nominal DC link voltage of $V_c = 350\,$V is depicted. The resulting waveform of $\overline{v}_{ca}$ shows a slight overshoot which is tolerable since during normal operation of the converter the reference DC link voltage $v_{c\,ref}$ remains constant.

The operation of the controller for balancing the DC link voltages of a leg in the simulation model is presented in Fig. 11. For this simulation, the module capacitance of module 1 was changed to 50% of the nominal value of $C = 2800\,\mu$F and the capacitance of module 2 was changed to 200% of the nominal value, which explains the unequal height of the current ripples. In addition, by multiplying the measured DC link voltage of module 3 artificially with 0.8, a step was applied to the controller from 50 ms onwards to investigate the control behavior. The resulting waveforms show, that the controller is able to maintain the balance of the modules of one branch despite their deviation in capacitance and an artificial change in their reference voltage. Please note that the average module voltage $\overline{v}_{ca}$ of the leg does not change during this test. Only the balancing controller is affected in this case.
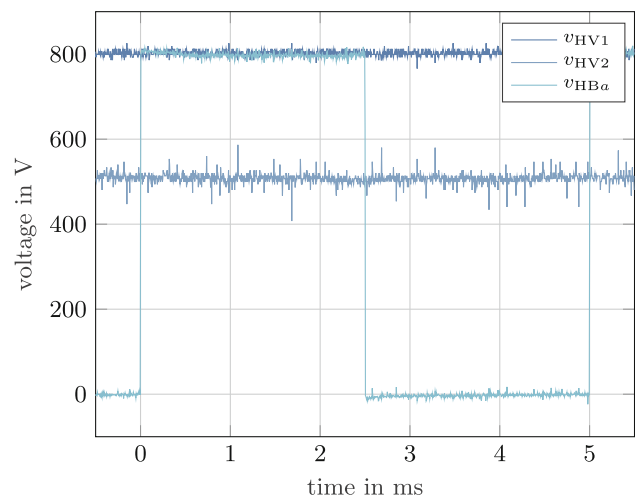
Fig. 11 Step response of the balancing controller

4.4 Experimental Results

The proposed controller structure, i.e. power balance controller, the DC link voltage balancing controller and auxiliary functions such as the PWM block and the generation of the current reference values have been implemented in an FPGA-based control system. This system was then used to control the demonstrator described in Sect. 2. To verify the basic function of all measurement and control systems of the prototype, the transfer of the rated current of $I_r = 83\,$A of the converter was carried out in an experiment.

A voltage of $v_{HV1} = 800\,$V was applied on the upper voltage side, and a reference DC link voltage of $v_{c\,ref} = 350\,$V was specified in power balance controller. The lower voltage side was loaded with a power resistor of $R = 6\,\Omega$, resulting in a voltage drop of $v_{HV2} \approx 500\,$V. Figs. 12 and 13 depict the measured voltage and current waveforms taken from the lab-scale laboratory

Fig. 10 Simulation of the response of the controller for the average values of the DC link voltages to a step of its reference value $v_{c\,ref}$ from 350 V to 420 V

Fig. 12 Measured in- and output voltage v_{HV1} and v_{HV2} together with the output voltage of the half-bridge in leg a, v_{HBa} during the rated power transfer test of the converter
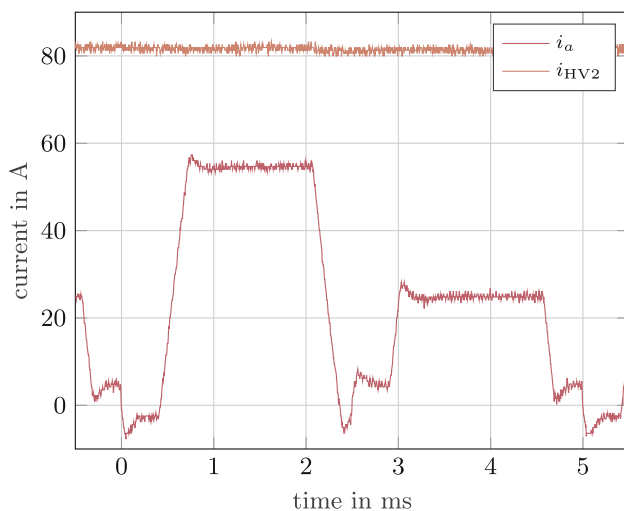
Fig. 13 Measured current on the lower voltage side i_{HV2} together with the current in leg a, i_a during the rated power transfer test of the converter

prototype. They show one period $T = 5\,\text{ms}$ of the converter switching scheme during steady steady operation at constant output currents and output voltages. The measured waveforms are in good agreement with the analytically derived values from Sect. 2. Very small overshoot occurs during the trapezoidal current transitions of the waveform i_a and the measured output quantities v_{HV1}, v_{HV2} and i_{HV2} show only a small deviation from their average value.

5 Conclusion and Outlook

This publication expands the information presented in [11] about the HVDC-DC converter developed within the research project "griDConv" at the Graz University of Technology. Besides an overview of the operation principles of the inverter, simplified dimensioning rules for the passive components are presented. In addition, a novel soft-switching commutation strategy for the half-bridge circuits is introduced, which allows scalability of the topology with the voltage on the upper voltage side. Furthermore, the current control concept described in [11] is extended for a practical implementation of the inverter by two auxiliary controllers which provide the ability to control the DC link voltages of the full-bridge modules.

Future planned research activities include a novel structure of the balancing controller for the DC link voltages, investigations on the effects of the inverter operation on connected DC grids as well as hardware improvements concerning the communication between the modules.

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