



## Extending the application range of MMCs in high-performance drives: limiting issues and new proposals

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**Abstract** Modular Multilevel Converters (MMCs) are becoming more and more popular in medium-voltage applications thanks to several interesting features. The major limitation for applications with variable speed drives (VSDs) is the submodule capacitors' voltage ripple, which depends directly on the output current/torque and inversely on the output frequency/speed. Among all the hybrid MMC topologies addressed in recent literature, the Flying-Capacitor Passive Cross-Connected arms (FC-PCC) MMC seems one of the most promising to cope with this issue. This article provides a comprehensive overview of its features and capabilities. The main open issues limiting safe and reliable converter operation in VSD applications are addressed, and novel solutions are presented, such as the optimization of the converter digital control strategy, the distributed implementation of the architecture, the L-C oscillations damping during the pre-charge/start-up of the converter, and the optimized arm inductor design based on magnetic coupling concepts. The effectiveness of all the proposals is demonstrated through an accurate simulation of a 22 kW Permanent Magnet Synchronous Machine (PMSM) drive, including a complete model of the effects of the real-time communication and the processing latency. A prototype of the system has been developed employing some known and novel ar-

chitectural solutions, as discussed in the last section of the paper.

**Keywords** Modular Multilevel Converters, MMC · Multilevel converters · Flying-Capacitor · Permanent Magnet Machine drives · Digital control · Voltage balancing · Submodule · Coupled inductors

### Erweiterung des Anwendungsbereichs von MMCs in Hochleistungsantrieben: bekannte Probleme und neue Vorschläge

**Zusammenfassung** Modulare Multilevel-Konverter (MMCs) werden aufgrund von mehreren Eigenschaften in Mittelspannungsanwendungen immer beliebter. Jedoch ist die Höhe der Spannungswelligkeit der Submodulkondensatoren für Anwendungen mit drehzahlvariablen Antrieben (VSDs) eine der größten Einschränkungen. Sie ist direkt vom Ausgangsstrom/-drehmoment und umgekehrt von der Ausgangsfrequenz/-drehzahl abhängig. Bei allen in der jüngsten Literatur behandelten hybriden MMC-Topologien ist der „Flying-Capacitor Passive Cross-Connected Arms(FC-PCC)“-MMC eine der vielversprechendsten Topologien, um dieses Problem zu bewältigen. In diesem Beitrag wird ein umfassender Überblick über seine Eigenschaften und Möglichkeiten gezeigt. Bekannte Probleme, die den sicheren und zuverlässigen Betrieb von Umrichtern in VSD-Anwendungen einschränken, werden angesprochen, und neue Lösungen vorgestellt: wie die Optimierung der Architektur und der Strategien der verteilten digitalen Steuerung des Umrichters, die Dämpfung von L-C-Schwingungen während des Vorladens/Anfahrens des Umrichters und das optimierte Design der Arm-Induktivität basierend auf magnetisch gekoppelten Konzepten. Die Wirksamkeit der behandelten Ansätze wird durch genaue Simulation eines 22-kW-Permanentmagnet-

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Synchron-Antriebs (PMSM) einschließlich eines vollständigen Modells der Auswirkungen der Echtzeit-Kommunikation und der Verarbeitungslatenz nachgewiesen. Ein Prototypentwurf des Systems wurde unter Verwendung einer bekannten und neuartigen Architektur entwickelt, welche im letzten Abschnitt des Beitrags erläutert wird.

**Schlüsselwörter** Modulare Multilevel-Konverter, MMC · Multilevel-Konverter · Fliegender Kondensator · Permanentmagnet-Maschinenantriebe · Digitale Steuerung · Spannungsabgleich · Submodul · Gekoppelte Induktivitäten

## 1 Introduction

Modular Multilevel Converters offer many advantages in medium voltage drives and emerging power conversion applications. First of all, modularity is an important aspect, as the MMC is realized as a cascade serial connection of identical cells, submodules (SM), thus intrinsically scalable to an arbitrary number of levels while guaranteeing a small footprint. Second, low-voltage semiconductor devices can be used in the SMs, which allows to reduce the losses and achieve higher efficiency. Moreover, the multilevel output guarantees lower electromagnetic interference (EMI) and high-frequency harmonics on the output waveforms, leading also to reduced stress on motor bearings. Similar advantages can be achieved by using cascaded converters, but in MMC the absence of bulky multiphase transformers allows to reduce the overall converter size and cost. Unfortunately, the adoption of MMCs in motor drives applications is affected by an intrinsic issue of this topology, i.e. the SM capacitor ripple increases with output current magnitude and decreases with output frequency, [4, 5, 12, 13]. Therefore, the torque production capability is strongly limited in the low-speed range of the machine, to avoid over/under voltage at each SM, compromising the drive performance.

Various control techniques have been developed to mitigate this critical issue, [9, 12]. The most common solution is to inject a common-mode voltage on the machine to perform a balancing action on the SM capacitors' stored energy. However, those techniques bring some disadvantages mainly related to the machine reliability: the additional voltage contribution increases the failure rate of the winding insulation and exposes the machine to the risk of premature bearing issues related to fluting, scoring, cracks and fractures. Recent topologies, such as Flying-Capacitor Passive Cross-Connected arms MMC (FC-PCC MMC) [1, 8], Active Cross-Connected MMC [6], Modified Hybrid MMC [11], allow to manage the SM ripple voltage with various approaches. A combination of high-frequency voltage and current injection is proposed in [1, 8], allowing to manage the SMs voltage and enabling

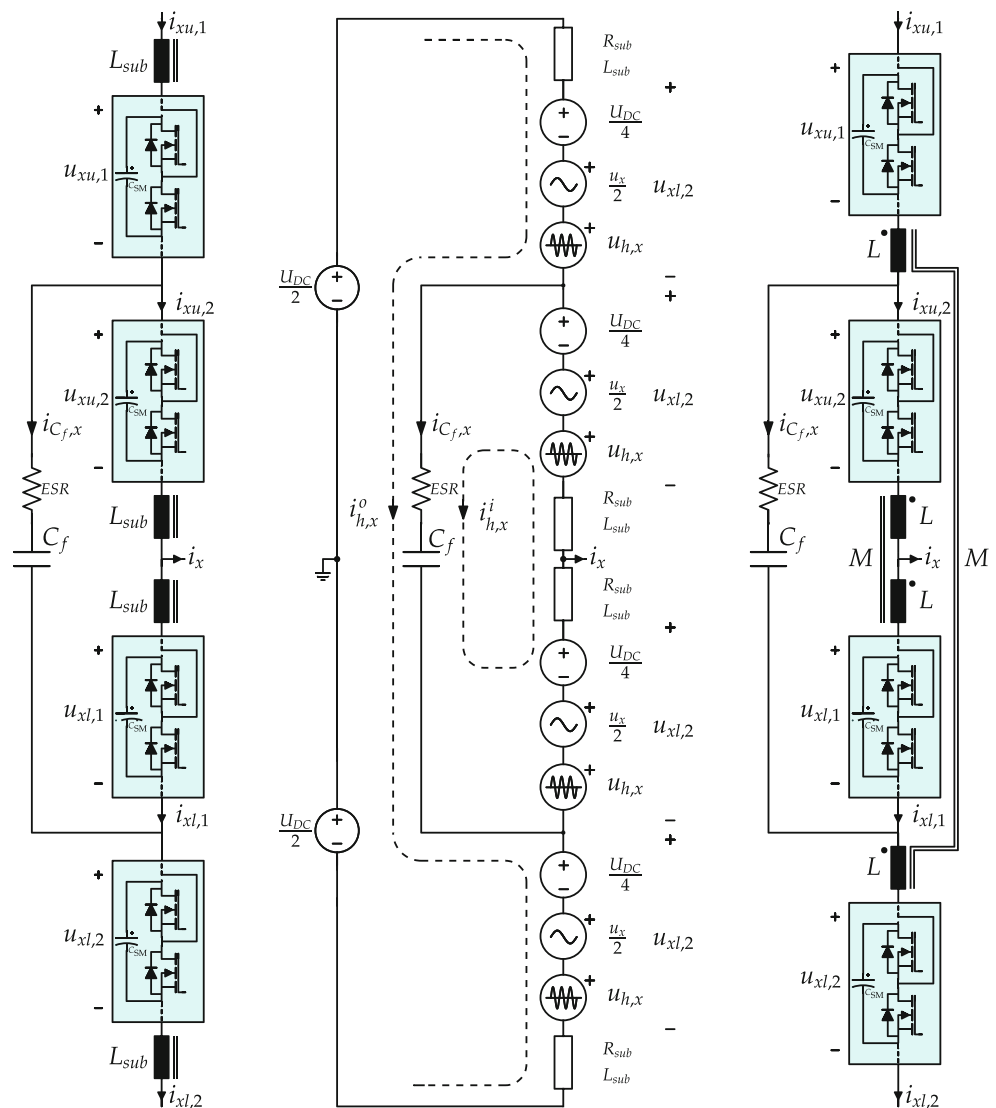
proper motor drive operation even at zero frequency and rated torque.

An outline of the optimized control strategy and the associated advanced communication architecture proposed for FC-MMC based drive system is reported in this paper. The problem of the pre-charge/start-up of the converter will be explained, and an advanced novel control strategy proposed and discussed. Some hints regarding the whole converter design will be given in conjunction with a new sub-arm coupled inductor design concept, allowing a reduction of the inductor volume and cost, and increased compactness of the overall converter. The effectiveness of these control and architectural proposals will be demonstrated with an accurate simulation of a 22 kW FC-MMC based drive for Permanent Magnet Synchronous Machines (PMSM), taking all the system implementation constraints into consideration, also including the communication strategy, and protocol associated latency.

## 2 FC-PCC MMC topology

The basic structure of each FC-MMC phase-leg (denoted with a letter  $x = a, b, c$ ) is shown in the schematic on the left-hand side in Fig. 1. It is split into two arms (subscript  $y$ , the upper arm  $y = u$ , and the lower arm,  $y = l$ ) with respect to the leg mid-point, i.e., the output terminal, whose output current is  $i_x$ . Each arm is split into two sub-arms, named upper, marked with the subscript 1, and lower, marked with the subscript 2, respectively. A generic implementation consists of a series connection of  $N$  half bridge (HB) submodules per arm, each one equipped with a capacitor  $C_{SM}$  with a nominal voltage  $U_C = U_{DC}/N$ , where  $U_{DC}$  is the total dc-bus voltage. A SM has two active states, i.e., inserted (SM output voltage  $U_{SM} = U_C$ ) or bypassed ( $U_{SM} = 0$ ). The SM can also be in the blocked state, in which both active switches are off, but current may flow through the antiparallel diodes. In order to save additional hardware, the power supply for SM control and gate driving is taken from the SM capacitor  $C_{SM}$ , indeed, a separate power supply from an external source would require high-voltage isolation and would not be feasible, in most cases. The total leg inductance (twice the arm inductance  $L_{arm}$ ) is split into four parts, each one in series with each sub-arm and named  $L_{sub}$ . The equivalent resistance of each sub-arm, given by the inductance winding resistance and the power devices on-state resistances is also considered, i.e.,  $R_{sub}$ . The flying-capacitor  $C_f$  is connected across the two midpoints of the upper and lower arms. This provides an additional path for the ac current, which is exploited by the control for SM balancing. The flying-capacitor itself is part of two circuit loops: the inner one, comprising the middle sub-arms, and the outer one, with the top sub-arm of the upper arm and the bottom sub-arm of the lower arm.

**Fig. 1** Flying-Capacitor Passive Cross-Connected Modular Multilevel Converter phase-leg (left), equivalent model (middle), and proposed coupled inductors scheme (right)



### 3 FC-PCC MMC model

#### 3.1 FC-PCC MMC mathematical model

Taking as reference the steady-state averaged model of an FC-MMC phase-leg reported in the middle schematic of Fig. 1, it is possible to express the sub-arm inserted voltage as follows:

$$u_{xu,1} = \frac{U_{DC}}{4} - \frac{u_x}{2} - u_{h,x}, \quad u_{xu,2} = \frac{U_{DC}}{4} - \frac{u_x}{2} + u_{h,x} \quad (1)$$

$$u_{xl,1} = \frac{U_{DC}}{4} + \frac{u_x}{2} - u_{h,x}, \quad u_{xl,2} = \frac{U_{DC}}{4} + \frac{u_x}{2} + u_{h,x} \quad (2)$$

where  $u_{h,x}(t) = \hat{U}_{h,x}(t) \sin(\omega_h t)$  is the additional high-frequency voltage term injected by each sub-arm. (1) and (2) show the conventional MMC's behaviour of the output voltage  $u_x$  at the fundamental frequency  $\omega$  and dc voltage  $U_{DC}$ . All the voltage components are averaged along one switching period.

The high-frequency voltage  $u_{h,x}(t)$ , is introduced with opposite signs by the sub-arms, so that the re-

lated components cancel out in the total arm voltage and hence will not produce any effect on the output voltage, nor on the dc-bus voltage. Whereas, their effect is visible on the additional path created with the flying-capacitor  $C_f$ . The overall flying-capacitor current will be the sum of the outer and inner loop currents  $i_{C_f,x} = i_{h,x}^i + i_{h,x}^o = 2i_{h,x}$ , where  $i_{h,x}^i = i_{h,x}^o = i_{h,x}$  is valid in case of balanced sub-arms impedances and equal high-frequency voltage perturbations  $u_{h,x}(t)$ .

With the same procedure, it is possible to express the sub-arm currents where the dc current  $i_{d,x}$  and the fundamental frequency  $i_x$  components of the conventional MMC model are preserved with the single addition of the high-frequency current terms  $i_{h,x}$ :

$$i_{xu,1} = i_{d,x} + \frac{i_x}{2} + i_{h,x}, \quad i_{xu,2} = i_{d,x} + \frac{i_x}{2} - i_{h,x} \quad (3)$$

$$i_{xl,1} = i_{d,x} - \frac{i_x}{2} - i_{h,x}, \quad i_{xl,2} = i_{d,x} - \frac{i_x}{2} + i_{h,x} \quad (4)$$

The interaction of the high-frequency voltages injected by the sub-arms with the high-frequency in-

jected currents that flow through the flying-capacitor establish a power flow between the upper and lower arms. In particular, the power is exchanged between the top sub-arm of the upper arm and the bottom sub-arm of the lower arm, which are part of the outer loop. The same happens between the bottom sub-arm of the upper arm and the top sub-arm of the lower arm, which are part of the inner loop. The combination of these interactions introduces the possibility to control the power exchange from the upper and lower arm and vice versa, hence compensating for any energy imbalance between dc-buses of different SMs. In order to maximize the power transfer, the high-frequency currents are controlled to be sinusoidal and in phase with respect to the high-frequency impressed voltage  $u_{h,x}(t)$ , i.e.,  $i_{h,x}(t) = \hat{A}_{h,x}(t) \sin(\omega_h t)$ .

### 3.2 FC-PCC MMC current dynamics

Furthermore, it is possible to model the converter current dynamics in order to design a proper converter control strategy. Starting from the averaged model shown in the central schematic of Fig. 1, it is possible to apply Kirchhoff's voltage law to both the outer and inner loops, leading to:

$$U_{DC} - L_{\text{sub}} \frac{di_{xu,1}}{dt} - R_{\text{sub}} i_{xu,1} - u_{xu,1} - u_{Cf} - L_{\text{sub}} \frac{di_{xl,2}}{dt} - R_{\text{sub}} i_{xl,2} - u_{xl,2} = 0 \quad (5)$$

$$u_{Cf} - u_{xu,2} - L_{\text{sub}} \frac{di_{xu,2}}{dt} - R_{\text{sub}} i_{xu,2} - R_{\text{sub}} i_{xl,1} - L_{\text{sub}} \frac{di_{xl,1}}{dt} - u_{xl,1} = 0 \quad (6)$$

Substituting the expressions for the sub-arms currents (3) and (4), and rearranging the terms to have the forcing quantities on the left side, the following relations are obtained:

$$\frac{U_{DC} - (u_{xu} + u_{xl})}{2} = L_{\text{arm}} \frac{di_{d,x}}{dt} + R_{\text{arm}} i_{d,x} \quad (7)$$

$$\frac{U_{DC} - 2u_{Cf} - (u_x^o - u_x^i)}{2} = 2L_{\text{sub}} \frac{di_{h,x}}{dt} + 2(R_{\text{sub}} + \text{ESR}) i_{h,x} \quad (8)$$

where the term  $i_{d,x}$  has been redefined to include, in a steady-state balanced operation, both the leg common-mode dc current of (3) and (4), and any possible low-frequency circulating current across two different legs  $i_{xz}$ , and  $u_x^o = u_{xu,1} + u_{xl,2}$  and  $u_x^i = u_{xu,2} + u_{xl,1}$  are the total voltages inserted by the outer loop and inner loop sub-arms respectively, and ESR is the equivalent series resistance of the flying-capacitor as represented in Fig. 1. Eqs. (7) and (8) prove that the dynamics of the low-frequency leg circulating current  $i_{d,x}$  is naturally fully-decoupled from the one of the high-frequency current  $i_{h,x}$ , since these two quantities are controlled by different combinations of the SM inserted voltages.

## 4 Compensation of the low-frequency energy fluctuations

Voltage ripple across SM capacitors is due to low-frequency energy fluctuations that arise in the converter leg, and it is related to the output current amplitude and frequency, [9]. Evaluation of the power processed by a generic converter arm  $p_{xy}$  is necessary to design a compensation strategy based on the interaction of high-frequency voltage and current components:

$$p_{xy} = \underbrace{\frac{U_{DC}}{2} i_{d,x} - \frac{u_x i_x}{2}}_{p_{x,\text{CM}}} \pm \underbrace{\frac{U_{DC} i_x}{4} - u_x i_{d,x} - \hat{U}_h \hat{A}_{h,x} + \hat{U}_h \hat{A}_{h,x} \sin(2\omega_h t)}_{p_{x,\text{DM}}} \quad (9)$$

where the + sign applies to the upper arm  $y = u$  and the - sign to the lower arm  $y = l$ . The arm power  $p_{xy}$  can be split into two components, identical for both the upper and lower arm of the same phase-leg: a common-mode  $p_{x,\text{CM}}$  and a differential-mode  $p_{x,\text{DM}}$ . The first component is responsible for the variations of the average value of the SM capacitor energy of the entire phase-leg. Whereas, the second one accounts for any imbalance of the average energy stored by the SM capacitors of one arm (upper or lower) compared to the other. As a result, the presence of these two components deviates the SM capacitor voltages from the rated value. Based on the expression of the common-mode power component  $p_{x,\text{CM}}$ , it can be easily seen that the degree-of-freedom to be exploited for the control of this power component is the low-frequency leg circulating current  $i_{d,x}$ . Conversely, the high-frequency current  $i_{h,x}$  can be used to regulate the differential-mode power component  $p_{x,\text{DM}}$ .

## 5 Distributed digital control strategy

A drive based on this type of converter requires a complex control strategy that acts at various levels of abstraction, in order to ensure proper, reliable, and safe converter operation. Fig. 2 shows the corresponding high-level functional block diagram of the overall drive control system highlighting the electric machine, the power converter and the logical blocks related to the control strategy tasks. The five control tasks, A, B, C, D and E, can be organized in the hierarchy reported in Fig. 3, which identifies the corresponding control domain and a brief description of the functions. Following an in-depth analysis of the various operation of the control layers, it has been possible to propose a distributed implementation of the proposed hierarchical control structure. To achieve this, the system is designed with one Central Unit (CU) and a number of decentralized microcontroller units, each one located within each SM (SM MCU). All the units share a common M-LVDS communication bus. Proper galvanic isolation is guaranteed at each SM by novel

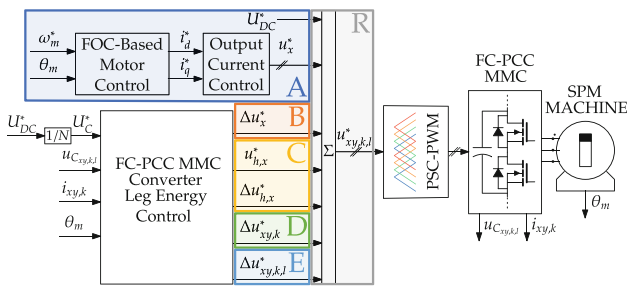


Fig. 2 Control system high-level functional block diagram of the FC-PCC MMC based drive system

bidirectional optical transceivers, [1]. The overall voltage reference of each SM is calculated by the block  $R$  as an algebraic sum of each control task output, being either calculated by the CU or by each SM MCU, and then actuated through a phase-shifted-carrier pulse-width-modulator (PSC-PWM) at SM level. The corresponding data paths of the various control voltage components, as well as the related equations giving the correct voltage reference depending on the position of the SM within the converter leg, are shown in Fig. 4. The adoption of a distributed control system for a modular topology such as the MMC offers various advantages:

- faster processing and minimum data exchange between computational units (i.e., minimum latency), as compared to either fully centralized, characterized by a considerable operation queue and a lot of communication overhead, or a fully decentralized approach, limited by low computing performance derived from cost constraints;
- full scalability, allowing to build an MMC with an arbitrary number of SMs in the phase-leg (theoretically possible, provided that the required throughput of the communication bus is actually achievable).

However, the distributed implementation of the control strategy is challenging because SMs and central unit have to exchange various data packets, namely measurements, partially processed data or voltage references to be synthesized, with accurate timing constraints. Therefore, a reliable high-speed communication link and tight synchronization among all the microcontrollers are required. Moreover, being the SMs series-connected, their control units are referred to voltage potentials that depend on their position in the converter leg. In general, a galvanically isolated link should be realized for exchanging information between the different control units. This would introduce additional complexity to the communication infrastructure, in order to guarantee the required bus performance. A comprehensive explanation of all the different goals and data sources of all the control actions can be found in [1].

CONVERTER LAYER	FOC MOTOR CONTROL	A
LEG LAYER	LEG COMMON-MODE ENERGY CONTROL	B
ARM LAYER	ARM DIFFERENTIAL-MODE ENERGY CONTROL	C
SUB-ARM LAYER	SUB-ARM EQUALISATION CONTROL	D
SM LAYER	SINGLE SM EQUALISATION CONTROL	E

Fig. 3 High-level control layers hierarchy for FC-PCC MMC

### 5.1 Optimized communication architecture

Even though the distributed control approach brings numerous advantages in terms of control strategy flexibility, overall computational effort minimization, and improved converter scalability, it is not flawless:

- the need for a control unit in each submodule increases both the cost and the design complexity of the SM with respect to a fully centralized approach;
- the computational units require a reliable and fast communication channel for exchanging all the necessary information.

Even if the first one seems to be the most limiting aspect, it turns out that the inclusion of a supplementary processing unit on each SM is a resource to leverage, rather than a limitation. In fact, besides the execution of local control actions, they can be exploited for protection, monitoring and diagnostics tasks, too. In contrast, communication between the SM and the CU is the real challenge in an MMC converter. This section describes the communication architecture proposed in order to meet real-time operation and synchronization requirements.

In case of high-frequency PSC-PWM MMCs, the requirement in terms of control bandwidth can be strict, and this directly impacts the required bus transmission rate. Therefore, in [3] an extensive optimization has been carried out in order to minimize the data transmission, organize the scheduling and synchro-

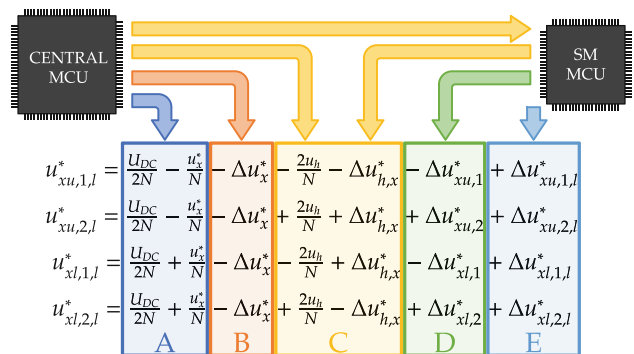
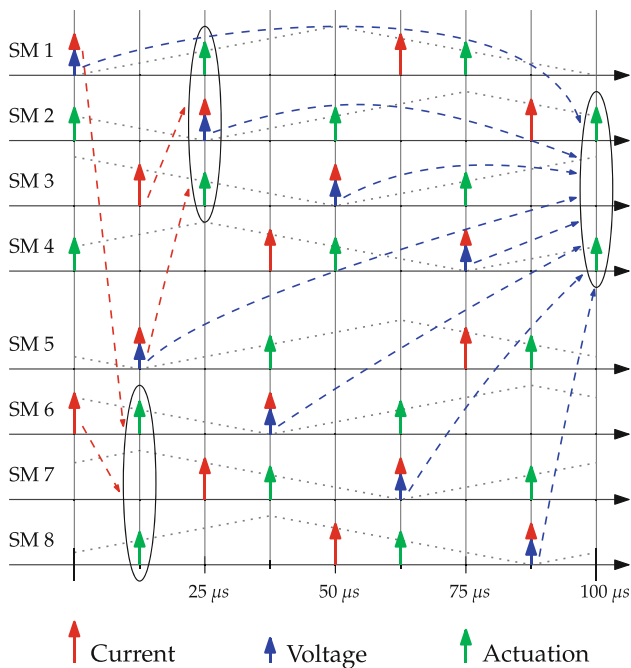


Fig. 4 Distributed control architecture: the sources of each reference voltage component fed to the  $l$ -th SM within the sub-arm PSC-PWM modulator are highlighted





**Fig. 5** SMs scheduling diagram: red and blue arrows indicate the time instants in which the SMs transmit their own current and voltage measurements respectively, green arrows point out the control actuation instants; the dotted grey lines represent each SM carrier

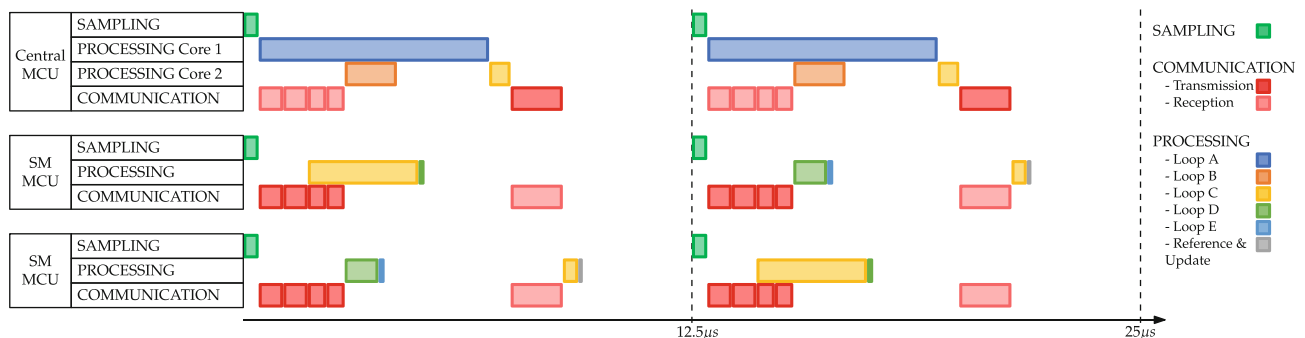
nize the communication according to technological constraints and real-time requirements. In particular, the time-shift  $t_{sh} = 12.5\mu s$  between two modules of different sub-arms identifies a so-called slot. At the beginning of each slot, every sub-arm current is transmitted to all the entities attached to the bus in order to maximize the control bandwidth; in contrast, the voltage control bandwidth may be narrower (i.e. requires lower sampling rate), therefore, all the leg voltage measurements are spread into the entire PWM carrier period, allowing to reduce the transmission requirements. Additionally, to limit the protocol-related overhead, measurement forwarding on the bus can be scheduled such that each voltage packet is aggregated with the current sensed by the same SM. Fig. 5 summarizes the dataflow for the upper arm of a generic phase, which is identical to the lower

arm. PWM carriers are shown for reference (dotted grey lines) in order to highlight the synchronization aspects. Voltage and current packets are indicated by the blue and red arrows, respectively, and data aggregation is represented by the arrows together. Eventually, the PWM update instants are marked with solid green arrows. The colored dashed arrows represent the links between a sampling instant (red for current, blue for voltage) and the consequent actuation event, i.e. the voltage reference calculation which exploits those measurement samples.

The proposed optimization leads to the reduction of the communication protocol to a fundamental sequence of  $25\mu s$ , as reported in Fig. 6. The sequence can be analysed considering the CU and any two SMs exhibiting a  $t_{sh} = 12.5\mu s$  time-shift, i.e., two submodules belonging to a different sub-arm. Essentially, computing units need to perform three different actions: sampling of measurements, processing of control actions and exchanging information through the communication bus. The length of each bar approximately represents the estimated duration of each operation. A worst-case evaluation of the required processing time has been carried out, assuming an appropriate margin, by analysing and profiling the code which implements the adopted algorithm on the MCU. The sampling stage is straightforward and involves the SM voltage and current, or the machine speed and the converter bus voltage, at CU level. Control tasks scheduling is represented with the same colour convention as in Figs. 2, 3 and 4 and has been optimized with the aim of prioritizing the tasks that require communication. Eventually, the communication section is shown in Fig. 6. Red boxes represent transmission and pink boxes stand for reception. The communication pattern changes along the time slots according to the scheduling reported in Fig. 5.

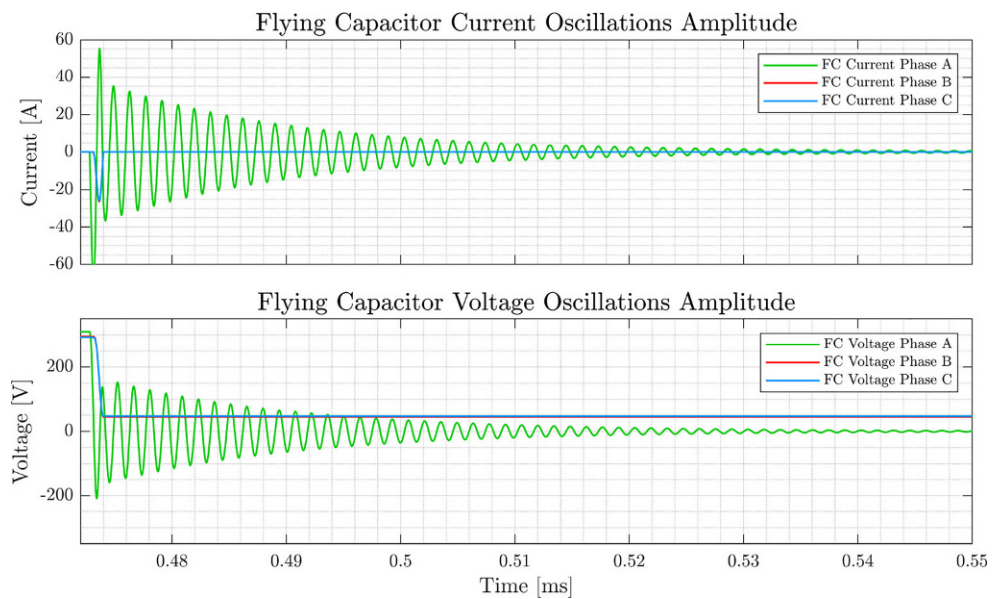
### 6 Pre-charge/Start-up strategy with L-C oscillations damping

Prior to the steady-state converter operation, proper pre-charge/start-up of the SMs capacitors up to the nominal voltage values is required. However, the topology modification obtained through the addi-



**Fig. 6** Fundamental sequence timing diagram among central unit and submodules

**Fig. 7** Uncontrolled L-C oscillations during converter pre-charge/start-up phase



tion of the flying-capacitor increases the complexity of this process. During this phase, undamped oscillations between the flying-capacitor and the sub-arm inductor can be triggered, leading to potentially harmful current levels as reported in Fig. 7. A suitable pre-charge control must be designed in order to limit these unavoidable resonance events, [7]. Another requirement is that, by the end of the pre-charge phase, all SMs need to reach the nominal voltage value ( $U_{SM} = U_{DC}/N$ ), regardless of the actual capacitance value (i.e., considering actual tolerances of the capacitance values) and the voltage across the flying-capacitors needs to be half of the dc-bus voltage  $U_{cf} = U_{DC}/2$ . Moreover, since the load is an electrical machine, the output current during the pre-charge/start-up period should be as small as possible, in order to keep the uncontrolled torque negligible.

Most of the pre-charge techniques reported in the literature, [2, 14, 15, 17], are based on additional hardware dedicated for the pre-charge phase. Typically, an isolated power supply is employed to power the SM control logic, in order to be able to drive the power switches regardless of the SM capacitor voltage level during the pre-charge phase. However, avoiding dedicated hardware and lowering the complexity is the main goal of the proposed pre-charge strategy. Taking into account all the requirements, a multistage pre-charge strategy has been designed. The scheduling of the whole process is implemented as a state machine, which is executed within the central control unit of the converter and is in charge of supervising the correct operation of the three stages:

1. uncontrolled pre-charge: the power switches cannot be controlled because the SM capacitor voltage is too low and the control logic power supply cannot turn on. Thus, the current can flow only through the antiparallel diode of the upper switch of each

SM. A current limiting resistor  $R_{st} \geq U_{DC}/3I_{max}$  is inserted to limit the inrush currents. The voltage across the capacitor  $C_{SM}$  should reach at least the minimum value that allows the SM MCU power supplies to turn on. After this phase, the voltages across the flying-capacitors of each leg are almost at their setpoint values;

2. SM capacitor pre-charge: a single converter leg is charged at a time, in order to reduce the complexity and to improve the voltage equalization, while the others are driven with the SMs in blocking state. During the first part of this stage (2a), the dc busses of the SMs on the outer sub-arms are controlled to the voltage set point through the control task E, [1, 3], whereas the SMs of the inner sub-arms are bypassed. However, L-C oscillations can arise, as shown in Fig. 7. This typically occurs during the start-up of the first converter leg only, because the flying-capacitor is charged up to its nominal voltage value. On the other hand, during the start-up of the other phase-legs, their flying-capacitor has already been discharged during the transition between two converter legs, thus eliminating this issue. To overcome this problem, the SMs of the inner sub-arms are inserted to effectively dampen the L-C oscillations only during the pre-charge of the first converter leg. At the end of the damping phase, the flying-capacitor is discharged and the inner sub-arms SMs are bypassed, allowing the outer loop ones to fully charge to the setpoint. Once the capacitors in the SMs of the outer sub-arms have reached the setpoint voltage, they can be bypassed in order to charge the SMs of the inner sub-arms (2b). However, also in this case L-C oscillations can be a severe problem since they can cause the SM capacitor voltage to drop below the power supply turn-on causing the switches to become uncontrol-

**Table 1** FC-MMC based drive parameters

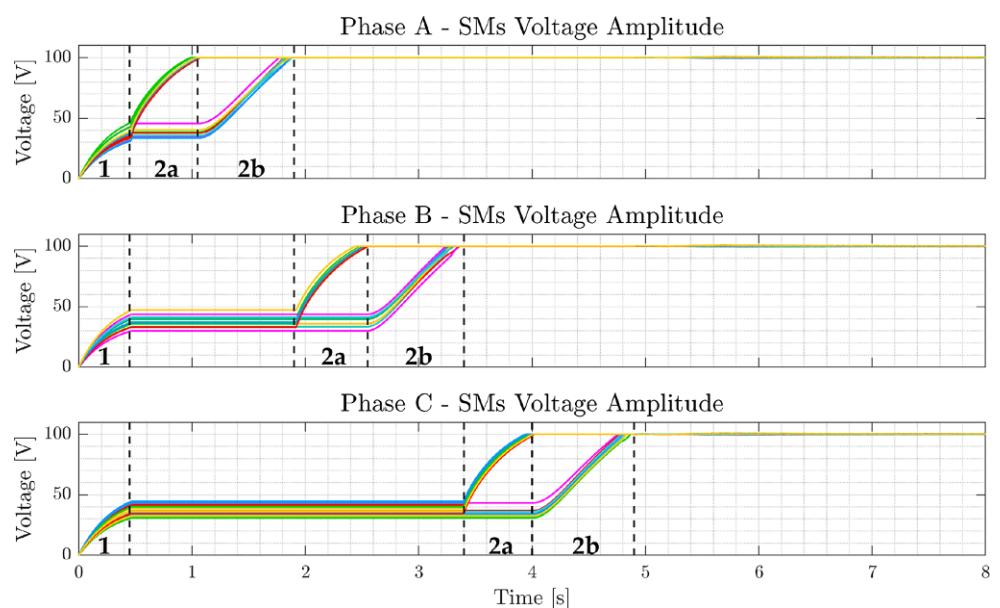
Rated dc-bus voltage	$U_{DC}$	800V
Number of SM per arm	$N$	8
SM capacitor rated voltage	$U_C$	100V
Rated peak phase voltage	$\hat{U}_x$	400V
Rated peak phase current	$\hat{I}_x$	75A
Total arm inductance	$L_{arm}$	1 mH
Total arm resistance	$R_{arm}$	10 m $\Omega$
Rated SM capacitance	$C_{SM}$	3900 $\mu$ F
Rated flying-capacitance	$C_f$	50 $\mu$ F
PWM carrier frequency	$f_i$	10 kHz
HF injection frequency	$f_h$	1 kHz

lable. This issue can be solved by properly tuning the control loop  $E$ .

- FC pre-charge: pre-charging of the flying-capacitor cannot be done at the same time as the SMs capacitors since, during the leg-to-leg transition, it would discharge on the SMs capacitors. For this reason, the flying-capacitors are charged only after the voltages of all the SMs capacitors reach their setpoint values. Aiming at avoiding oscillations in the equivalent L-C circuit during this stage, the control loops  $A$ ,  $B$ ,  $D$  and  $E$ , [1, 3], are activated. This happens because a common-mode voltage is synthesized by the SM to effectively charge the flying-capacitors and it can lead to undesired current (i.e., torque) production (counteracted with  $A$  control) and SM capacitor average voltage variation (counteracted with  $B$  control). To achieve this, the required common-mode voltage reference for outer loop SMs varies from  $U_{DC}/N$  to  $U_{DC}/2N$ , while the reference for inner loop SMs varies from 0 to  $U_{DC}/2N$ .

The proposed pre-charge and start-up strategy has been validated by means of numerical simulation,

**Fig. 8** SMs capacitor voltages during the pre-charge/start-up of the converter. The numbers 1, 2a and 2b mark the various stages of the algorithm



even in case of significant deviations from the nominal capacitance values. The main parameters of the converter are specified in Table 1. The voltages of the SM capacitors during the whole procedure are reported in Fig. 8. The numbers (1, 2, 3) shown in the diagram correspond to the stage numbering in the above. It can be noticed that, regardless of the capacitance values (which are visible by the different transients duration), the steady-state voltage at the end of the pre-charge is the same and, even more important, there are no discharge transients that can lead to the turn-off of the SM control logic power supplies. In Fig. 9, flying-capacitors currents (top) and voltages (bottom) are reported, showing limited oscillations during the whole transient and the desired steady state behaviour. Eventually, the overall duration of the entire start-up is limited to a few seconds.

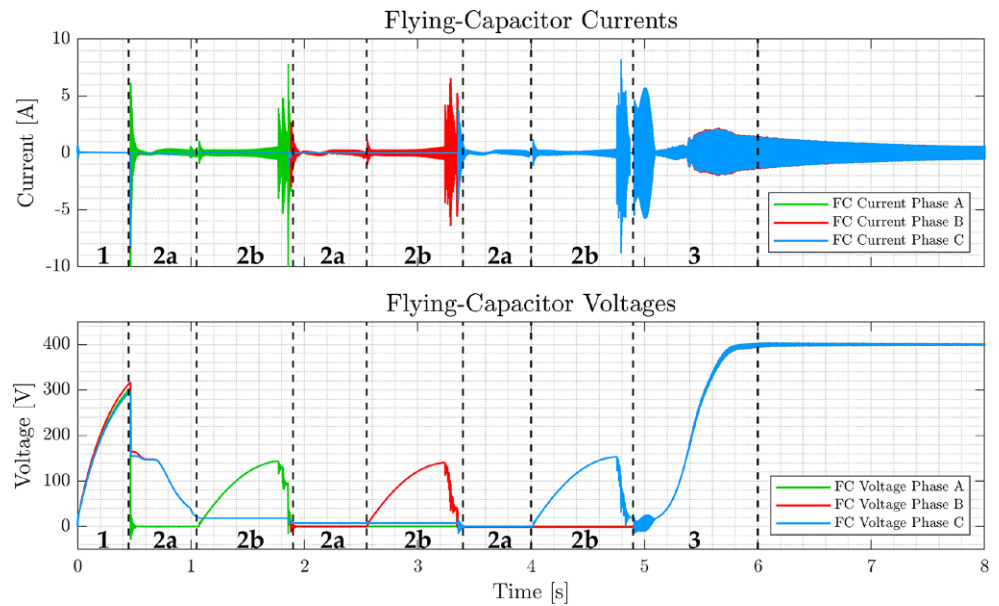
## 7 Coupled sub-arm inductor design

In order to reduce the overall size, weight and cost of the magnetic components, a new coupled inductor solution is put forward in this paper, [10, 16]. Thus, for a three-phase MMC, the inductor count is reduced to only six, with respect to the twelve of the initial discrete inductor approach. The main idea to effectively couple the inductors is to combine the current components (3)–(4) in order to reduce the current that actively generates the inductor flux. As reported in the right-hand side schematic of Fig. 1, coupling between the sub arm inductors of the outer loop and the ones of the inner loop is proposed, leading to the following expression for the inductor flux:

$$\begin{aligned} \lambda_{tot}^{co} &= Li_{xu,1} + Mi_{xl,2} + Li_{xl,2} + Mi_{xu,1} \\ &= 2(i_{d,x} + i_{h,x})(L + M) \end{aligned} \quad (10)$$



**Fig. 9** Flying-capacitor currents (top) and voltages (bottom) during the pre-charge/start-up of the converter. The numbers 1, 2a, 2b and 3 mark the various stages of the algorithm



Therefore, the coupled inductor flux depends on twice the sum of the low-frequency  $i_{d,x}$  and high-frequency injected current  $i_{h,x}$ , with no dependency on the output load current. Regarding the inductance values of (10), two possible solutions can be adopted for the coupled sub-arm inductor. Assuming a fixed resonance frequency (between sub-arm inductors and flying-capacitor) used for the high-frequency injection as described in [1, 3], the self inductance value of the coupled inductor can be assigned as  $L = L_{\text{sub}}$ ; otherwise, the inner loop inductance value can be assumed equal to the coupled inductance of the single inductor case, i.e.,  $L_{\text{sub}} = L + M$ . In the first scenario, the mutual inductance term  $M$  allows to reduce the flying-capacitor capacitance  $C_f$ . However, this would result in a non-effective inductor size reduction and an increased voltage at the flying-capacitor terminals. On the contrary, the second approach allows to maintain the flying-capacitor unchanged with respect to the discrete inductor case, but the inductor flux can be largely reduced, leading to a significant size reduction. Based on those considerations, it is possible to give an expression for the area products (i.e., the product of core cross-section area and winding area) in the discrete and coupled cases ( $D$  and  $C$  superscripts, respectively):

$$A_p^D = \frac{L_{\text{sub}} I_{pk}^2}{B k_r k_c J}, \quad A_p^C = \frac{2(L+M) I_{pk} (i_{d,x} + i_{h,x})}{B k_r k_c J} \quad (11)$$

Some conclusions regarding the result can be derived by analyzing the numerators, since the denominators are identical. Being  $L_{\text{sub}} = L + M$ , it is possible to write the statement  $2A_p^D \geq A_p^C \Rightarrow I_{pk} \geq (i_{d,x} + i_{h,x})$ , which is always true since  $I_{pk} = i_{d,x} + i_{h,x} + i_x$ . Therefore, since the area product is a figure of merit strictly related to the physical size of the inductor, it can be concluded

that the proposed design is an interesting solution to reduce the size and cost of the magnetics.

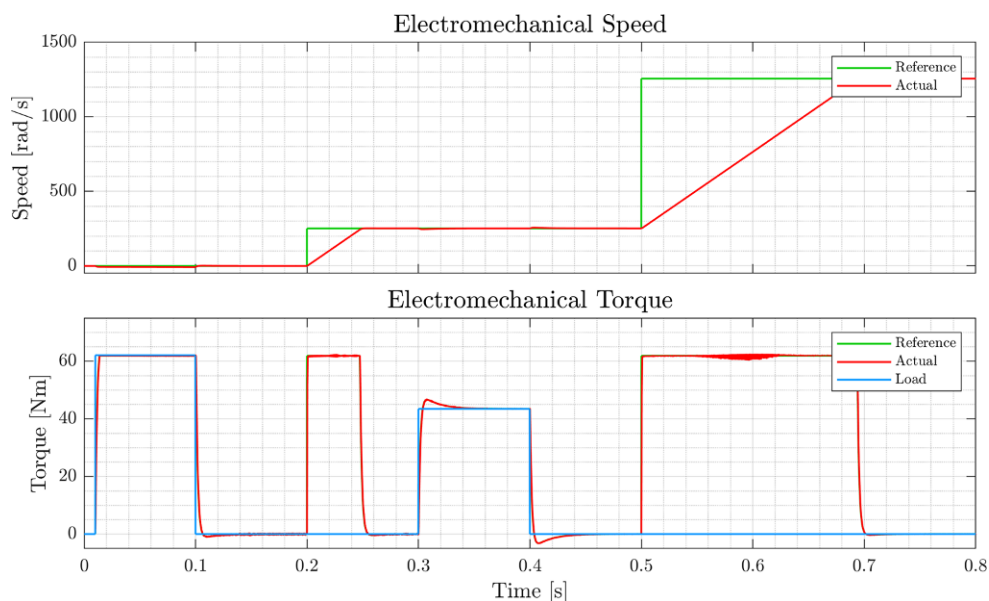
## 8 Simulation results

A 22 kW PMSM drive, whose converter and machine parameters are reported in Tables 1 and 2, respectively, is considered to validate the proposed converter architecture. An accurate simulation model has been developed in order to take into account the implementation system, i.e., the requirements and constraints of the distributed control architecture, communication and related latencies. The fundamental step to simulate the implementation of the proposed control architecture is the implementation of the SM scheduling diagram reported in Fig. 5. Taking into account the proper scheduling of bus access, it has been possible to simulate data packet traffic according to the proposed design solution. The whole process of elimination of redundant information, data aggregation, and control task scheduling results in an improved communication scheme that allows to loosen the constraints on the required link data rate, and come up with the proposed control architecture implementation. At the same time, the converter performance (in terms of output regula-

**Table 2** PMSM parameters

Rated torque	$T_n$	62.7 Nm
Rated speed	$n_n$	4000 rpm
Pole pairs	$p_p$	3
Rated current	$I_n$	52 A
Phase resistance	$R_s$	54 mΩ
Phase inductance	$L_d = L_q$	470 μH
PM flux linkage	$\Lambda_{mg}$	0.187 Wb

**Fig. 10** Torque and speed response: electrical speed (top) (reference: green, actual: red) and torque (bottom) (reference: green, actual: red, load: blue)



tion, reliability and robustness) is not affected by the distributed control implementation choices.

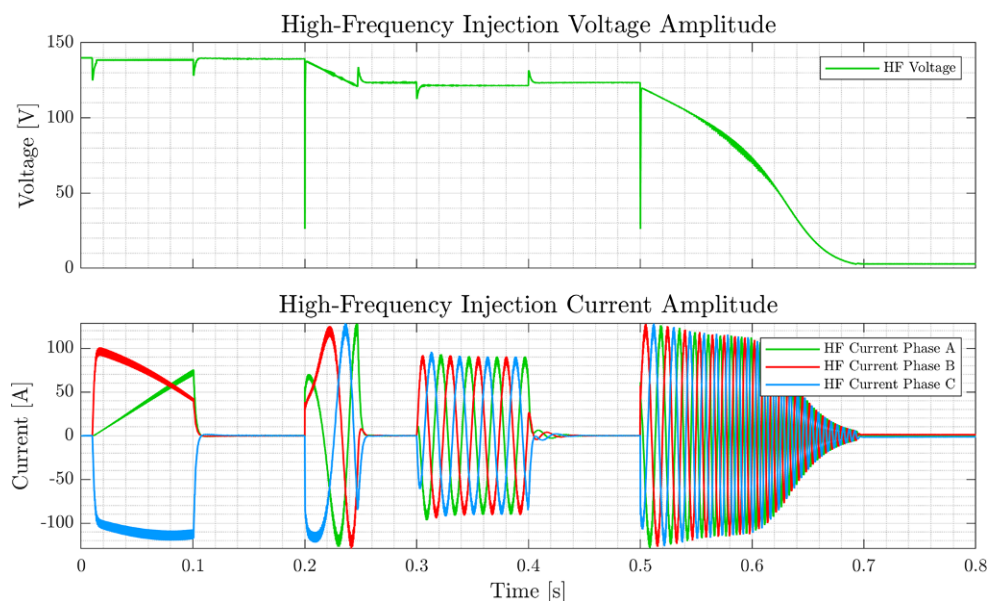
Selected simulation results are reported hereafter, with the aim of proving the effectiveness of the control, especially regarding the voltage balancing issues, even at high load torque in zero/low-speed conditions. The torque and speed profiles applied in the tests are reported in Fig. 10. The energy balancing action described in [1] is performed through the combined high-frequency injection. The amplitudes of those contributions are shown in Fig. 11, in the top and bottom diagrams, respectively. Those signals will be high-frequency modulated before being fed to task R. It is worth to highlight that also the high-frequency injection shutdown procedure proposed in [1] is clearly visible in Fig. 11. The output currents are shown in Fig. 12, both in the synchronous  $dq$  reference frame (top two subplots) and in the three-

phase stationary reference frame (bottom subplot). Eventually, validation of the proposed strategy for the balancing of capacitor voltages is reported in Fig. 13, considering the SMs of leg A. As can be seen, the voltage ripple is limited to less than 10 % of the rated SM voltage during the whole test pattern. This has been possible thanks to the adaptation of the arm differential-mode energy control and shutdown strategy proposed in [1].

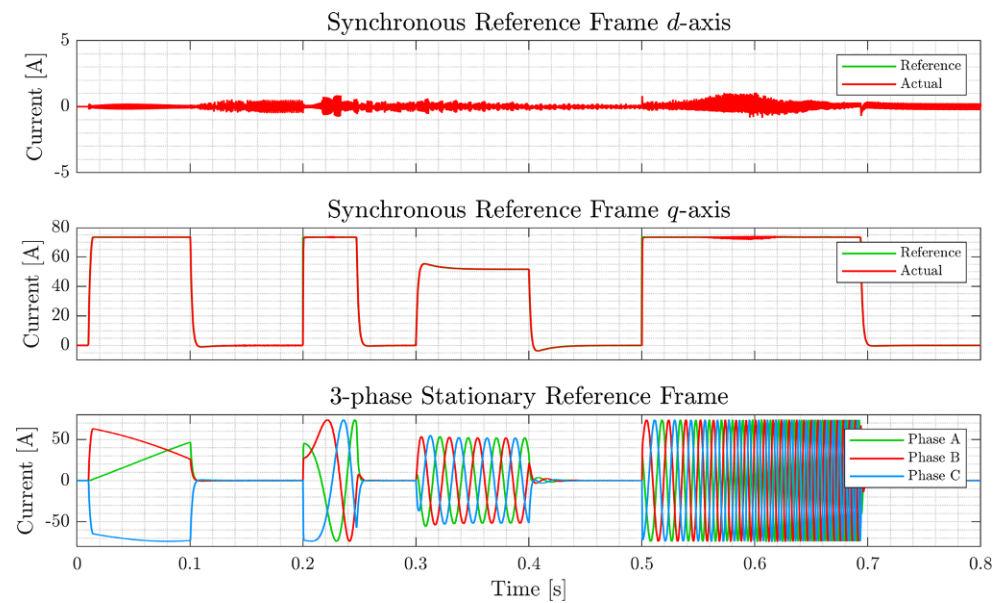
## 9 Hardware prototype design

A down-scaled prototype of the converter, with the related control boards, has been developed and designed. Compactness and modularity were the main design criteria for the converter prototype, whose 3D renderings of the SM and the CU assemblies are shown in Fig. 14. The SM features a sandwich struc-

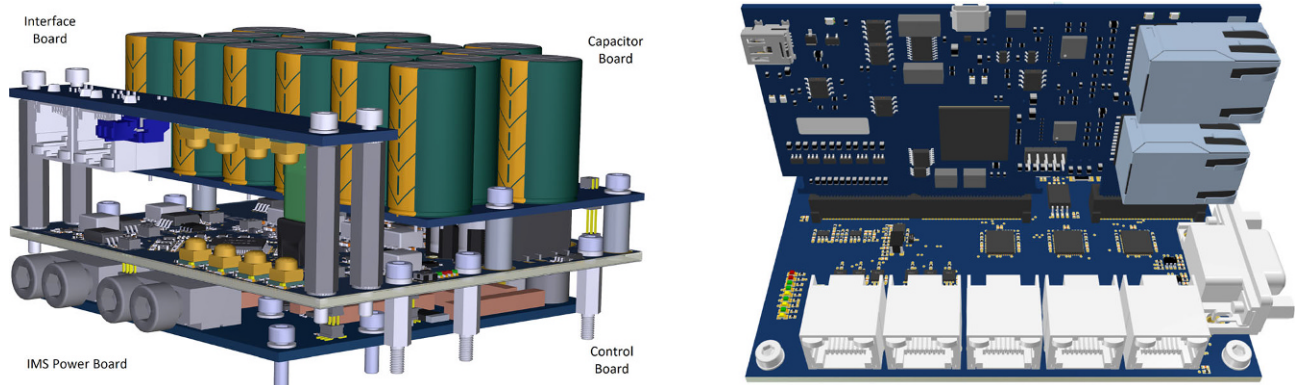
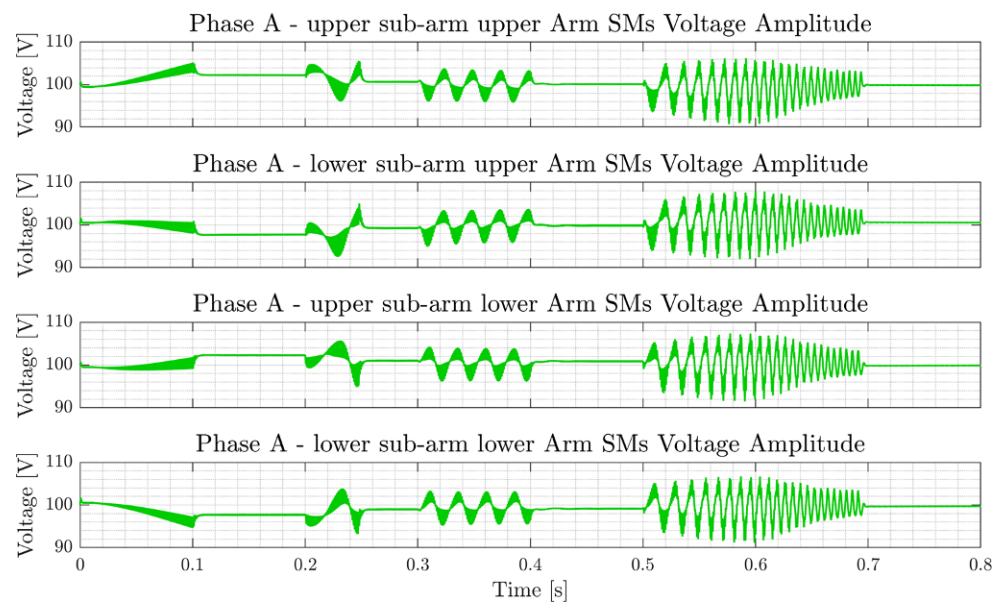
**Fig. 11** High-frequency injected voltage (top) and currents (bottom) amplitudes



**Fig. 12** Output currents behaviour: synchronous  $dq$  reference frame (top two subplots) and three-phase stationary reference frame (bottom subplot).



**Fig. 13** Phase A SMs capacitors voltages



**Fig. 14** 3D renderings of the converter prototype: submodule (right) and central unit (left) assemblies



ture that includes: a power board (bottom) based on an insulated-metal-substrate (IMS), where power semiconductors and interconnections are mounted; a control board (middle), hosting the SM microcontroller, the gate drivers, and communication devices; and the capacitor board (top, rear). An additional board (top, front), which is mounted on insulating spacers, hosts the ground-referenced side of the optical interface between the communication bus and the SM control electronics. Regarding the CU, its structure only consists of a control card hosting a dual-core microcontroller, the encoder connector on the right, and the RJ45 ports for the connection to the communication bus.

## 10 Conclusions

In this paper, novel concepts and control solutions aiming at extending the application range of MMCs to medium voltage high-performance variable speed drives have been presented. The main features of this class of converters are highlighted to justify their adoption in such demanding applications. The limitations of these topologies have been discussed and some of the major problems in MMC design and control for VSD applications are addressed, namely the reduction of the SM capacitors voltage ripple in the whole torque/speed operating range, the proper and safe pre-charge/start-up of the converter and the optimized design of the magnetic components based on a novel coupling concept.

A down-scaled MMC prototype has been designed and the related parameters are considered in the simulations. The 3D rendering of the SM and CU assemblies demonstrates the compactness and modularity of the system. The effectiveness of all the proposals is demonstrated by accurate simulation of a 22 kW PMSM drive, including the effects of real-time communication and processing latency.

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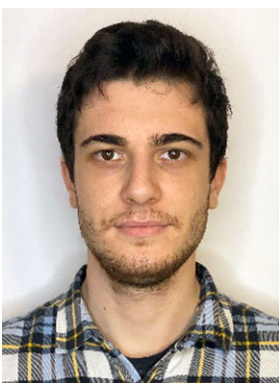


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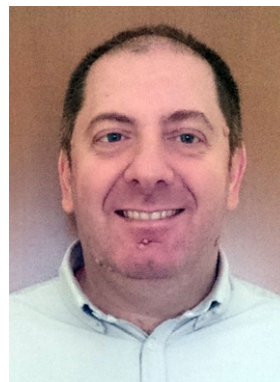


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