Originalarbeit

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The impact of DC-bus impedance on the switching performance of low-voltage silicon power MOSFETs

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Abstract Typical DC-bus stabilization for low-voltage power circuits consists primarily of ceramic capacitors due to the capacity density and low equivalent series resistance (ESR) resulting in low conduction losses. Particularly in hard-switching and hard-commutation operation, the low ESR and high equivalent series inductance (ESL) of the capacitors in the commutation path restrict the damping of the switch node voltage overshoot and introduce high-frequency ringing, reducing the voltage margin of the transistor. Therefore, this paper analyzes the impact of the DC-bus impedance and proposes a DC-bus snubber based on an RC network to form the DC-bus impedance's characteristic, which minimizes the overshoot voltage. A comprehensive simulation using measurement-derived component models is shown, which is verified by an in-situ measurement on a test PCB. Furthermore, transient measurements using a double pulse test setup show the effectiveness of the proposed approach.

Keywords Synchronous buck converter · DC-bus impedance · MOSFET switching performance · DC-bus snubber · Overvoltage damping · Voltage margin

Einfluss der Zwischenkreisimpedanz auf das Schaltverhalten von LV-Silizium-basierten MOSFETs

Zusammenfassung Eine typische Zwischenkreisstabilisierung für Niederspannungsstromkreise besteht hauptsächlich aus Keramikkondensatoren, da die Kapazitätsdichte und der niedrige äquivalente Serienwiderstand (ESR) zu geringen Verlusten in den Bauelementen führen. Insbesondere beim harten Schalten bzw. Kommutieren beschränken der niedrige ESR und die äquivalente Serieninduktivität (ESL) der Kondensatoren im Kommutierungspfad die Dämpfung des Überschwingens der Schaltknoten- und Zwischenkreisspannung, wodurch die Spannungsreserve des Transistors reduziert wird. Daher befasst sich dieser Artikel mit dem Einfluss der Zwischenkreisimpedanz und schlägt einen Zwischenkreis-Snubber vor, der auf einem RC-Netzwerk basiert. Damit wird die Charakteristik der Zwischenkreisimpedanz beeinflusst, wodurch die Spannungshöhe des Überschwingens am Schaltknoten und an der Halbbrücke reduziert wird. Basierend auf messtechnisch erfassten Bauteilwerten wird eine Simulation der Zwischenkreisimpedanz gezeigt, welche durch eine Messung mittels einer bestückten Leiterplatte verifiziert wird. Darüber hinaus werden in diesem Artikel transiente Messungen mit einem Doppelpuls-Testaufbau gezeigt, und die Wirksamkeit des Zwischenkreis-Snubber wird verifiziert.

Schlüsselwörter Synchroner Abwärtswandler · Zwischenkreisimpedanz · MOSFET-Schaltverhalten · Zwischenkreis-Snubber · Dämpfung der Überspannung · Spannungsreserve

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1 Introduction

Low voltage (LV) silicon power MOSFETs are commonly adopted in switching power electronic converters in different kinds of topological configurations. The half-bridge one is the natural choice in non-isolated high-efficiency high-current DC-DC conversion, where synchronous rectifying operation allows a strong reduction of the conduction losses. The switching behavior is greatly affected by the non-linear characteristics of the output capacitance, parasitic inductance of the package, leads and PCB traces, as well as possible significant reverse recovery charge due to the non optimal characteristics of the intrinsic diode. This contributes to both an increase of the switching losses, and to a significant voltage overshoot and ringing at the switch node and across the entire leg, resulting in a reduction of safety margin or even a possible damage of the device.

Accurate modelling of the switching oscillation and overshoot phenomena in case of SiC power MOSFETs is provided in several recent papers, [4, 6, 7], as the faster commutation waveforms of these devices amplify the detrimental effects of the circuit layout and parasitic elements. Equivalent circuit-level analytical models are reported and validated, incorporating all major parasitic contributions and analyzing how they affect both turn-on and turn-off behavior.

Most effective mitigation strategies of overshoot and ringing are mainly based on either slowing down the switching transient, leading to increased switching losses, or by the minimization of the parasitic elements in the switching loop, i.e., DC-bus impedance across the half-bridge leg and physical layout of the switching cell has to be carefully considered and designed.

Like with standard silicon power MOSFETs, SiC devices also show reverse recovery effects within the body diode and a non-linear output capacitance characteristics, but the contribution to the switching losses and to the voltage overshoot and ringing is comparatively low, except for very fast switching transients. Although they are used with a higher nominal DC-bus voltage, the effect of overshooting switch node voltage is mostly uncritical, slightly affected by the very low output capacitance. The selection of voltage classes for SiC technology is also strictly grouped, in contrast to low-voltage silicon power MOSFETs. Therefore SiC devices can be selected individually to fit the desired DC-bus voltage, without any specific issues in maintaining enough safety voltage margin. On the other hand, any kind of additional voltage overshoot has to be considered in the low-voltage case, thus reducing the safety margin, or requiring a device with a higher maximum drain-source voltage rating, which decreases performance or increases costs.

Shaping of the DC-bus impedance is probably the most effective solution and it is normally done by placing additional passive elements in a specific position of the PCB, e.g. an RC or C-RC snubber network across the switching cell or the main DC-bus capacitor. This method is generally known for filter networks and [2] provides a good summary about it. This approach attracted most attention in the last years and the related design methods have been reported in several papers, [1, 8–10].

In [10] a double pulse circuit is used to analyze the ringing suppression effects of RC snubber circuit placed across the half-bridge leg. A high-frequency equivalent circuit of the double pulse circuit is derived and an RC snubber circuit for ringing suppression is analytically designed by scrutinizing the characteristic equations via the root locus method. The ringing suppression effect of the designed RC snubber is confirmed via circuit simulations and experimental demonstrations.

In [1] a DC-bus RC snubber circuit is considered to suppress the parasitic ringing in high-speed, hard-switched converters with SiC MOSFETs. Unlike the traditional RC or RCD snubber across the switch drain-to-source terminals, allowing to suppress ringings by slowing down the dv/dt and therefore increasing the switching losses, [3], a snubber across the DC-bus dampens only the high-frequency ringing and does not increase the switching loss. By analyzing a small-signal impedance network relating the time-domain ringing to the frequency-domain Bode plots, the R-C combination that achieves the best damping effect is calculated. The most interesting contribution of this paper is that closed-form expressions are developed so that the proposed method can be easily implemented in actual designs.

In [8] the switching transient of SiC MOSFET with DC-bus RC snubber is investigated and an analytical model based on a finite state machine (FSM) is proposed. The authors claim that this approach is able to depict the whole switching actions of the SiC MOSFET with high accuracy, as demonstrated by the comparisons between the calculated and measured waveforms during the switching transition. A comprehensive investigation of the impacts of RC snubber on switching oscillation, switching loss, and high-frequency EMI noise is reported. An interesting outcome is that they prove that the added RC snubber does not bring any additional switching loss in the circuit.

One of the open issues still is the additional losses which are introduced at the snubber level. This is investigated in [9], where an optimized snubber circuit based on a C-RC network is proposed. It is demonstrated that it can not only suppress the switching oscillation and overvoltage, but also effectively reduce the snubber loss compared with the standard DC-bus RC circuit. This will be beneficial to the actual application of this snubber into the high-power and high-frequency field.

In this paper this topic is further investigated with reference to low-voltage silicon power MOSFETs,

which have been used in a recent very high power density battery charging applications, [5]. A half-bridge configuration is considered for the analysis and a proper RC snubber circuit is designed and evaluated, both from simulation and experimental tests. The impact of the snubber is investigated by proper impedance measurements on a wide spectrum range by dedicated test setup, allowing impedance measurements with different snubber and DC-bus capacitor positions. Time domain analysis is also reported based on a double pulse testing setup. Time transient behavior of the switching node voltage and DC-bus at the input of the switching cell are considered, aiming at highlighting the effects of the different impedance shaping in zero current switching, hard commutation and zero voltage switching. The reported results confirm the effectiveness of the analyzed solutions and the validity of the theoretical and simulation investigations. Damping of the switch node voltage overshoot and ringing is possible, thus allowing a better exploitation of the power MOSFET voltage capabilities and reduced EMI issues.

2 DC-bus snubber

The voltage overshoot of a switch node voltage is mainly defined by the commutation loop inductance and the di/dt of the switched current. Especially the commutation of the current from one power electronic device to the other one is crucial, because of their nonlinear junction capacitance and reverse recovery charge characteristics. Fig. 1 shows the configuration being analyzed in this paper, which is a half bridge configuration with 100 V 4 mΩ low voltage silicon based MOSFETs from Infineon (BSC040N10NS5SC). As shown in Fig. 1 the DC-bus snubber consists of a series connection of a small ceramic capacitor and a resistor. This snubber is considered to be placed as close as possible to the half-bridge and paralleled to reduce the total impedance at the switching cell. A lumped equivalent circuit model taking the parasitic components (e.g., the PCB inductances L_{PCB1} and L_{PCB2}) into account is shown in Fig. 2. Minimizing the distance to the transistors has the advantage of reducing L_{PCB2} and thus the need to position the main DC-bus capacitor C_B very close to the power transistors, which highly relieves layout constraints. This is especially beneficial in case top-side cooled devices are used, because the distance between the PCB and the heat sink is somehow effectively constrained to the height of the transistor. Consequently, placing a mechanically smaller DC-bus snubber is a preferred choice as compared to moving the main DC-bus capacitors close to the switching cell.

Considering the commutation loops in Fig. 2, a more detailed overview into the circuit parasitics involved in the commutation transients and sequence can be understood. In particular, the commutation sequence is important to understand the operation and contribution of the DC-bus snubber.

In the first step, the output current i_1 is considered to be positive (exiting from the output node of the leg) and conducted via the low-side body diode, as the lower switch is supposed to be already in the off-state (end of the dead-time period). Therefore the output voltage u_{sw} node is slightly negative according to the forward characteristic of the body diode. If the high-side transistor is now turning on, it will have to commute the current i_1 from the low-side diode, thus charging the equivalent output capacitance C_{LS} and supplying the reverse recovery charge too. This results into a high current which has to be provided by the main capacitor in case no DC-bus snubber is adopted. Therefore, the commutation loop involves all the series parasitic inductances shown with the blue arrow **III** in Fig. 2. Especially when the main DC-bus capacitor C_B loop exhibits a considerable amount of parasitic inductance, due to its placement far away from the switching cell, this introduces a resonance frequency f_{res} given in Eq. 1 and peak overshoot value defined by the stored energy in the commutation loop

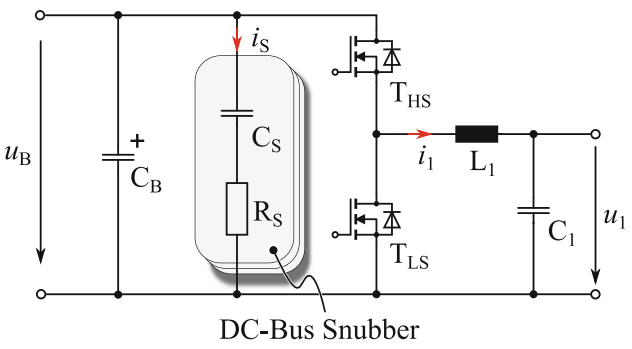

Fig. 1 Schematic of a typical buck converter with an added snubber network in parallel to the DC-bus capacitor. u_B describes the DC-bus voltage, i_S the current through the snubber networks and u_1 represents the output voltage

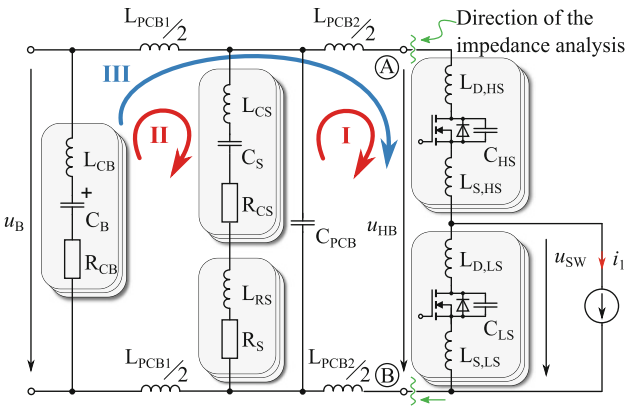

Fig. 2 Detailed schematic with parasitic elements including the package inductance of the switches, the parasitic inductance and series resistances of the DC-bus and snubber capacitors as well as the package inductance of the snubber resistor

inductance L_{CM} and the output capacitance C_{oss} of the power switches. It leads to an overshoot which increases with its commutation loop inductance and it is also transiently affected by the equivalent series resistance of the main DC-bus capacitors. If the DC-bus snubber is taken into account and its position is close to the power switches, the commutation loop inductance is reduced and it is mainly defined by the package inductance of the switches, a lower parasitic inductance of the PCB, and the parasitic inductance of the snubber circuit.

$$f_{res} = \frac{1}{2\pi \cdot \sqrt{L_{CM} \cdot C_{oss}}} \tag{1}$$

$$R_S = 2 \cdot \sqrt{\frac{L_A}{C_S}} - R_{CS} - R_{CB} \tag{2}$$

$$L_A = L_{CB} + L_{PCB1} + L_{CS} + L_{RS}$$

$$C_B \gg C_S \gg \begin{cases} C_{PCB} \\ C_{LS} \\ C_{HS} \end{cases}$$

The inductance and therefore its impedance from the blue commutation loop **III**, as shown in Fig. 2, is much higher so the current will mostly be conducted by the red commutation loop **I**, resulting in a much higher resonance frequency and a smaller overshoot voltage of the switch node as compared to the commutation sequence mentioned before. During the commutation sequence without the DC-bus snubber involving loop **I**, the capacitors C_S will discharge, therefore decreasing its voltage and triggering the recharging event indicated by loop **II** in Fig. 2. In general the DC-bus snubber acts also like a resistor, which is very important in the charging sequence **II**, because the two capacitors C_B and C_S will resonate between each other via their internal parasitic inductance as well as the PCB inductance L_{PCB1}. To damp this resonance, the series resistance of the DC-bus snubber has to be adjusted to achieve an aperiodic behaviour as shown in Eq. 2 considering the component parameters of Fig. 2. The impact of L_{PCB2}, C_{PCB}, the transistors output capacitance C_{oss} (C_{HS} and C_{LS}) in combination with their parasitics, play a minor role because of the smaller capacitance values compared to the snubbers capacitance. The benefit of this method is that the initial commutation current will be provided by the DC-bus snubber, thus reducing the stress of the transistors by partly limiting the current through them. This is done by a descending voltage u_{HB} during the commutation while keeping the commutation loop as small as possible, and damping the charging current of the DC-bus snubber with its optimal DC resistance, so that any kind of additional resonance will be damped properly. To further reduce the overshoot in the commutation loop **I**, paralleling of the transistors was considered, so that the package inductance will be halved and thus pushing the resonance frequency between the snubber and the switches capacitor's even higher.

2.1 *Modeling and simulation of the DC-bus impedance*

Considering the beforehand described effects of the commutation, this section describes the impact of adding the DC-bus snubber characteristic to the original DC-bus impedance as seen from the commutation current. Especially, in low-voltage applications, ceramic DC-bus capacitors are used to stabilize the DC-bus voltage by storing the amount of charge needed for a given voltage drop during transient events. Therefore typical package size is large (e.g., case code 2220 has a size of $5.7 \times 5.0 \times 3.5\,\mathrm{mm}^3$) and it is difficult to be mounted close to the switching device/cell. On the other hand, the capacitors of the DC-bus snubber have to be small from a mechanical point of view, so that they could be fit very close to the power switches. Moreover, they should exhibit low parasitic inductance, so that they still provide low impedance especially in the frequency range where the ringing is expected to happen. While the perfect resistance value is already defined by Eq. 2, the optimal capacitance value is still unknown. Therefore some simulations of the DC-bus impedance as seen by nodes A and B in Fig. 2 were carried out. For the simulation, typical parameters for the DC-bus voltage of 60 V were selected, as well as a maximum switched current of 40 A. These values are based on a recent high power density battery charger application [5] to supply an intermediate voltage rail. First, the parts according to Table 1 were considered for simulation without any snubber circuit. It only contains the main DC-bus capacitors C_B, including its parasitics, as well as the PCB plane capacitance and inductance. The result of this simulation is shown in Fig. 3 in blue. Clearly, the impedance characteristic of eight parallel connected DC-bus capacitors can be seen as well as the peak at 100MHz representing the resonance between the capacitors parasitic inductance, PCB inductance and the PCB capacitance, thus resulting in a ringing at the mentioned frequency.

The red curve of the same figure is related to the simulation model with eleven snubber elements, whose parameters are also reported in Table 1. Comparing the two simulation results, one can notice a significant difference in the high-frequency range due to the frequency shaping of the snubber network. In particular, the resonance at 100MHz is completely eliminated and the magnitude of the impedance around that frequency range is absolutely reduced. A highly damped additional resonance is present in the red curve at a lower frequency due to the additional capacitive contribution of the snubber network. Additionally the impedance shows now a significant resistive behaviour illustrated in Fig. 3. This is pro-

Table 1 Details of the chosen components and its values, including the measured parasitics and package values, as shown in schematic of Fig. 2. Note that the sum of the package parasitics is listed in this table

Name	C	L	R	Manufacturer	Part number	Number of elements used in:	
–	(nF)	(nH)	(mΩ)	–	–	Simulation 1	Simulation 2
DC-bus capacitor							
C_B	10250	3.94	2.20	KYOCERA	AVX 22201C106KAT2A	8	8
DC-bus snubber							
R_S	–	0.94	980	KOA Speer	RK73H1JTTD1R00F	0	11
C_S	2.97	1.77	61	Würth Elektronik	885342206005	0	11
PCB*							
L_{PCB1}	–	1.05	–	Custom made PCB	–	1	1
L_{PCB2}	–	0	–	Custom made PCB	–	1	1
C_{PCB}	1.62	–	–	Custom made PCB	–	1	1
MOSFET							
T	0.550**	0.20	4	Infineon	BSC040N10NS5SC	0	0

* for an arrangement as shown in Fig. 7
** for $V_{DS} = 60\,V$

vided from the series damping resistors for lowering resonance currents.

The different possible positions of the snubber networks has not been considered for this analysis, as the parasitic contribution of the DC-bus on the overall inductance could be neglected as it is made out of interleaved ground and power planes, and the considered frequency range is well below any kind of wave effects.

The choice of the number of snubber elements which should be considered and simulated is a degree of freedom that could be exploited in order to reduce the peak voltage overshoot Δu_{sw}.

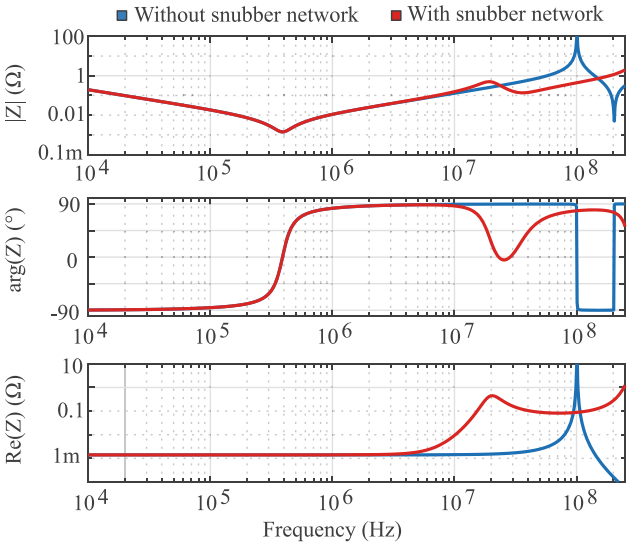

Fig. 3 Simulation of characteristic curves of the magnitude, phase and real part of the impedance Z as seen from the terminals A and B **with** (*red*) and **without** (*blue*) the DC-bus snubber network

2.2 *Models of adopted components including parasitics*

High fidelity modeling and simulation of the DC-bus impedance and evaluation of the contribution of the snubber network requires an accurate characterization of the actual frequency dependant model of each component adopted in the circuit, i.e., including all their parasitics. Impedance measurements were performed using a Keysight E4990A Impedance Analyzer and approximated based on an equivalent model for each component individually according to Fig. 2.

Table 1 gives a detailed overview of the measured results and equivalent lumped model parameters. While the parameters of the individual component parasitics and PCB plane capacitance can be easily measured or simulated, the parasitic inductance of the PCB is more difficult to obtain. To overcome this problem, it was decided to measure first the PCB plane capacitance alone, then the main DC-bus capacitors were soldered in and the impedance with the analyzer has been measured by probing directly on the pads A and B, shown in Fig. 2. The results of this measurement exhibits a resonance frequency which can be used to calculate back an estimate of the plane inductance L_{PCB1}. L_{PCB2} represents the inductance of the small distance between the measurement points A and B to the MOSFETs, it was estimated that the value is in the pH range and therefore the element was neglected for the analysis within this paper.

3 Performance Evaluation

The effectiveness of the impedance shaping by DC-bus snubber has been experimentally evaluated on a test circuit in an actual application scenario, [5]. In this section the experimental setup will be sketched first, highlighting the physical positions of the switching cell, the DC-bus capacitors, the snubber networks

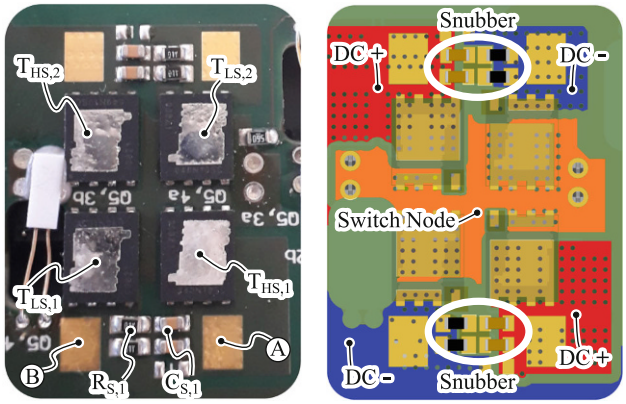

Fig. 4 **a** Arrangement of the power MOSFETs within the switching cell on the bottom side of the PCB. **b** PCB layout of the most outer layer, showing the location of the DC-bus and switch node. Note, the connection between the polygons is done in the inner layer. Fig. 13b gives more details

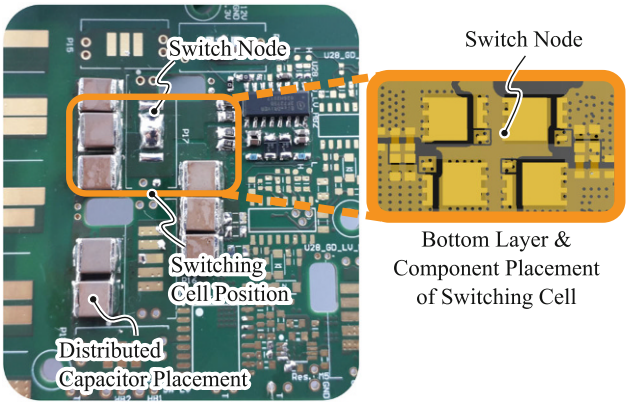

Fig. 5 Distributed placement of the DC-bus capacitors. The enlargement shows the position of the switching cell layout and components on the bottom side

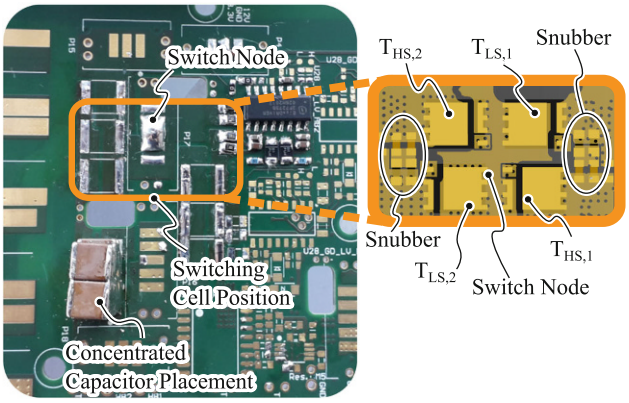

Fig. 6 Concentrated (non-ideal) placement of the DC-bus capacitors

and the measurement points and probing setup, this last being a very important aspect to be considered for reliable measurement results. Then, the frequency domain response by the impedance measurements and the time domain response by the double pulse testing are presented and discussed, highlighting the beneficial effects of the snubber network and the differences between various scenarios.

3.1 Hardware test setup

The test hardware used for evaluating the performance consists of an eight layer PCB containing several power and ground planes which are interleaved to minimize the equivalent inductance and maximize the DC+ to DC− plane to plane capacitance. The switching cell arrangement is shown in Fig. 4 and highlights the position of the snubbers $R_{S,1}$ and $C_{S,1}$ next to the power transistors $T_{xS,y}$ (x = H,L;y = 1,2) which are placed in a crossover configuration.

While the bottom layer of the PCB is used to connect the individual devices to each other, the layer immediately above acts as a ground plane and is connected to the negative DC-bus to provide a return path for the current. The top side of the PCB is shown in Figs. 5 and 6, where the different placement variations of the main DC-bus capacitors are considered and highlighted (distributed and concentrated), while the gate driver, the main switching inductor, and supply cables were kept at the same position.

In Fig. 5 the optimal solution for placing the main DC-bus capacitors is considered, i.e., they are distributed throughout the switching cell and directly placed at its opposite side, thus reducing the parameter L_{PCB1} to approximately its minimum value. On the other hand, the arrangement reported in Fig. 6 considers a concentrated placement of those capacitors, approximately 2 cm away from their ideal position and stacked in the vertical direction to represent a high area density assembly case.

As shown in Fig. 4 the DC-bus snubbers are placed next to the MOSFETs in pairs of two. Still, the test PCB contains more switching cells, which are actually not used. Even though it was considered to place snubbers next to them, because of the influence on the impedance of the DC-bus. The impact of distributed snubbers have been evaluated by considering the probing position shown in Sect. 3.3.

Measurements have been made using passive probes with a bandwidth of 500 MHz for the gate signal, DC-bus and switch node voltages, whereas 1 GHz low-voltage active differential probes have been used to measure the voltage across the snubber resistors, providing a rough estimation of the conducted current through the snubber cell. Fig. 7 shows the test setup including probes.

3.2 Impedance measurements

To verify the effectiveness of the proposed impedance shaping approach, this section builds from the component level impedance measurements in Sect. 3,

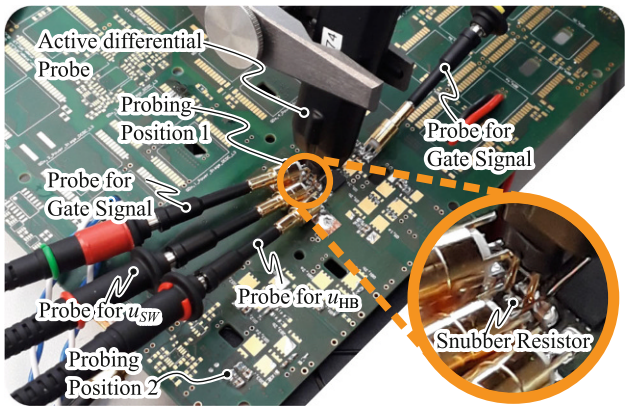

Fig. 7 Probing positions in the test setup. Note the position for the differential probe, which is used for voltage measurement across the DC-bus snubber resistors in the enlargement

which aimed to extract the equivalent model of each component considered in the simulation, to total impedance measurements performed at PCB level.

The test PCB has been assembled with the snubber networks on the bottom side, as shown in Fig. 4, and the main DC-bus capacitors according to the layouts in Figs. 5 and 6 (i.e., the already discussed distributed and concentrated cases, respectively).

The first issue that should be considered when approaching these type of measurement is the design of a proper test setup for obtaining the required accuracy and in-field calibration of the probing. In fact, according to the simulation results, a very low value of the DC-bus impedance can be expected over the considered frequency range, with an increase of the real part of the impedance above 20 MHz to values in excess of 0.1 Ω.

A custom in-field test fixture was designed and built which compensates the distance between the probing positions A and B (as shown in Fig. 4) and the impedance analyzer properly. The test fixture with the two probing points C and D is illustrated in Fig. 9.

The probe is soldered onto a solid copper sheet to allow the initial short calibration, while the open calibration is performed by lifting the measurement points C and D from the sheet, and connecting each individual source and measure signals together with a small soldering joint. After completing the calibration procedure, the measurement points (both source and measure) have been soldered onto the desired PCB nodes A and B for impedance measurements.

The obtained results are shown in Fig. 8 for two cases: when the snubber networks are not mounted (Fig. 8a), and when they are (Fig. 8b). Additionally the simulation results of Fig. 3, characteristic curves of the magnitude, phase and real part of the impedance Z as seen from the A and B terminals are reported. Three curves are plotted: simulated impedance (red curve), measured impedance with concentrated DC-bus capacitors (blue curve), and measured impedance with distributed DC-bus capacitors (green curve).

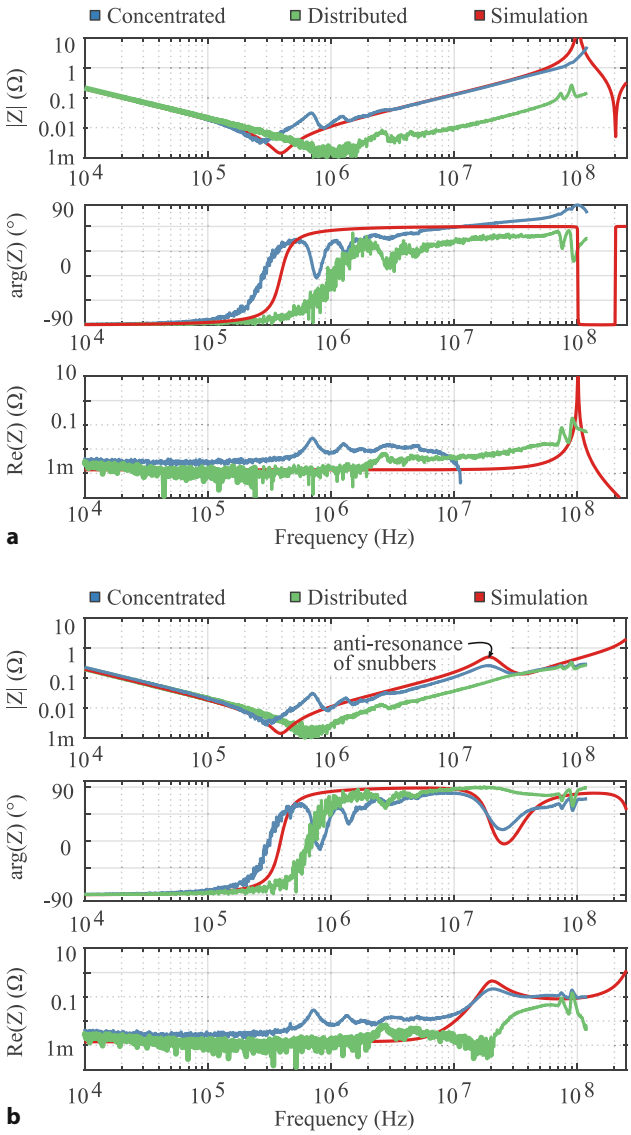

Fig. 8 Measured (*blue, green*) and simulated (*red*) characteristic curves of the magnitude, phase and real part of the impedance Z as seen from the A and B terminals: **a without** and **b with** DC-bus snubber networks

Fig. 8a shows that the experimental curve without snubbers and concentrated placement. The simulated curve match almost perfectly, as the simulation model is indeed a concentrated one. The experimental result with distributed placement highlights that quite a huge reduction of the impedance is achieved in a wide frequency range, providing beneficial effects on the switching behavior. Also, several resonance points between 700 kHz and 3 MHz are present in both cases (without and with the snubber networks), as concentrated DC-bus capacitors are resonating between each other because of the vertical stacking.

From the results of Fig. 8b it can be clearly seen that for the concentrated placement of the DC-bus capacitance the snubbers are fulfilling the expectations above 10 MHz, with an anti-resonance frequency at

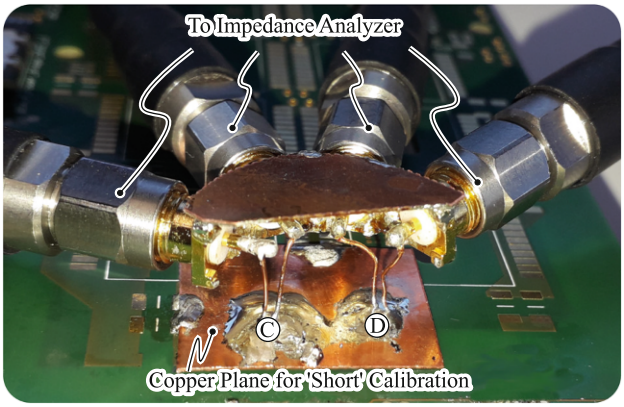

Fig. 9 Probing position for 'short' calibration within the test setup. For a more reliable measurement the probe tips have been soldered to the copper plane

18.6 MHz compared to the expected 19.5 MHz. Additionally, the peak impedance at this anti-resonance frequency is lower than expected from simulation (0.25 Ω compared to 0.49 Ω), resulting in a reduced overshoot when charging and discharging the DC-bus snubbers from the main DC-bus capacitors.

Additional remarks on the results shown in Fig. 8: any impedance measurement is very sensitive to variation of the probing position and connection of the probing points. As a result, the impedance of the test setup with distributed DC-bus capacitors including snubber networks seems to be higher than the setup without, which is not expected. This result in an inductance difference below 500 pH, representing the lower boundary of the measurement accuracy.

3.3 Double pulse testing results

In this section time domain transient responses of the different configurations of the test circuit are reported, as obtained by double pulse tests, whose setup is shown in Fig. 12. The aim is to verify the switching performance with respect to peak switch node voltage u_{SW} overshoot, ringing frequency and DC-bus voltage u_{HB} drops. All the tests consider the same DC-bus voltage of 60 V and the same pulse patterns to get comparable results for different scenarios: modifying the test PCB according to Fig. 6 without any DC-bus snubber network close to the power MOSFETs at the switching cell; same placement of the main DC-bus capacitors, but snubber networks have been added close to the power MOSFETs. The results which show the impact of those modifications are shown in Fig. 10. In addition a second scenario has been investigated which considers that the main DC-bus capacitors have to be rearranged, resulting in a distributed placement of them on the top side of the PCB as shown in Fig. 5. For this case three further modifications have been considered: the snubbers stay in place; the snubbers will be removed; the snubbers are replaced by two main DC-bus capacitors. Mechanical details are represented in Fig. 13 whereas Fig. 11 shows the corresponding measurement results. In general, we have considered different switching conditions in the different tests, namely zero current switching, hard commutation and zero voltage switching.

A commercial inductor (Würth Elektronik 7443763540068) with 6.8 µH was connected between the switching node and the negative DC-bus. Probing positions are shown in Fig. 7.

The sequence of pulses was designed in order to have roughly 40 A flowing into the inductor, while a hard commutation is performed.

The results of the first test setup are reported in Figs. 10abc and refer to the concentrated (and therefore non-ideal) placement of DC-bus capacitors and no snubber network case. While for zero current switching no significant overshoot can be identified, the voltage overshoot during hard switching results in a large overshoot of about 21.2 V both at the switching node (red trace), and on the DC-bus voltage u_{HB} (blue trace). This can be explained as, for zero current switching only C_{oss} of the power MOSFETs has to be charged, whereas the reverse recovery charge during hard commutation makes a significant difference in the switching transition. The voltage across main DC-bus capacitors C_B is only slightly affected, therefore the voltage drop has to occur on the longitudinal inductances L_{CB}, L_{PCB1} and L_{PCB2}, resulting in stored energy, which will get transferred to the output capacitance C_{LS} of the low-side MOSFET, causing the peak overshoot in voltage and resonance at about 91.7 MHz. This resonance can be seen during zero voltage switching too, which is illustrated in Fig. 10c. Obviously, the magnitude of the peak DC-bus voltage overshoot is significantly smaller, because the longitudinal inductance only has to conduct the current being switched, thus the stored energy is less. The resonance frequency measured with the transient method is slightly smaller than the predicted one (100 MHz) according to Fig. 3 (blue), which is a result of neglecting the package inductance of about 200 pH per device and L_{PCB2}.

By adding the paralleled DC-bus snubbers, the longitudinal commutation loop inductance will not only be reduced, but an additional resistive characteristic will be introduced, thus allowing an effective damping of any resonance and pushing the resonance frequency upwards. The impact of this measure is shown in Figs. 10def for the DC-bus and switching node voltage. Figs. 10ghi show the current through the snubber network at probing position 1 and 2 according to Fig. 7.

As expected from the DC-bus impedance simulations, the resonance frequency at 100 MHz which was measured with 91.7 MHz is pushed upwards to 181 MHz, which was barely modeled in the simulation and impossible to be validated with a 120 MHz impedance analyzer, like the one adopted in the

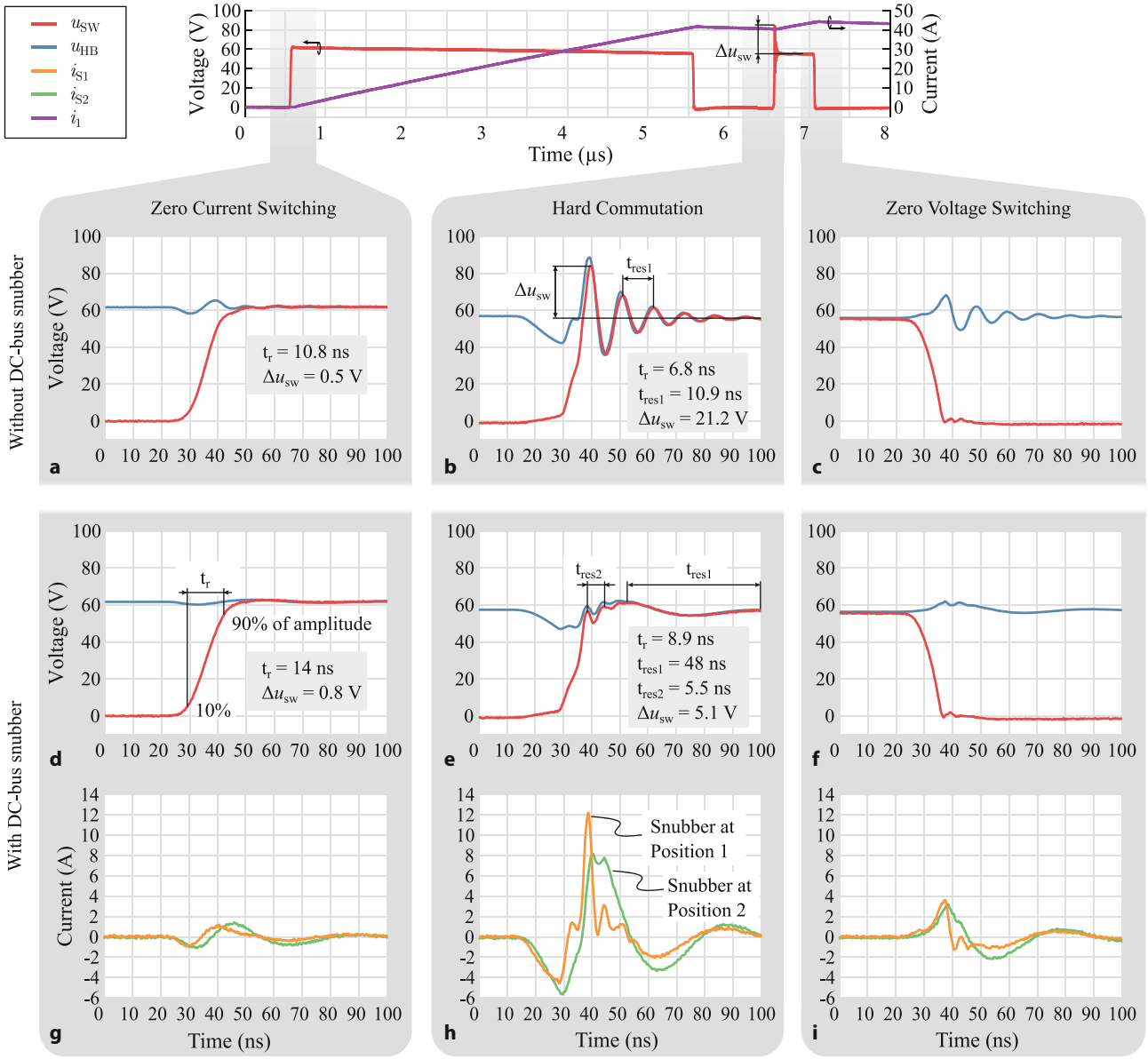

Fig. 10 Results of the double pulse test, showing the different voltage and current waveforms for zero current switching, hard commutation and zero voltage switching while the DC-bus capacitors are placed **non-ideal** according to Fig. 6. **a–c** show the behaviour **without** DC-bus snubber. **d–i** show the performance **with** snubber.

experiments. The anti-resonance point which is expected to be at about 19.5 MHz, was measured at 20.5 MHz, which is slightly above. More important is the overshoot of the switching node voltage. This has decreased from 21.2 V down to 5.1 V, being a major improvement considering a 60 V DC-bus voltage. But still, the expected aperiodic recharging behaviour of the DC-bus snubber capacitors could not be perfectly achieved, which results from imperfect modeling especially of the PCB power and ground planes. This will also explain why the current i_S (according to Fig. 1) through the snubber 2 (away from the power MOSFETs) is lagging in time due to additional inductance compared to the current through the snubber 1 (very close to the MOSFETs). Comparing zero voltage switching results (Fig. 10c to Fig. 10f) the benefits of using DC-bus snubber networks are clearly visible too. The peak overshoot as well as the ringing will be damped.

While the first setup takes a non-ideal placement of the main DC-bus capacitors C_B into account, the second test setup considers a distributed placement of the main DC-bus capacitors according to Fig. 5. Fig. 11 shows the corresponding transient measurements with respect to three additional modifications which are illustrated in Fig. 13. First the snubbers are still in place supporting the stabilization of the DC-bus at the switching cell. As expected, this configuration result in a low amount of total commutation loop inductance, therefore voltage overshoots

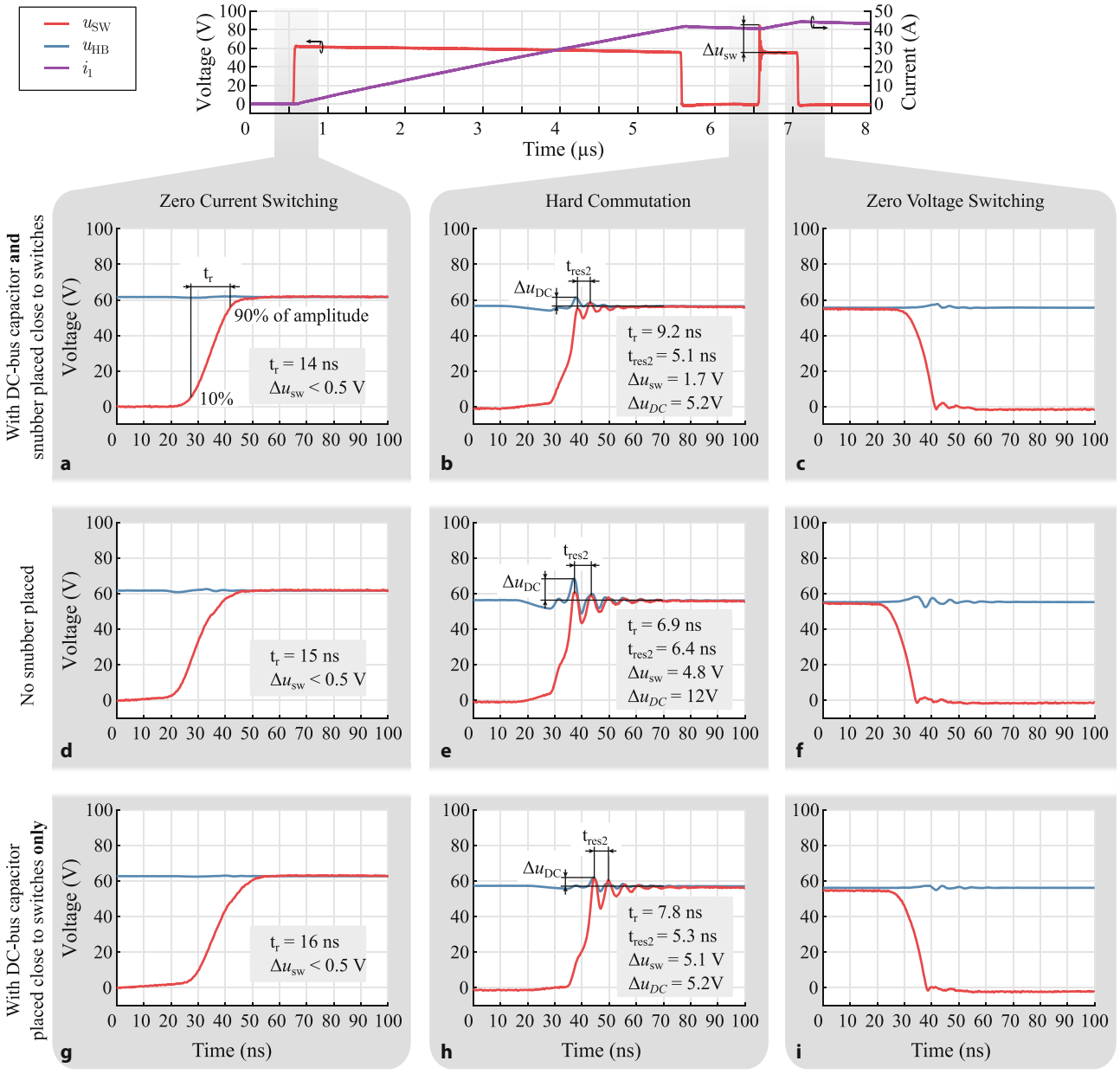

Fig. 11 Double pulse test results, showing the different voltage and current waveforms for zero current switching, hard commutation and zero voltage switching while the DC-bus capacitors are placed **very distributed** on the surface above the switching cell according to Fig. 5. **a–c** show the behaviour **with** DC-bus snubber according to Fig. 13a. **d–f** shows the performance **without** the snubbers according to Fig. 5b. **g–i** show the measurement results in case main DC-bus capacitors are used instead of the snubbers on the bottom side according to Fig. 5c

are minimized to only 1.7V, and the ringing is well damped while the frequency at which it occurs is 196MHz. Figs. 11abc show these results while Fig. 5a represents the mechanical setup. For the second test, the DC-bus snubbers were removed to see the impact of the snubbers, while having the main DC-bus capacitors placed very distributed on top of the PCB, like shown in Fig. 13b. Eliminating the snubbers will have the consequence that the commutation path goes through the PCB only, with the consequence that the commutation loop inductance slightly increases. Fig. 13b also gives insights into the PCB layer stackup indicating the DC+ layers in red, DC– in blue and the switch node in orange. Figs. 11def represent the according measurements and indicates that not only the ringing frequency decreases form 196MHz to 156MHz, also the DC-bus voltage measured at the switching cell increases from 5.2V to 12V. The third alternative is the very close placement of the main DC-bus capacitors on the same side where the switches are placed. While this setup is very common for bottom side cooled semiconductors, it adds additional mechanical constrains in case top side cooled devices are used. The height constrain of each component

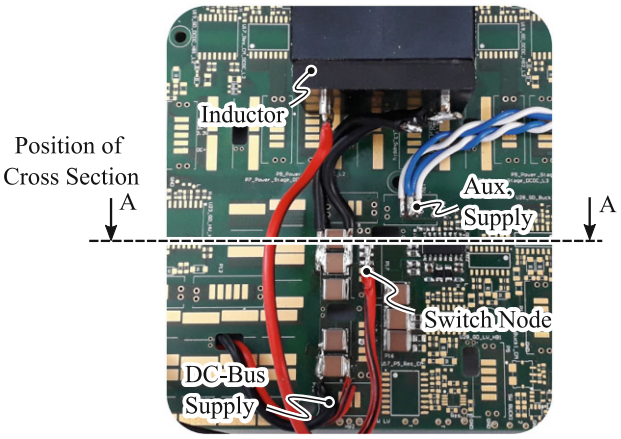

Fig. 12 Measurement setup for the double pulse tests. Note the position and direction of the cross section. A detailed view is shown in Fig. 13

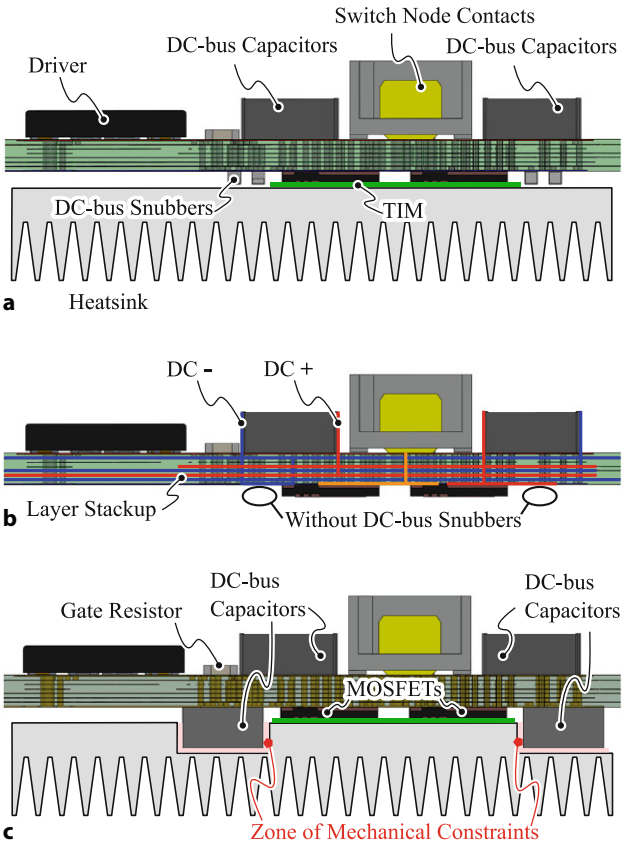

Fig. 13 Cross section through the PCB showing different options for capacitor placement. **a** with DC-bus snubbers. **b** without DC-bus snubbers. **c** Placement of the main DC-bus capacitors near the switches instead of the snubber network. Note the mechanical restrictions with the heatsink when placing DC-bus capacitors on the bottom side near the switches because of different component height. In addition **b** shows the layer stackup indicating the massive interleaving of the power and ground planes (*blue and red*) as well as the routing of the switch node signal (*orange*)

has to be considered. Especially when the power semiconductors have a smaller height compared to the main DC-bus capacitors, special measures must be taken into account. Therefore Fig. 13c represents one solution. Hence, the difference in height cannot be compensated with a thicker Thermal Interface Material (TIM), the heatsink has to be milled where the capacitors are placed. This does not only impact the thermal heat dissipation properties, it adds additional mechanical constraints e.g. positioning. From an electrical performance point of view, the voltage overshoot during hard commutation is similar compared to the setup with snubbers. Details are shown in Figs. 11ghi. Comparing the results for the shown modifications, clearly the overshoot can be significantly reduced when implementing DC-bus snubbers near by the switching transistors. Due to the small size of those components they can easily be mounted and no additional mechanical measures are needed.

4 Conclusion

This paper presents the experimental validation of the advantages using DC-bus snubbers in low-voltage silicon power MOSFET based switching applications. The beneficial effects in adopting a DC-bus snubber network on the switching behavior has been demonstrated, especially when the DC-bus capacitors have significant amount of parasitic inductance or cannot be placed very close to the switch node. Based on frequency characterization of possible actual candidate components, a simulation of the DC-bus impedance has been performed in order to estimate the switching behaviour considering a non-ideal placement of the main DC-bus capacitors. The impact of the implementation of the snubber networks has been verified by an in-field measurement of the impedance. Time domain transient double pulse tests show a significant reduction in the voltage overshoot at the switching node. It is shown that a reduction of the peak voltage overshoot from 21.2V to 5.1V and even down to 1.7V is possible considering optimal placement of the snubber networks and the DC-bus capacitors. A better utilization and safety margin of the low-voltage silicon power MOSFETs voltage capabilities is therefore possible.

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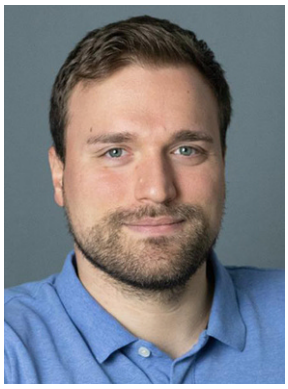

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