Fast and simple model generation for superjunction power MOSFETs

An easy way to get accurate SPICE models even without precise information from the data sheet

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This paper describes a new way to create a behavioral model for power MOSFETs with highly nonlinear parasitic capacitances like those based on superjunction (SJ) principles. The process ranges from a simple measurement to the final model for SPICE simulations. One of the benefits of the proposed modeling technique is that it does not require any information about the voltage-dependent capacitances of the MOSFET from the data sheet but instead relies on a simple measurement method using a vector network analyzer. The measurement data can be used for modeling all parasitic capacitances and inductances in the SPICE model. Compared to existing simulation models by the manufacturer, the proposed model promises better convergence, more accurate high-frequency behavior and faster simulation time. The advantages and disadvantages of this modeling technique are discussed.

Keywords: superjunction; power MOSFET; SPICE; modeling; power electronics

Schnelle und einfache Modellgenerierung für Superjunction Leistungs-MOSFETs

Ein einfacher Weg zu genauen SPICE-Modellen auch ohne genaue Informationen aus dem Datenblatt.

Diese Arbeit beschreibt einen neuen Weg zur Erstellung eines Verhaltensmodells für Leistungs-MOSFETs mit hochgradig nichtlinearen parasitären Kapazitäten, wie jene basierend auf dem Superjunction-Prinzip. Der beschriebene Prozess reicht von einer einfachen Messung bis hin zum fertigen Modell für SPICE-Simulationen. Einer der Vorteile der vorgeschlagenen Modellierungstechnik besteht darin, dass keine Informationen über die spannungsabhängigen Kapazitäten des MOSFET aus dem Datenblatt benötigt werden, sondern stattdessen auf eine einfache Messmethode mit einem Vektornetzwerkanalysator zurückgegriffen werden kann. Die gewonnenen Messdaten können für die Modellierung aller parasitären Kapazitäten und Induktivitäten im SPICE-Modell verwendet werden. Im Vergleich zu bestehenden Simulationsmodellen des Herstellers verspricht das vorgestellte Modell eine bessere Konvergenz, ein besseres Hochfrequenzverhalten und eine schnellere Simulationszeit. Die Vor- und Nachteile dieser Modellierungstechnik werden diskutiert.

Schlüsselwörter: Superjunction MOSFET; Leistungs-MOSFET; SPICE; Simulation; Modellierung; Leistungselektronik

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1. Introduction

Today, modern switched power electronic systems can be found in a variety of applications such as AC adapters, solar inverters, battery chargers, variable frequency motor drives, etc. They include modern power semiconductor switches which are increasingly based on superjunction techniques, silicon carbide (SiC) or gallium nitride (GaN) semiconductors. In simulations, it is becoming increasingly important to better represent the high-frequency behavior of MOSFETs. This makes it possible, for example, to take a closer look at control problems caused by strong load changes or to simulate the conducted electromagnetic emissions of an electronic system. In [1] it is described that one of the main challenges for accurate electromagnetic emission simulations is that the generated noise in a power electronic system is highly dependent on the circuit and semiconductor parasitics.

For accurate SPICE simulations in power electronics, accurate models of power MOSFETs are therefore essential. In many cases, manufacturers do not provide such models at all, or not for common SPICE simulators like LTspice. Manufacturer models are also mostly analytical models which are based on precise physical knowledge of

the internal structure, like shown in [2]. To generate such models without this knowledge, so-called behavioral models are commonly used [3–5].

This paper shows how behavioral models for SPICE simulation can be created using a simple measurement with a vector network analyzer (VNA). A special focus is put on modeling the voltage-dependent parasitic capacitances¹ of superjunction (SJ) MOSFETs since they are highly nonlinear and therefore difficult to imposi-

¹Whether the nonlinear capacitances of a MOSFET are regarded as “parasitic” or not lies, of course, in the eye of the observer. They are always part of a MOSFET but, similar to the body diode, often unwanted. Since their strong nonlinearity causes unwanted problems in the application shown in this paper, they are referred to as “parasitic” in the following.

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ble to model with somewhat not too complex mathematical equations. While accurate modeling of these nonlinearities is important for the accuracy of the models [6], it often leads to long simulation times and frequent convergence problems. This paper shows a way to generate fast and well converging models using an SJ MOSFET with very strong nonlinear parasitic capacitances. As gallium nitride (GaN) and silicon carbide (SiC) power transistors show less steep voltage dependent capacitances, we believe the model is also suited for those devices. The measurement procedure described in Sect. 2 also showed results for GaN and SiC devices that were consistent with the data sheet. For such models, however, the modeling of the output- and reverse-diode characteristic curve described in Sect. 3 must be revised. For example, GaN devices do not have an inherent body diode but are still capable of reverse conduction.

2. Measurements

As described in [7], all parasitic capacitances and inductances required for a behavioral model of a power MOSFET with three pins can be determined by a single S-parameter measurement using a VNA. The measuring system shown in Fig. 1, which is described in great detail in [8], additionally offers the possibility to measure these parasitic capacitances voltage dependent. The power MOSFET is depicted with all parasitics. These include the voltage-dependent parasitic capacitances C_{GD} , C_{GS} and C_{DS} as well as parasitic terminal inductances of the bonding wires L_G , L_D and L_S . The VNA is protected by two DC blocks from the high voltage source V_{DS} . The HF-filters prevent the measurement from being influenced by V_{DS} which is stepped over the first 100 V in 1 V steps. From the obtained voltage-dependent S-parameters, the parasitic inductances as well as the voltage-dependent capacitances can be calculated in one single step. The extraction of the capacitances from the S-parameter measurements can be done at any frequency below the resonant frequency; the extraction of the inductances at any frequency above the resonant frequency. Secondary effects such as temperature or frequency dependence of the parasitics were thoroughly tested and can be excluded. Likewise, no significant fabrication tolerances could be determined by measurements on various components although such tolerances are not ruled out. For this specific power MOSFET, the S-parameters were sampled at a frequency of 10 MHz to calculate the capacitances because the S-parameter measurement was most accurate over the whole drain-source voltage range there. In a similar way, as it is described in [7], the equations (2) and (3) show this calculation using the drain-source capacitance as an example. The parasitic inductances are sampled at 1 GHz and are calculated similarly. These values are constant and amount to $L_D = 0.2$ nH, $L_G = 3.5$ nH and $L_S = 1$ nH for the given model.

Figure 2 shows the result of the measurements of the voltage-dependent input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances in comparison with the data sheet up to a drain-source voltage of 100 V, above which the values do not change significantly anymore. These capacitances are defined in terms of the equivalent circuit capacitances as:

$$\begin{aligned} C_{iss} &= C_{GS} + C_{GD} \quad (\text{with } C_{DS} \text{ shorted}); \\ C_{rss} &= C_{GD}; \quad C_{oss} = C_{DS} + C_{GD} \end{aligned} \quad (1)$$

where C_{GS} is referred to the capacitance due to the overlap of the source and the channel regions by the polysilicon gate and is more or less independent of the applied drain source voltage (V_{DS}).

C_{GD} often consists of two parts. The first part of this capacitance is defined by the overlap of the gate (e.g. polysilicon) and the semiconductor material underneath in the drift region. The second part

Fig. 1. Measurement system for parasitic capacitances depending on the drain-source voltage V_{DS} and the parasitic inductances of a power MOSFET

Fig. 2. Comparison of the measured voltage-dependent capacitances C_{iss} , C_{oss} and C_{rss} with data sheet values

is associated with the depletion region under the gate. C_{GD} is a non-linear function of the drain-source voltage.

C_{DS} is the capacitance associated with the body diode and strongly depends on the drain-source voltage.

The difference in the measured values of the reverse transfer capacitance C_{rss} in Fig. 2 can be attributed to the insufficient measuring dynamics of the VNA used for the measurement. The measurement dynamics of a more modern VNA would be sufficient to measure this capacitance more accurately. However, as shown in Sect. 4, it turns out that these differences do not have a great influence on the resulting model. The small deviation of C_{rss} from the data sheet values at approx. 25 V was confirmed by several measurements of different components of the same type. Furthermore, a linear extrapolation seems to be sufficient for all capacitance values above

Fig. 3. Illustration of the MOSFET model for LTspice. The parasitic capacitances, as well as the behavior of the MOSFET and the body diode, are modeled with the help of voltage controlled current sources

100 V.

$$X_{CD} = \frac{2S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}} \cdot Z_0 \quad (2)$$

$$C_{DS} = \frac{2\pi f \cdot X_{CG}}{X_{CD}X_{CG} + X_{CD}X_{CS} + X_{CS}X_{CG}} \quad (3)$$

3. Model creation in LTspice

Almost the entire model can be represented by voltage controlled current sources which provide several advantages compared to the models that are usually provided by the IC manufacturers. The entire model is shown in Fig. 3. In the following, modeling of the individual components is described.

3.1 Modeling of voltage-dependent parasitic capacitances

For modeling the nonlinear, voltage-dependent capacitances, the capacity changes within the first 50 V are crucial since here especially the output capacity C_{oss} and the reverse capacity C_{rss} change by several orders of magnitude.

Looking at the measurement curves in Fig. 2 it becomes clear that a mathematical modeling of the capacity changes, like it is done in [3], becomes difficult to impossible in this case. Especially the nonlinearities around $V_{DS} = 25$ V, where the capacity values decrease by several decades, are very difficult to describe with sufficient accuracy by a function that interpolates the real curve. Doing so would most likely lead to sacrificing either simulation time or reliable convergence. For this reason, a table-based procedure based on the measurement results of Sect. 2 is presented.

The capacitances in Fig. 1 can be simulated in LTspice with the help of voltage controlled current sources. The values of the capacitances, which depend on V_{DS} , are passed to the simulator in form of a table which lists the corresponding capacitance in relation to V_{DS} . A voltage controlled current source models the behavior of the parasitic capacitance (C_{GS} , C_{GD} and C_{DS} in Fig. 3) using the following equation as an example for C_{DS} :

$$i_{DS} = C_{DS}(V_{DS}) \cdot \frac{dV_{DS}}{dt} \quad (4)$$

The values are read by a voltage controlled voltage source (V_{CGS} , V_{CGD} and V_{CDS} in Fig. 3) by using a classical look-up table whose interpolated output voltage is used in equation (4) for the values of $C_{DS}(V_{DS})$.

3.2 Modeling of output characteristic

The output characteristic $I_D = f(V_{DS}, V_{GS})$ of the MOSFET and the forward characteristic $I_F = f(V_{SD})$ of the body diode are modeled with voltage controlled current sources as well. The characteristic curves and the threshold voltage V_{TO} can usually be taken from the data sheet or can be measured alternatively. The threshold voltage V_{TO} , the on-resistance r_{DSon} and two drain current values I_{D1} and I_{D2} with their respective gate-source voltages V_{GS1} and V_{GS2} at a certain drain-source voltage are passed to the model.

In the linear region, the output characteristic follows the root function in equation (5). Within the saturation region, the drain current is calculated by equation (6). The unknown parameters c and r are derived in equations (7) and (8). Right now, the temperature dependency is not considered but will be added in a future work. In addition, it is not possible to investigate possible tolerances on the basis of the given characteristics of the data sheet.

$$I_D = \frac{\sqrt{V_{DS}}}{r_{DSon}} \quad (5)$$

$$I_D = c \cdot (V_{GS} - V_{TO})^r \quad (6)$$

$$c = \frac{I_{D1}}{(V_{GS1} - V_{TO})^r} \quad (7)$$

$$r = \frac{\ln(I_{D1}) - \ln(I_{D2})}{\ln(V_{GS1} - V_{TO}) - \ln(V_{GS2} - V_{TO})} \quad (8)$$

3.3 Modeling of breakdown voltage

Finally, the breakdown voltage is modeled by a simple parallel connection of a voltage source V_{BR} and a diode in series. Although this value has no meaning for normal operation, the breakdown behavior of the MOSFET was modeled according to the manufacturer's model and verified by simulation.

4. Model comparison

4.1 Half bridge test circuit

The described model is compared with two different complex models of the manufacturer (L0 and L3) by means of a simple test circuit. For this purpose, a half-bridge circuit, as seen in Fig. 4, is implemented as a step-up converter. The focus of the test setup was to test the MOSFET model for difficult convergence conditions while keeping the test setup as simple as possible. Therefore, a heavy load change was simulated. The load resistance R_L is switched from

Fig. 4. Test circuit for simulation in LTspice. The load resistance R_{Load} is changed from $10\ \Omega$ to $1\ \text{M}\Omega$ after a settling time of $0.5\ \text{ms}$. i_L is compared for different simulation models of the transistors M_1 and M_2

$10\ \Omega$ to $1\ \text{M}\Omega$ after a settling time of $0.5\ \text{ms}$. All passive components of the half-bridge are modeled by their ideal component values with additional parasitics ($V_{in} = 50\ \text{V}$; $L = 100\ \mu\text{H}$, $R_L = 50\ \text{m}\Omega$; $C_{in} = C_{out} = 1\ \mu\text{F}$, $ESR = 1\ \Omega$). The MOSFETs M_1 and M_2 are alternately clocked at $500\ \text{kHz}$ by an ideal voltage source with a rise- and falltime of $1\ \text{ns}$ with $1\ \text{ns}$ dead time.

4.2 Simulation constraints

To run a simulation in LTspice that includes the simulation models of the power MOSFET of the manufacturer, usually different parameters in the simulator must be used. These parameters are e.g. specified in application notes of the component manufacturer [9]. These parameter settings ensure that the simulation with the manufacturer models converges.

The following parameters are required to run a simulation with the manufacturer model:

$$\begin{aligned} gmin &= 1e-10; \quad abstol = 1e-10; \\ reltol &= 3e-3; \quad cshunt = 1e-15; \quad trtol = 5 \end{aligned}$$

In order to compare the simulations of the test circuit when using the new models described in Sect. 3, these parameters were used for all simulations with the L3 model, although the new model would only need a single parameter, namely $cshunt$. In all the presented cases in this paper, the “modified trap” method, recommended by the LTspice chief developer [10] and the application note of the manufacturer, was used as integration method. Nevertheless, simulations with other integration methods were also performed. The “gear” method shows comparable results for both models whereas the “trapezoidal” method leads to considerable convergence problems with the manufacturer model but not with the presented model.

4.3 Results

Figure 5 shows a comparison of the inductor current i_L when using different MOSFET models for M_1 and M_2 . The results with the proposed model are compared with those of two different complex manufacturer models. It can be clearly seen that the inductor current in the simulation with the proposed model corresponds approximately to that of the most complex manufacturer model (L3 model) in value. Deviations in the mean current i_L are probably the result of different modeling of the characteristic curves of the proposed and the L0 model. Especially during load changes, the manufacturer's model shows great overshoots of the current i_L which can only be attributed to calculation errors due to its shape. This was verified by several simulations with other load changes. The manufacturer's L3 model partly showed currents in the kA range which could not possibly correspond to realistic values. However, if the two models are compared under non-varying load, as shown in Fig. 6,

Fig. 5. Comparison of the simulation results via the inductor current i_L . Shown are two manufacturer models of different complexity (L0 and L3) and the proposed model

Fig. 6. Zoomed in inductor current i_L when the load is not changing. The most complex manufacturer model (L3 model) and the proposed model show similar behavior

they show similar behavior regarding the transient currents. The simulation time with the L3-model is about 3 to 4 times the duration with the presented model. The latter is similarly fast as the L0 model in almost all simulations.

The model proposed in this study only claims to offer a solution whose results correspond to the most complex manufacturer model with respect to its high-frequency behavior but with simpler methods and shorter simulation time which is successful. Which model delivers the more precise current, however, must be verified by measurements in a further work. Measurements of the actual switching behavior of the MOSFET are currently in progress. The comparison of the simulations with the manufacturer's existing model already shows promising results that speak for the presented modeling variant. However, this variant has the great advantage that due to the simple measurement method using a VNA and an automatable modeling process, neither a model provided by the manufacturer nor exact knowledge about the MOSFET itself is required.

5. Conclusion

This paper shows an approach to simulate behavioral models of power MOSFETs with very strong nonlinear parasitic capacitances, particularly superjunction power MOSFETs. In combination with a simple measurement setup using a VNA, this new modeling method is possible without detailed knowledge of the internal structure of

the MOSFET and its parasitics. With the obtained measurement results from the VNA, the nonlinear capacitances can be easily transferred into the SPICE model which makes it possible to automate the modeling process. By comparison with the manufacturer's simulation model, it was shown that the approach of modeling with voltage controlled current sources shows promising results. As has been shown, certain manufacturer models only work in a narrow range with regard to the set simulation parameters. The proposed model tends to give better convergence in less simulation time and fewer simulation errors without requiring special settings in SPICE. Further performance tests regarding simulation time and convergence in more complex circuits are planned.

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