

Comparison of EMI effects on different current mirror structures using a post-processing framework

D. Zupan, B. Deutschmann

In this paper the use of a simulation framework for comparing the effects of electromagnetic interference (EMI) on different current mirror structures is demonstrated. This is done with the help of an existing tool that is extended by specific, newly developed Python® scripts. The Cadence Design System and Spectre are used as simulation environment. The resulting outputs obtained by DC and transient simulations serve as an input for the next post-processing steps. The investigated current mirror topologies are well-described in literature and are already analyzed with respect to their EMI robustness. This paper focuses on simplifying the comparison of these structures and reducing the need of mathematical derivations. The script results are displayed directly in the schematic by using a heatmap and annotations for voltage nodes and current terminals. Mainly, two analyses are performed, whereas one part deals with EMI-induced DC offset shifts and the other part deals with the propagation of disturbance frequencies to the output current. Finally, the analytic results are compared with the graphical ones in order to check the feasibility of using the presented framework and the newly developed scripts and procedures.

Keywords: electromagnetic interference EMI; current mirror; integrated circuit; Cadence Design Framework; EMI analysis; direct power injection DPI

Vergleich von EMI-Effekten bei verschiedenen Stromspiegelstrukturen durch Verwendung eines Post-Processing Frameworks.

In dieser Arbeit wird die Verwendung eines Simulationsframeworks zur Gegenüberstellung von elektromagnetischen Interferenzeffekten auf unterschiedliche Stromspiegelstrukturen demonstriert. Dies wird mithilfe eines bereits vorhandenen Tools, welches um spezifische, neu entwickelte Python-Skripte erweitert wird, realisiert. Als Simulationsumgebung werden hierfür das Cadence Design System und Spectre verwendet. Die dabei entstehenden Resultate von DC und transienter Analyse dienen als Input für die weiteren Verarbeitungsschritte. Die untersuchten Stromspiegeltopologien sind bereits gut erforscht und auch hinsichtlich ihrer Robustheit betreffend EMI in der Literatur beschrieben. Diese Arbeit konzentriert sich auf die Vereinfachung des Vergleichs der unterschiedlichen Topologien und soll die Notwendigkeit mathematischer Herleitungen reduzieren. Die Ergebnisse der Skripte werden direkt in der Schaltung durch Verwendung von Farbverläufen sowie durch Anmerkungen für Spannungsknoten und Stromein-/Stromausgänge dargestellt. Hauptsächlich werden zwei Analysen durchgeführt, wobei einerseits ein EMI-induziertes Verschieben des DC-Offsets und andererseits die Ausbreitung von Störfrequenzen zum Stromausgang hin untersucht werden. Schließlich werden die analytischen Resultate mit den grafischen verglichen, um die Anwendbarkeit des präsentierten Frameworks und der neu entwickelten Skripte und Prozeduren zu überprüfen.

Schlüsselwörter: elektromagnetische Interferenz; Stromspiegel; integrierte Schaltungen; Cadence Design Framework; EMI-Analyse; direct power injection DPI

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1. Introduction

Immunity to electromagnetic interference (EMI) is becoming increasingly important in modern integrated circuit (IC) designs. Interferences and disturbances can be coupled into electronic circuits in various ways, either conducted or radiated [1, pp. 6-10]. Numerous effects can occur on these circuits due to electromagnetic (EM) disturbances. This can be a shift of direct current (DC) operating point (OP) [2], an unwanted high-frequency disturbance signal spreading and demodulating in the circuit [3], rectification of amplitude modulated radio frequency (RF) signals, charge pumping and many more.

A lot of literature is already available on the influence of EM disturbances on ICs [4], [5]. However, the presented approaches to investigate such effects on the functionality of ICs are mostly analytical

and quite time consuming, requiring a lot of simulation time and further redesign work. Especially the effectiveness of certain anti EMI measures is tedious to compare among different circuit topologies. Therefore it is reasonable to use a simulation framework, that can simplify these comparisons. Such a post-processing tool, that can be utilised, was already presented in [6]. It is written in Python programming language and integrated into the Cadence Design System (CDS). It enables the development of user defined post-processing scripts, to analyse the interference effects on ICs.

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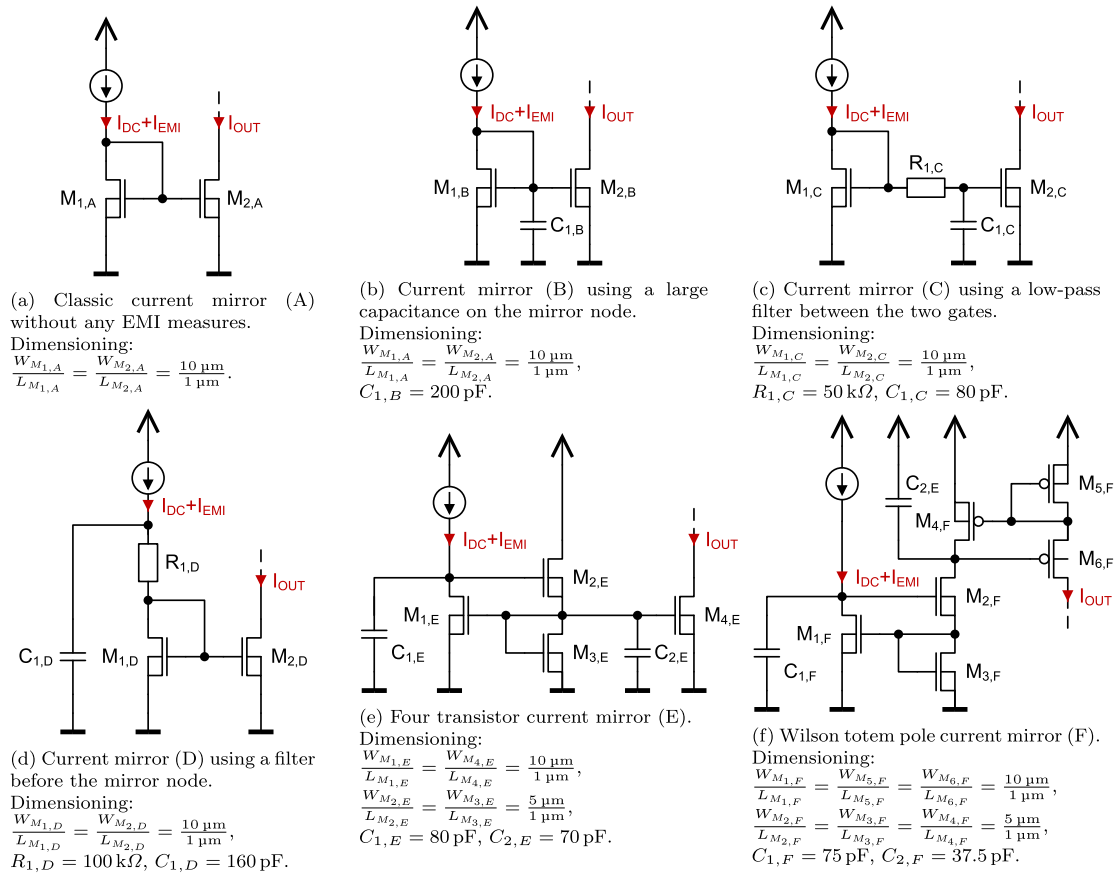


Fig. 1. Investigated current mirrors, identified by letters A to F, including dimensioning taken from [7]

In the following the mentioned tool will be used to investigate the immunity of different current mirror structures to EMI. Such basic circuit blocks are already well described in [7]. The results obtained by the framework should be displayed in the schematic by using heatmap colouring and annotations, giving a graphical overview on the EMI robustness. Therefore, the main goal of this paper is to present, develop and test scripts, that should ease and simplify selecting the best circuit in terms of EMI.

This article is organised as follows: Sect. 2 describes six different current mirror circuits, that will be examined in the course of this article. In Sect. 3 the post-processing tool, including the development of the used scripts are presented, followed by the interpretation of the obtained results. Finally conclusions on the applicability of the shown concepts are drawn.

2. Current mirror concepts

In this section a summary on the investigated current mirror structures is given. The focus lies on the concepts that are explained in detail in [7, Case Study 3, pp. 52-72], implemented in a standard CMOS 0.35 μm technology. Additionally the main properties, advantages and disadvantages are highlighted briefly.

The six current mirror circuits under investigation are depicted in Fig. 1, whereas the dimensioning is taken from [7]. This includes width W and length L of every transistor, as well as resistor and capacitor values. First a simple two-transistor current mirror is investigated as shown in Fig. 1a. A current of $I_N = 10 \mu\text{A}$ should be mirrored with a ratio of 1 : 1. In addition to the DC current I_{DC} a disturbance signal in form of a sinusoidal interference current I_{EMI} is superimposed, as described by equation (1). A modulation index

m is introduced as the ratio of the EMI amplitude to the DC current (see equation (2)). Obviously the first simple circuit is not suited for applications, where EMI plays a critical role, as the disturbance signal is mirrored to the output of the current mirror.

$$I_N = I_{DC} + I_{EMI} = I_{DC} + \hat{I}_{EMI} \cdot \sin(\omega t) \quad (1)$$

$$m = \frac{\hat{I}_{EMI}}{I_{DC}} \quad (2)$$

As a next step, a capacitor can be added to the gates of the two transistors of the current mirror as shown in Fig. 1b to reduce the EMI effects. However the disadvantage lies in the large capacitance that is needed, which is not reasonably integrateable. Extending this current mirror with a resistor gives a low-pass filter from the first to the second gate node as shown in Fig. 1c. This topology can of course reduce the influence of high frequency disturbances, however it leads to a shift in DC voltage on the second gate node, which is not desirable. Another possibility is trying to filter the disturbance already before reaching the diode-connected transistor as shown in Fig. 1d [8]. However, the required supply voltage needs to be increased due to the resistor.

Finally, two other EMI resisting current mirrors, using more than two transistors, are presented in [7]. One is shown in Fig. 1e, the purpose of the two additional transistors M_2 and M_3 is to keep the gate source voltage of M_1 and M_4 at a constant DC voltage, which is done by negative feedback. Furthermore the impedance of the mirror node is kept low [7, pp. 61-67]. The other circuit is a Wilson totem pole current mirror and shown in Fig. 1f. It can help decreas-

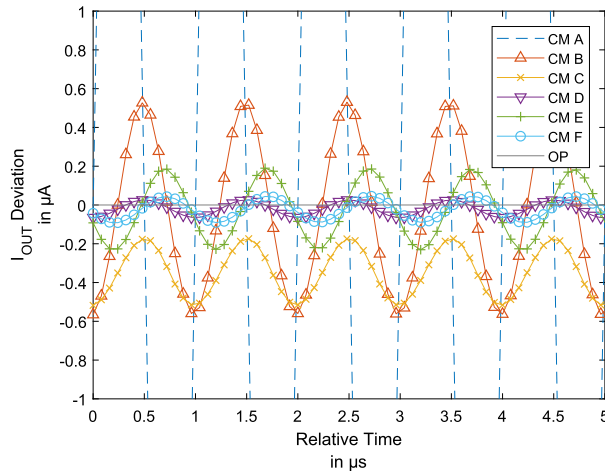


Fig. 2. Output current deviation from the OP for current mirrors A to F for same EMI input current (Amplitude 5µA, EMI Frequency 1MHz)

ing the total area by decreasing the total capacitance needed [7, pp. 67-69], [9].

The authors in [7] mainly focus on two parts, in their analyses:

- One is an EMI induced DC shift. Obviously this should be prevented, as a shift in DC voltage or current cannot be simply filtered, but countermeasures with more complex circuitry (control) have to be applied [7, pp. 40-43], [2].
- The other is the propagation of the disturbance frequency to the mirror node and to the output current, ultimately.

A comparison in time domain, highlighting the DC shift with respect to the OP analysis is given in Fig. 2, whereas five periods of the output current of the EMI disturbed circuits are plotted after settling. In terms of DC shift all circuits, except current mirror C, perform equally well, having nearly no deviation in DC offset under the influence of EMI. This is valid for modulation indices $m < 1$, i.e. when the EMI signal amplitude is smaller than the input DC current [7, p. 70, Table 3.3]. Furthermore it is visible that the amplitude of the output current is highest for current mirror A. As of representation reasons its output current is partly truncated in Fig. 2.

In [7] all circuits are designed to have an attenuation of about 40 dB at a frequency of 1 MHz, which is the lower frequency corner for performing direct power injection (DPI) tests [10]. However, for this exemplary analysis the frequency responses are slightly modified to demonstrate the qualitative estimations obtained from EMI frequency propagation analysis. The analytically derived and calculated frequency responses from input to output current are summarised graphically in Fig. 3. It is visible, that the frequency response of the transfer functions $H_x(s) = \frac{I_{OUT}(s)}{I_{IN}(s)}$ is varying at 1 MHz. Additionally, the frequency responses for circuits E and F are steeper (more poles) and have a higher corner frequency (smaller capacitance values). From a quick glance it can be said, that current mirror D performs best in terms of frequency attenuation at 1 MHz, followed by F, C, E, B and finally A.

Evidently these analytical approaches are very convenient in terms of comparing different structures. However, the derivations might become quite complex and tedious to solve, even for small circuits. Therefore, it is desirable to make use of a tool, that can help to classify the circuits in terms of their EMI robustness. This framework is presented in the next section.

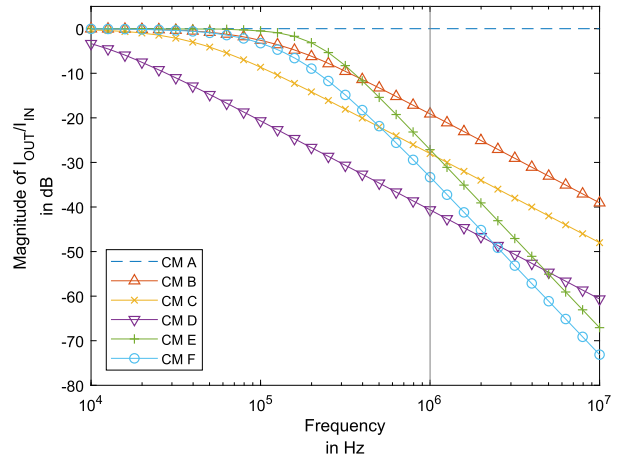


Fig. 3. Frequency response of transfer functions for current mirrors A to F

3. Application of post-processing tool for EMI robustness investigation

This section utilises the post-processing framework presented in [6]. The basic idea of such a tool is to help identify circuit blocks and voltage or current nodes, that are influenced by an electromagnetic interference.

The main processing part is done by user defined Python scripts, that need to be developed according to the designer's needs. These scripts classify specific voltage nodes and current terminals from best to worst. In this case, these will focus on the DC shift and frequency propagation as described previously. The classification is done by means of a heatmap, introducing a rating, where red is defined as worst, going via yellow and green, to blue meaning best, i.e. least influenced by EMI. The grading and therefore colouring is determined by the individual Python procedures. These can either be looking at absolute values, such as violations of specific limits that are defined in EM compatibility requirements or standards, or – like in this case – relative grading of the nodes and terminals from red being most susceptible to EMI and blue being least susceptible. Furthermore the grading can be set to be logarithmic or linear. For comparing the EMI immunity of the six presented current mirrors, the results are annotated in the schematic, with their respective heatmap grading.

For each of the two analyses – DC shift and frequency propagation – the script principles, as well as the results are shown, described and compared with the summary from Sect. 2. For the following simulations an exemplary EMI frequency of $f_{EMI} = 1$ MHz and a modulation factor of $m = 0.5$ are used, to demonstrate the applicability of the developed scripts.

3.1 DC shift analysis

First an EMI induced DC shift is investigated. In order to perform this analysis, two simulation results are needed, which are DC and transient. Obviously the DC result is used as undisturbed reference model. The transient result including the EMI disturbance is utilised for the detection of OP deviations. The script, that was developed, functions in the following way:

- The transient results are low-pass filtered by using a moving average filter, with a filter window being an integer multiple of the EMI period.
- The obtained averaged voltage and current values, are compared to the reference values of the undisturbed DC simulation, by calculating the absolute difference.

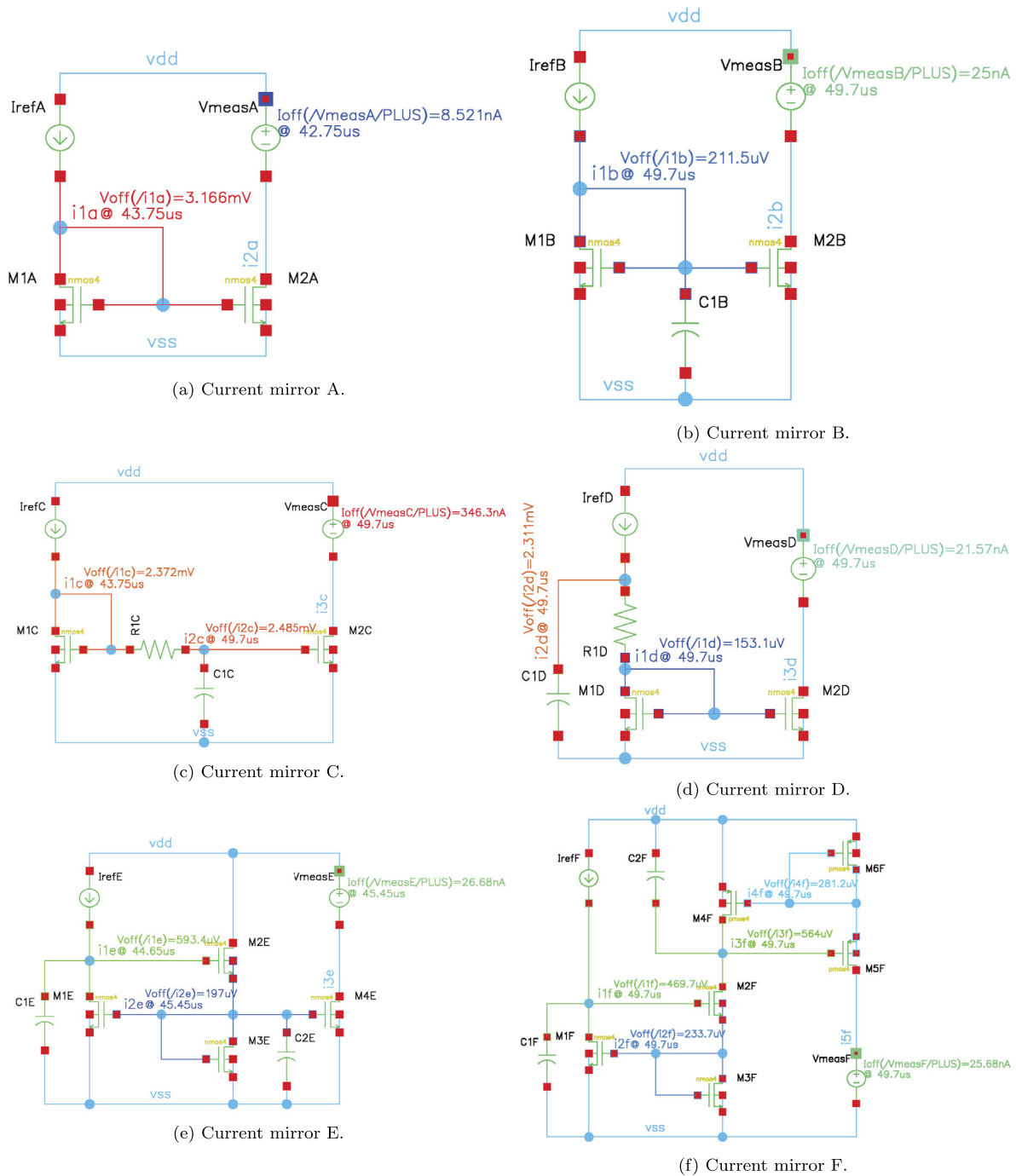


Fig. 4. DC shift analysis results for current mirrors A to F, annotated in Virtuoso Schematic Editor

- These differences are finally ordered by magnitude, the highest deviation being worst and lowest deviation being best.

The results of this analysis for all six circuits are annotated into Cadence Schematic Editor and are shown in Fig. 4 and summarised in Table 1. Looking at the output current, current mirror C is performing worst, what was also expected and what is shown in the red annotation on the terminal of V_{measC} in Fig. 4c. The output current deviation of circuit C is more than one magnitude higher compared to the other topologies. This can be seen graphically by the green and blue annotations and lower values on V_{measX} . However, due to the non-linear behaviour of diode connected transistors, also the

mirror node in circuit A is experiencing a very high deviation in terms of its OP (see voltage node $i1a$ highlighted and annotated in red in Fig. 4a), but this is cancelled out because of the symmetric topology, leading to a very small DC shift on the output current (see blue annotation on V_{measA}). For circuit B (see Fig. 4b) the large capacitor is attenuating most of the mirror node's DC shift, emphasised in blue for node $i1b$. Current mirrors D, E and F (Figs. 1d, 1e, 1f) show the opposite, that should be reached with the additional circuitry: For every voltage node, that is closer to the output, the DC shift is decreasing as the annotation colours go from orange, via yellow and green to blue, respectively the annotated values become smaller.

Table 1. Comparison of DC shift and EMI amplitude on the output current I_{OUT} for the six current mirrors

I_{OUT}	Current Mirror Circuit					
	A	B	C	D	E	F
DC shift of I_{OUT}	8.521 nA	25.00 nA	346.3 nA	21.57 nA	26.68 nA	25.68 nA
Amplitude of I_{OUT} at 1 MHz	4.973 μ A	526.9 nA	152.7 nA	26.29 nA	205.7 nA	68.18 nA

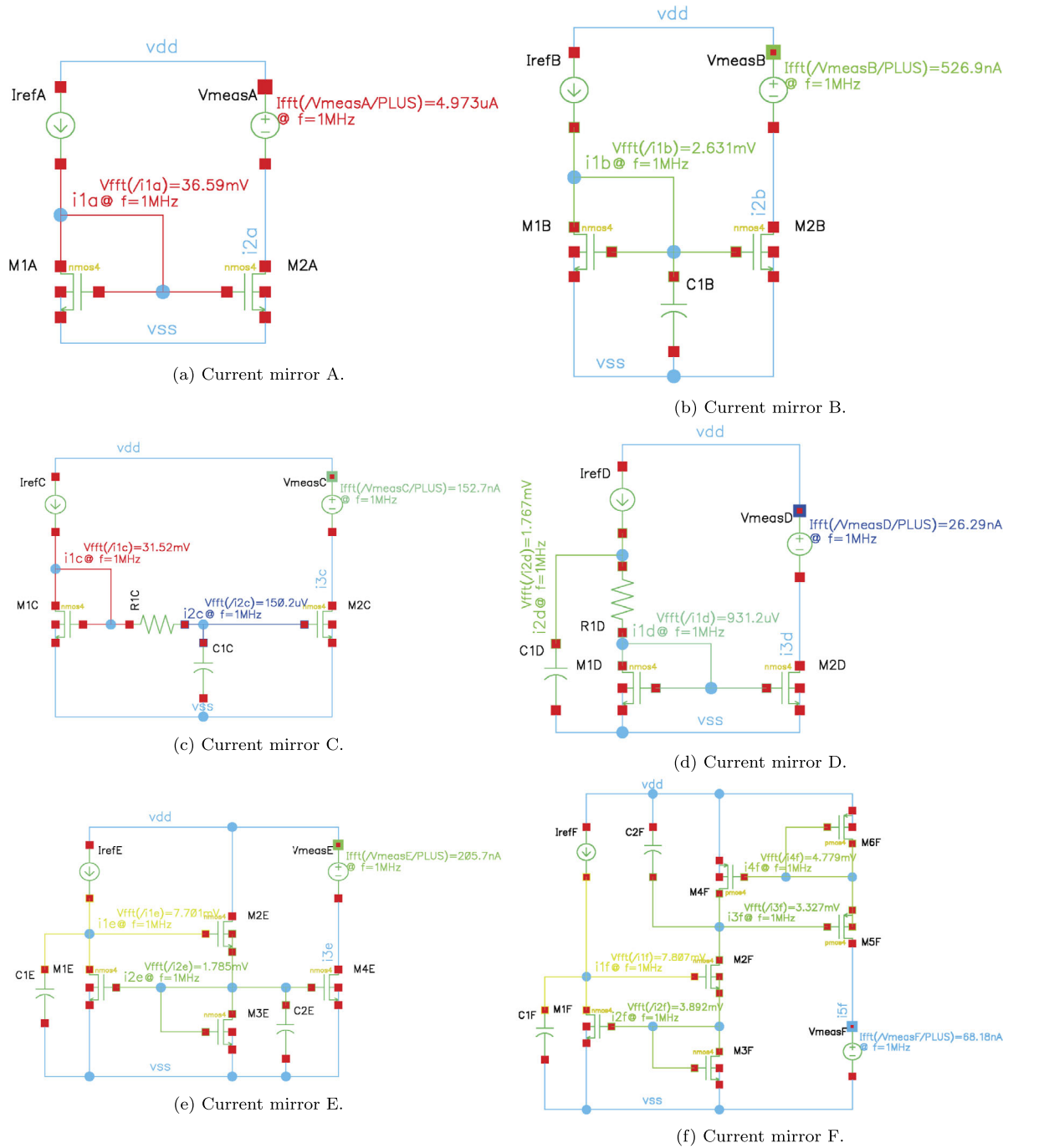


Fig. 5. Frequency propagation analysis results for current mirrors A to F for an EMI frequency of 1MHz, annotated in Virtuoso Schematic Editor

3.2 Frequency propagation

For investigating the frequency propagation, a second script is developed. However, this script only needs to be provided the transient results. It can be passed a frequency (range) of interest, that should be traced through the circuit. In this case the frequency of interest is set to the EMI frequency, in order to show the propagation of the disturbance within the circuit blocks. The procedure performs the following tasks:

- First a fast Fourier transform (FFT) is calculated from the saved voltages and currents.
- Afterwards the amplitudes in the desired frequency domain are summed up and
- finally ordered by magnitude again, from highest amplitude being worst and lowest being best.

The results are again annotated in Cadence Schematic Editor, comparing the six different current mirrors, with respect to EMI signal propagation. This is shown in Fig. 5. One can start with observing the disturbance frequency on the output currents. Obviously current mirror A performs worst with an amplitude of about 5 μA , i.e. the EMI current amplitude. Therefore the terminal of V_{measA} is marked with red in Fig. 5a. The same is shown in Fig. 2. Following the colours in terms of a heatmap (red-yellow-green-blue), we see that circuit D (see Fig. 5d) performs best, in comparison to all others. The annotated results are also summarised in Table 1. Ordering the circuits by the disturbance amplitude from D being best, via F, C, E, B, to A being worst, leads to the same results, that were also deduced from Fig. 3 in Sect. 2.

However, there are even many more things we can deduce from the heatmap and the annotations. To give a few examples:

- Adding a capacitor to the classic current mirror, already helps a lot in reducing the voltage amplitude on the gate of M_2 , when comparing Fig. 5a and Fig. 5b (see red vs. green highlighting on V_{measX} terminal and annotation).
- The low-pass filter is working as expected, reducing the voltage amplitude on the gate of M_2 (see nodes $i1c$ and $i2c$ in Fig. 5c).
- Using the transistors M_2 and M_3 in circuits E and F helps in shielding the following gates from high EMI currents (see voltage nodes in Fig. 5e and Fig. 5f).

3.3 Summary and future work

The demonstrated graphical approach simplifies the comparison of the different current mirrors significantly by reducing the need for analytical analyses. Most findings, that are described in [7], could be gathered from the annotated schematics. This can come in handy especially in more complex circuits, as problems could be addressed and solved at their source. Getting rid of DC offsets deeper in the circuitry often leads to higher efforts in terms of feedback loops or similar measures. Furthermore attenuating EMI frequencies as early as possible is a crucial point in preventing undesired demodulations in the circuit.

It has to be noted, that the circuits were examined for a single EMI frequency. This also means, that the annotated results primarily represented one specific EMI condition. Therefore, in future work the framework could be extended, in order to combine the results of more simulations with different EMI frequencies into a single annotated schematic.

4. Conclusion

In this article it was shown, that the conclusions on the EMI robustness of six investigated current mirror structures, that were drawn analytically, can also be deduced by using a simulation and post-processing approach. A tool, that is integrated into the Cadence Design System was used and extended by two scripts for DC shift and frequency propagation analysis. The results from these analyses were visually presented by voltage node and current terminal highlighting within the schematic in terms of heatmap colouring and annotation of values. The goal of simplifying the comparison of different topologies, without the need of time consuming derivations, was reached and using this framework proved to be useful.

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