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Integration solutions for reconfigurable multi-standard wireless transceivers

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This article presents an overview of modern integration concepts for receiver, transmitter and duplexer architectures. Based on innovative design techniques, a system-in-package integrated RF transceiver architecture is proposed as a low-cost low-power alternative to traditional multi-standard transceivers. The proposed transceiver architecture unites advantages of a sub-sampling receiver with tunable low noise amplifier (LNA), a high-efficiency digital power amplifier and an integrated duplexer with on-package passive components in order to fulfill the more and more stringent requirements for wireless systems. In addition to the transceiver architecture, measurement results of building blocks are presented. A LNA circuit implemented in 65 nm CMOS technology provides a continuously tunable-gain (3–23 dB) and a tunable frequency band (4.5 GHz–5.5 GHz) with noise figure of 2 dB and IIP_3 of −6.5 dBm at the highest gain. A high Q-factor, on-package transformer, implemented in a core-less 3-metal layer system-in-package substrate, presents a coupling factor of 0.6 and a Q-factor of approximately 30. This provides a low-cost, high-performance alternative solution to integrated matching networks and duplexers.

Keywords: RF transceivers; multi-standard; sub-sampling; integrated duplexer; tunable LNA

Integrationskonzepte für konfigurierbare Multi-Standard-Drahtlos-Transceiver.

Der folgende Artikel gibt einen Überblick über moderne Integrationskonzepte von Hochfrequenz-Transceivern, anhand von spezifischen Beispielen innovativer Empfänger, Sender und Duplexer-Architekturen. Das vorgestellte Konzept nutzt moderne System-in-Package-Technologien gemeinsam mit Chip-Integration als kostengünstige und energiesparende Alternative zu traditionellen Transceiver-Konzepten. Es vereint einen innovativen Sub-Sampling Receiver mit einem flexibel abstimmbaren Low-Noise Amplifier (LNA), einen effizienten digitalen Leistungsverstärker sowie einen passiven Duplexer, integriert in einer System-in-Package-Technologie. Ergänzend zur Transceiver-Architektur wird die Schaltungsrealisierung des LNA mit kontinuierlich verstellbarer Verstärkung von 3 dB bis 23 dB, einer verstellbaren Frequenz von 4.5 GHz bis 5.5 GHz, einer Noise Figure von 2 dB und einer IIP3-Linearität von −6.5 dBm bei höchster Verstärkung präsentiert. Weiters wird ein hochqualitativer Transformator vorgestellt, welcher durch Nutzung einer dreilagigen System-in-Package-Technologie realisiert wurde und einen Qualitätsfaktor von 30 sowie einen Kopplungsfaktor von 0.6 aufweist.

Schlüsselwörter: RF Transceiver; Multi-Standard; Sub-sampling; integrierter Duplexer; flexibler LNA

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1. Introduction

Modern wireless transceivers require multi-band and multi-standard operation, which leads to complex, bulky and power hungry implementations. An architecture for state-of-the-art multi-standard transceiver is shown in Fig. 1, where several transmitter (TX) and receiver (RX) chains are required in order to fulfill specifications for wireless standards.

With the evolution of wireless systems, even more communication standards are being proposed while maintaining backward compatibility, therefore, cost and complexity of RF transceivers tend to increase. For high-performance communication standards, external off-chip components with optimized performance such as duplexer filter and power amplifier (PA), are necessary to satisfy ever-growing standard requirements. On the contrary, for low-performance battery operated applications such as Internet of things (IoT), low-power and low-cost implementations are desired.

This article presents a set of innovative design concepts, for receivers, transmitters and system-in-package (SiP) integration, which provides reconfigurability, wide frequency operation, higher power efficiency and low-cost. Based on the presented concepts, an RF transceiver architecture shown in Fig. 2 is proposed. The RX chain is based on a tunable active-balun LNA and a sub-sampling down-conversion mixer with discrete-time signal processing (DTSP). The transmitter is realized as a high-efficiency digital power amplifier (DPA) working as RF-DAC. Finally, a SiP integration provides high-quality, low-cost passive components for matching network and duplexer implementation.

The whole transceiver architecture is thought to be designed in a single-chip, avoiding cost increase caused by a multi-chip solution.

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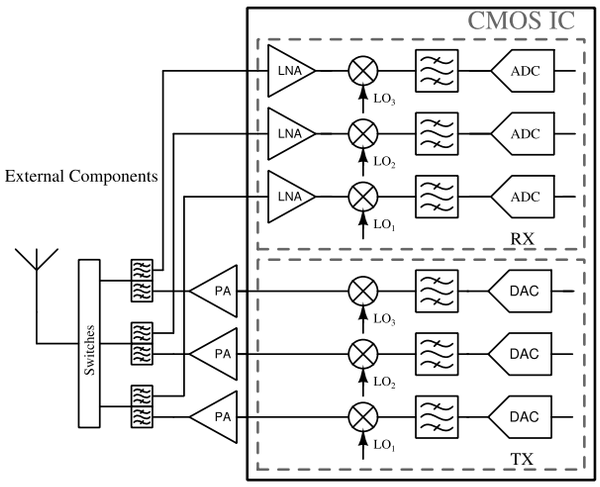

Fig. 1. Traditional multi-standard transceiver architecture with external passive components

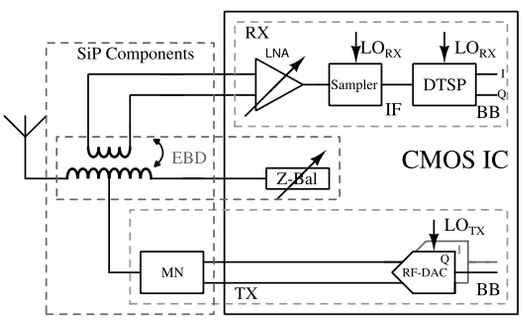

Fig. 2. Proposed transceiver with sub-sampling receiver, SiP integrated electric balance duplexer (EBD) and digital intensive transmitter

A tunable-band LNA relaxes the linearity requirements of wideband LNAs, and the programmable gain fulfills the sensitivity requirements of various wireless standards. Ideal software defined radio (SDR) concept relies on a analog-to-digital converter (ADC) to digitize the RF signal immediately after the antenna and transfer the complete signal processing to the digital domain [1]. For example, for a Nyquist ADC with 2 GHz RF input signal, a sampling frequency of 4 GSps is necessary with high enough resolution. These stringent specifications are currently not practical for battery operated low-power applications. The sampling receivers provide a step towards this goal by employing discrete-time signal processing with additional flexibility [4, 5, 11, 13]. Receiver implementations in [4, 13] focus on oversampling the RF signal to place the images above the center frequency. The tuned receiver in [11] samples the 2.4 GHz RF signal at a very low sampling frequency of 100 MHz resulting in very high noise figure of 21 dB due to noise folding. The implementation [5] utilize bandpass sampling theory to optimize the sampling frequency of 1.07 GHz for 2.4 GHz RF signal but lacks the front-end LNA. The proposed sub-sampling receiver architecture utilizes sub-sampling mixer followed DTSP after the front-end LNA. Use of sub-sampling leads to lower local oscillator frequency, less-complex frequency synthesizer and lower power consumption compared to traditional all analog receivers.

An RF-DAC unites in one block the functionality of a digital-to-analog converter (DAC), up-conversion and amplification stages. It has the advantage of higher efficiency when compared to traditional analog PAs and can be integrated in standard CMOS technology. An electric balance duplexer (EBD) can be fully integrated in a SiP and prevents the use of external costly duplexer. SiP transformers can be used in the matching network (MN) and Duplexer as an alternative to CMOS transformers. They reduce the production cost and additionally contribute to a more efficient RF-DAC and low loss duplexer structures.

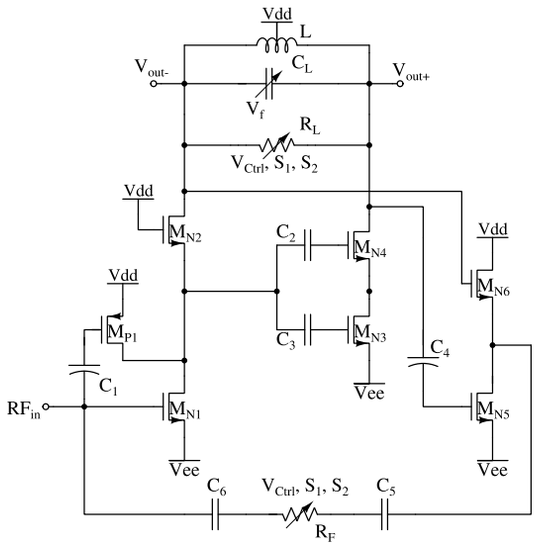

Fig. 3. Tunable-gain and tunable-band active balun LNA circuit diagram with buffered feedback [12]

The rest of article is organized as follows, in Sect. 2 a review about sub-sampling receivers will be presented with LNA implementation details. In Sect. 3 a review and analysis of a DPA will be presented. In Sect. 4 implementation and measurement results of on-package transformers for duplexer and MN will be shown. In Sect. 5 recently proposed solutions for integrated duplexers, its advantages and limitations will be discussed. Section 6 presents conclusions and final considerations of the proposed transceiver.

2. Sub-sampling receiver architecture

The sub-sampling receiver utilizes a tunable-gain and tunable-band active-balun common-source LNA followed by a sub-sampling mixer that down-converts the RF signal to IF and a DTSP block that down-converts the IF signal to baseband.

The LNA shown in Fig. 3, is based on the buffered resistive feedback topology with noise cancellation techniques as reported in [12]. The LNA closed loop gain is tuned by simultaneously varying the load resistor (R_L) and feedback resistor (R_F). R_L and R_F are implemented as active CMOS resistor (ACR) with 4 parallel slices as shown in Fig. 4. The ACR is controlled by an external analog signal V_{Ctrl} and two digital signals S_1 and S_2. The LC-tank provides a tunable bandpass characteristic from 4.5 GHz to 5.5 GHz using tunable MOS varactors. The inductor is a center-tapped coil with a simulated Q-factor of 13 which guarantees the output voltage balance.

The LNA architecture targeted for 5 GHz WLAN band is fabricated in a 65 nm CMOS technology with an active area of 0.043 mm^2. A continuous monotonous gain tuning from 3 dB to 23 dB is achieved for the LNA at 5.5 GHz as shown in Fig. 5a. The noise figure (NF) measurement is shown in Fig. 5b and it varies between 2 dB and 6 dB for different LNA gains. The third order inter-modulation product (IIP_3) is measured to be −6.5 dBm and +10 dBm at the highest and lowest gains respectively.

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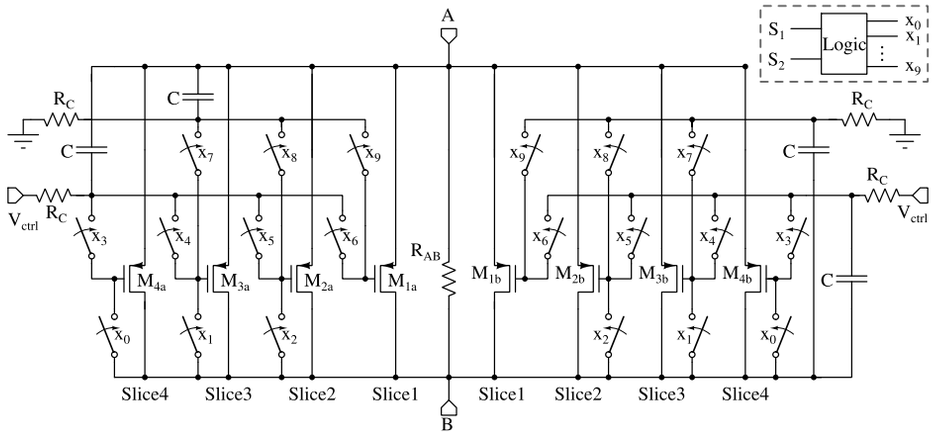

Fig. 4. Active MOS resistor circuit implementation of R_F and R_L [12]

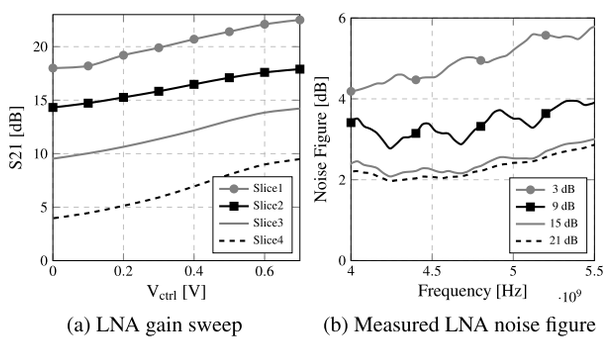

Fig. 5. Summary of measured results for tunable-gain and tunable-band LNA [12]

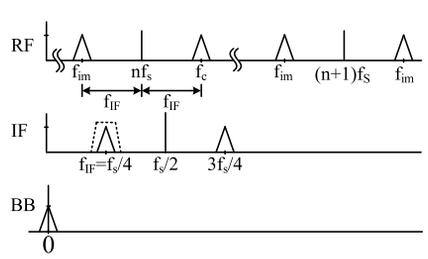

Fig. 6. Frequency spectrum for the sub-sampling receiver with discrete time signal processing [5]

Although the LNA implementation is targeted for 5 GHz WLAN band, the architecture can be modified for lower RF frequency, for example, 2 GHz with similar performance and area penalty of approximately 20%. The proposed receiver architecture utilizes sub-sampling based down-conversion mixer interfaced to the tunable LNA. The front-end LNA gain reduces the effect of sub-sampling mixer noise figure on the overall receiver noise figure. The LNA-mixer interface must be optimized for the analog tracking bandwidth and KT/C noise in the mixer.

The typical spectrum for the sub-sampled RF signal is shown in Fig. 6. Based on the bandpass sampling theory [14], the RF signal with center frequency f_c is sampled at sampling frequency of $f_s = \frac{4 \times f_c}{(2K-1)}$ and down-converted to an intermediate frequency (IF) $f_{IF} = \frac{f_s}{4}$, where K is an integer [5]. The nearest image (f_{im}) of this signal is present at the distance of $\frac{f_s}{2}$ as seen in Fig. 6. Selection of sampling frequency is an important parameter for the sampling receivers, based on the effect of noise folding, the lower sampling frequency results in higher noise figure and stringent filter requirement and higher sampling frequency results in easier filter design and lower noise figure, but more complex frequency synthesizer design [14]. If the selected sampling frequency is optimized, the image frequencies can be placed far enough to be filtered before the down-conversion either in the duplexer, in the selectivity of LNA or with a dedicated bandpass filter. Also, the front-end selectivity of the LNA reduces the effect of out-of-band noise on the overall mixer output noise. The second stage down-conversion utilizes discrete time signal processing or discrete time mixing to generate precise in-phase (I) and quadrature phase (Q) signals at the baseband (BB). This approach also has been studied for the wideband receivers in electronic warfare application [6]. The architecture provides a good enough flexibility, low-power design compared to traditional analog receivers.

3. Digital power amplifier based transmitter

A key component of a standard wireless transmitter is the PA. Among all the sub-blocks, PA is one of the most challenging blocks due to its requirements of high output power and high-efficiency. Therefore, in most of the cases, the PA is still not integrated into the transceiver chip (Fig. 1). Different semiconductor materials as GaAs and GaN are generally used for its realization, with the advantage of high-performance and drawback of higher production costs. On the other hand, standard CMOS technologies are more affordable than GaAs and GaN, but experience lower supply voltages, limiting the performance of integrated CMOS PAs.

Recently digital power amplifiers (DPAs) have been used as a fully integrated higher efficiency alternative for the conventional analog PAs. An example of DPA is the switched capacitor power amplifier (SCPA) as shown in Fig. 7a [15]. An *n*-bits SCPA consists of a set of 2^n unit capacitors C_u whose bottom plates are switched between *Vdd* and *gnd*, and top plates are connected in parallel. The number of switching slices corresponds to the number of *ON*-bits. The *OFF* slices are fixed to *gnd* or *Vdd*. The output voltage without a connected load (*Vo*) is a square wave proportional to the number of switching slices. The switching devices can be implemented as inverters as shown in Fig. 7b. The output impedance of the SCPA can be estimated by the parasitic resistance of the MOS devices R_{on}, the capacitance of C_u and the parasitic capacitances C_p as shown in

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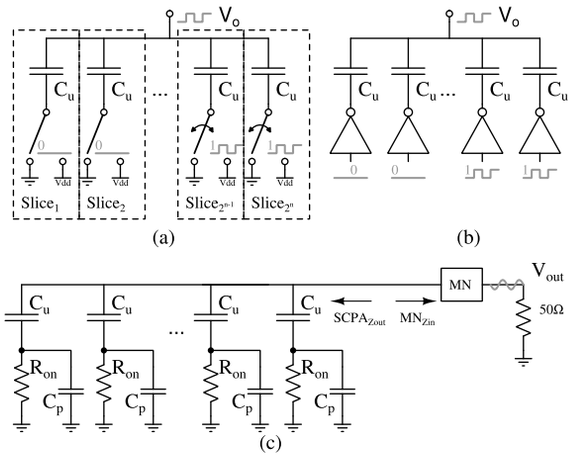

Fig. 7. Simplified model for switched capacitor power amplifier

Fig. 7c. One advantage of the proposed voltage mode SCPA in comparison to the current mode SCPAs [2] is that the output impedance $SCPA_{Zout}$ is independent of the number of ON and OFF slices and the MN does not need to be tuned.

The SCPA has an output swing limited by the voltage supply, which is very low in new CMOS technologies. Therefore, a load impedance well below 50 Ω is required to provide a high output power. An impedance matching network is added to the output of the SCPA. For the SCPA implementation, the target maximum efficiency is obtained when the impedance that loads the SCPA (MN_{Zin}) has real part larger than $SCPA_{Zout}$ defined by a factor α as show in Eq. (1).

$$\alpha = \frac{R_L}{R_{on}} = \frac{real(MN_{Zin})}{R_{on}} \tag{1}$$

The α factor is dependent on the SCPA design and can be empirically defined from a load pull analysis where values between 3 and 6 are generally obtained. The SCPA efficiency analysis is presented in detail in [9] and [15]. The MN provides the correct load impedance for the maximum efficiency, contributes to the impedance matching with the next stage and provides a bandpass characteristic in order to filter the square wave V_o.

Lowering MN_{Zin} would result in higher SCPA output power. Nevertheless, a low load resistance would require even lower MOS parasitic resistances R_{on} in order to maintain the ratio α. Additionally, challenging large transformation ratios would be necessary on the MN and a high current would flow through the inverter. Due to these limitations, a standard SCPA with 1 V supply voltage can achieve peak output power around 18 dBm. Most of the cellphone and wireless standards require higher output power, therefore an external PA would still be needed.

Some design techniques can be used to enhance SCPA output power. As SCPA implementation presented in [15], working with stacked devices and higher supply voltages can reach peak output power of 25.2 dBm. It uses a 3 V supply in 1.5 V technology. High output power can be also obtained by means of power combiner as shown in [10]. This solution can reach peak output power of 28.6 dBm with a standard supply voltage of 1.1 V.

A standard SCPA with low output power can be employed for low-performance, low-range IoT application and for high-performance applications such as WLAN and LTE, presented techniques for high output power are necessary. For the proposed fully integrated transceiver, the SCPA implementation provides a low-power, digital intensive transmitter path.

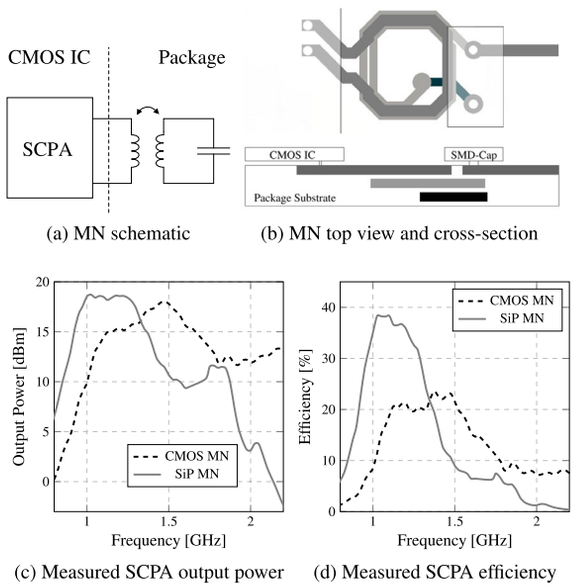

Fig. 8. SiP matching network design and measurement results [3]

4. Package integration solution

The impedance MN required for the SCPA is of extreme importance to reach the necessary output power, SCPA efficiency and filtering. For a commonly used differential SCPA, a transformer working as a balun is used as the main component of the MN. The resistive losses added by the parasitics of the transformer strongly influence the overall SCPA efficiency. With the tendency of integrating SCPAs on advanced technology nodes, integrated passives will lose quality and increase cost. Therefore, the research for high-quality low-cost transformers is fundamental for modern RF transceivers.

Recent technologies for system-in-package (SiP) integration are equipped with multiple metals and thin isolation layers, which allow the use of the available package substrate to design low-cost high-quality inductive devices. SiP transformers present a Q-factor of around 30, in comparison Q-factor of 10 to 15 obtained on CMOS technologies. In order to present the feasibility of a SiP MN and its advantages, an implementation example is shown where a 28 nm CMOS SCPA is evaluated with an on-chip matching network (CMOS-MN) and a package integrated network (SiP-MN).

A SiP-MN was designed on a 3-layer core-less package substrate [3]. As shown in Fig. 8a and 8b, the MN consists of a balun transformer designed on the substrate metal layers with a capacitor at the secondary, implemented as a surface-mounted device (SMD). The top view and the cross-section view of the MN are presented in Fig. 8b. The measured SCPA output power is shown in Fig. 8c and the SCPA efficiency in Fig. 8d.

Both implementations reach a peak output power of approximately 18 dBm. The SiP-MN presents a peak efficiency of 39%, which is significantly higher in comparison to the CMOS-MN with 23%. CMOS-MN presents efficiency better than 20% from 1.1 GHz to 1.5 GHz and SiP-MN presents efficiency better than 30% from 0.95 GHz to 1.3 GHz. It is important to remark that the design of lower frequency matching networks is more challenging, due to lower Q-factor obtained at low frequencies and larger inductance required.

The measured results correspond to a different frequency range than the target application proposed in this article. A redesign can be done for example at 2 GHz center frequency. From the measured results, the transformer Q-factor peaks between 1.5 GHz and 3 GHz

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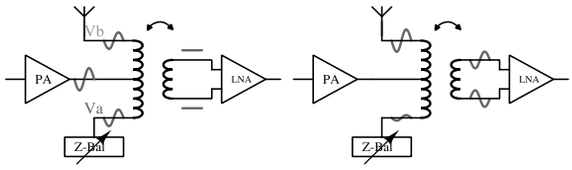

(a) Cancellation of Tx signal (b) Reception of antenna signal

Fig. 9. Working principle of electric balance duplexer

which benefits a higher frequency design. Additionally, lower inductor values are required for a higher frequency MN, resulting in area reduction.

5. Electrically balanced duplexer

In frequency division duplex (FDD) systems, the RX and TX signals are at neighbor frequency channels with a defined duplex spacing and share the same antenna. In order to ensure that the TX and RX signal do not interfere with each other, high-quality external bandpass filters are used as duplexers, as presented in Fig. 1. Even though many advances have been made in the TX and RX chain, the high-cost external duplexers are still a challenge to overcome.

An electric balance duplexer based on a hybrid transformer and a balanced impedance network was recently proposed as a fully integrated duplexer solution, as presented in Fig. 9 [7].

The PA is connected to the center tap of the transformer's primary. The antenna and the electric balance network (Z_{Bal}) are connected to the other pins of the primary. Z_{Bal} consists of a tunable impedance network used to mirror the antenna impedance. Ideally, when Z_{Bal} impedance matches to the antenna impedance (Fig. 9a), the TX signal flows from the center of the transformer to its extremities creating two identical voltages Va and Vb. The voltage difference over the transformer's primary is zero, therefore, the signal is not coupled to the secondary, and the receiver is isolated from the TX signal. The RX signal, shown in Fig. 9b, flows from the antenna through the primary and is coupled to the transformers secondary. The tunability of the Z_{Bal} should account for variations of the antenna impedance and environment changes.

EBD is a promising alternative for the high-cost external filter, but it still has several challenges on its implementation. Z_{Bal} needs to be designed for a large tunability range, covering antenna impedance variation of 1.5:1 VSWR, with high-resolution of 32 bits while maintaining the linearity of at least +70 dBm from TX to the antenna in order to fulfill the full-duplex scenario [8]. Moreover, a symmetrical center-tap transformer causes 3 dB losses on the TX chain due to the current divider, in addition to the losses due to the low Q-factor of integrated transformers.

The EBD presented in [7] has an isolation larger than the required 50 dB. However, the used hybrid transformer has a low Q-factor of around 10 which results in 11 dB insertion loss (IL) for the received signal. The insertion loss can be considerably improved with higher Q-factor transformers as shown in [8]. Thicker metal layers and larger area are used to reach a Q-factor around 17 which decreases IL to 3.9 dB.

Large hybrid transformers are feasible when using larger scale less-expensive CMOS technologies. Nevertheless, the large area is a limiting factor for using the EBD in a single-chip transceiver design in advanced technology nodes like 28 nm and 14 nm.

The transformer quality for SCPA matching network and integrated duplexer is critical as presented in Sects. 3 and 5. These transformers can be implemented on-chip with drawbacks of low Q-factor and a large area in high-cost IC technology. The implemented SiP transformers can replace on-chip designs to reduce the production cost, improve the SCPA efficiency and reduce the losses for SiP integrated duplexer.

6. Conclusions

In this work, an innovative transceiver architecture is presented based on the principle of sub-sampling down-conversion receiver with tunable-gain tunable-band LNA, high efficiency, fully integrated digital power amplifier (DPA), working as an RF-DAC and System in Package integrated duplexer solutions. Measured results are presented for important building blocks including low noise amplifier and matching network. The DPA provides a digital intensive, highly reconfigurable solution for the transmitter whereas the discrete time signal processing combined with sub-sampling in the receiver provides additional flexibility, low-power and less complex frequency synthesizer design. The presented architecture provides a step forward towards modern wireless front-ends and offers a highly efficient, cost effective solution.

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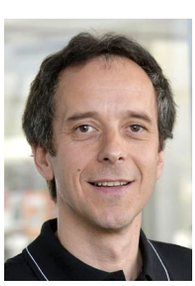

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