

Digital pulse-width modulator with spread-spectrum emission reduction

T. Karaca, M. Auer

Pulse-width modulated power-stages are used in many power-electronic applications because of their high efficiency. They are known to be a root cause for electromagnetic emission problems if no countermeasures are taken. This work presents a digital pulse-width modulator with an emission reduction method based on spread-spectrum modulation techniques. The proposed method is analyzed in detail, and two possible digital implementations are discussed. The implementations are compared in terms of chip-area and power consumption. Finally, an application of the proposed digital pulse-width modulator in a digitally-controlled Class-D audio amplifier is presented to show the feasibility of the concept. Using an FPGA prototype, a measured emission reduction of up to 9.5 dB is achieved.

Keywords: pulse-width modulator; spread-spectrum modulation; electromagnetic emission; Class-D amplifier

Digitaler Pulsweitenmodulator mit Spread-Spectrum-Emissionsreduktion.

Pulsweitenmodulierte Leistungsstufen werden aufgrund ihres hohen Wirkungsgrades in vielen leistungselektronischen Anwendungen eingesetzt. Sie sind bekanntermaßen eine der Hauptursachen für elektromagnetische Emissionsprobleme, wenn keine geeigneten Gegenmaßnahmen ergriffen werden. Diese Arbeit stellt einen digitalen Pulsweitenmodulator mit einem Emissionsreduktionsverfahren basierend auf Spread-Spectrum-Modulation vor. Das vorgeschlagene Verfahren wird im Detail analysiert, und zwei mögliche digitale Implementierungen werden diskutiert. Die Implementierungen werden in Bezug auf Chipfläche und Stromverbrauch verglichen. Schließlich wird eine Anwendung des vorgeschlagenen digitalen Pulsweitenmodulators in einem digital gesteuerten Klasse-D-Audioverstärker vorgestellt, um die Machbarkeit des Konzepts zu demonstrieren. Mit dem Prototypen wird eine gemessene Emissionsreduktion von bis zu 9,5 dB erreicht.

Schlüsselwörter: Pulsweitenmodulator; Spread-Spectrum-Modulation; elektromagnetische Emission; Klasse-D Verstärker

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1. Introduction

Pulse width modulators (PWM) are one of the core blocks of many power-electronic circuits. PWMs are used to encode an amplitude signal into a rectangular signal with varying pulse-width. They are needed especially in switched-mode power circuits, such as DC-DC converters, servo-motor drivers and power-amplifiers. In these applications, the active power components are operated as switches in order to achieve a high power efficiency and PWMs are needed to control these switches. Using PWM control, some state-of-the-art circuits achieve power-efficiency figures in excess of 95% [1].

Despite their high power efficiency, switched-mode circuits using a PWM have a major drawback. These circuits are prone to create electromagnetic emission. This emission can interfere with the functional integrity of other circuits inside the same device or violate legal emission limits as specified by EN or FCC regulations. The conventional way to deal with these emission is to apply filtering and shielding measures [2]. However, adding such additional components to a device is often not applicable due to cost or space requirements. Therefore several techniques have been developed to reduce the creation of emission already inside the switched mode circuit.

Slew-rate control methods [3, 4] are frequently used to reduce electromagnetic emission. The principle idea is to control the speed of voltage transitions at the power switches, thereby reducing high frequency noise. A drawback of these methods is their negative impact on power efficiency. Still, these methods are used in many applications [3–5] to counter high-frequency emission above 30 MHz.

For lower-frequency emission below 30 MHz spread-spectrum modulation (SSM) has shown promising results [6]. This technique distributes the generated emission energy over a large bandwidth, thereby reducing the overall amplitude of spiky emission. Moreover, the technique does not affect the power efficiency.

Several implementations of SSM for analog PWM [7–10] have been presented in the last years. However, an increasing number of switched-mode power circuits nowadays are digitally controlled. Analog methods for the implementation of SSM can no longer be used. Therefore, this work presents a digital PWM with SSM that is suitable for switched-mode power circuits with digital control. Related works presenting digital PWM with SSM [11–13] have focused on pseudo-random modulation for DC-DC converters. In contrast, this work shows a versatile implementation of periodic SSM. Moreover, the actual implementation effort of SSM in terms of area and power consumption for fully integrated applications is presented. Whereas many SSM implementations only focus on the emission reduction, this work also considers the penalties on the signal conversion performance of PWM. This enables the presented solution to be used also in highly linear power-amplifiers. Finally, the proposed concept is demonstrated with an FPGA based prototype.

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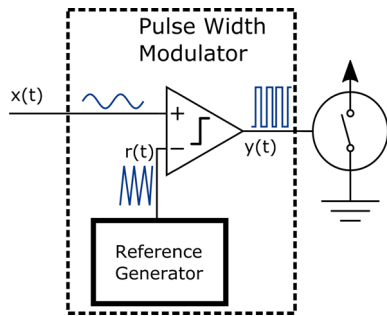


Fig. 1. Simplified block diagram of a PWM driving a power-switch

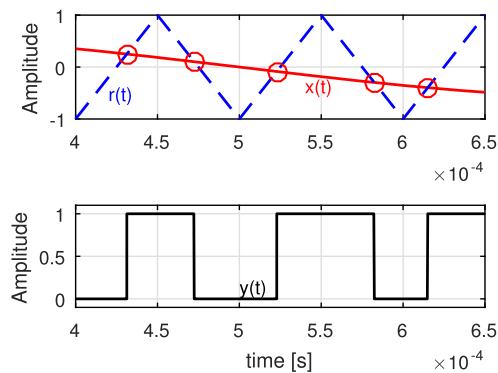


Fig. 2. Operation principle of the PWM: waveforms at the different nodes

The paper is organized as follows: Sect. 2 introduces the basic principles of PWMs and SSM, Sect. 3 presents the proposed digital PWM, describing the implementation in detail, Sect. 4 shows the application of the proposed PWM. An FPGA based prototype of a Class-D audio amplifier is presented and measurement results are given. Finally Sect. 5 summarizes the works.

2. Pulse width modulators and spread-spectrum modulation

Figure 1 shows the main building blocks and Fig. 2 the operation principle of a typical PWM. The PWM is used to encode an amplitude signal into a rectangular signal with varying pulse-width. The average of the resulting rectangular signal ideally represents the input amplitude signal. The created signal has only two levels and can be directly used to control a power-switch. As switches ideally do not dissipate power, a PWM in combination with a switch can be used to build a very power efficient voltage conversion system. Even for non-ideal switches the losses can be kept low and highly efficient systems are possible.

The PWM typically consists of two main building blocks, a reference signal generator and a comparator. The reference signal generator creates a sawtooth or triangle waveform. Triangle waveforms are preferred in many applications, as the resulting PWM signal shows lower unwanted harmonics [14]. The fundamental frequency of this reference signal is at least twice the input signal bandwidth. In many practical applications fundamental frequencies of 0.1 MHz to 1 MHz are used. The comparator detects the intersection points of the input signal with the reference signal, thereby creating a pulse width modulated rectangular output signal.

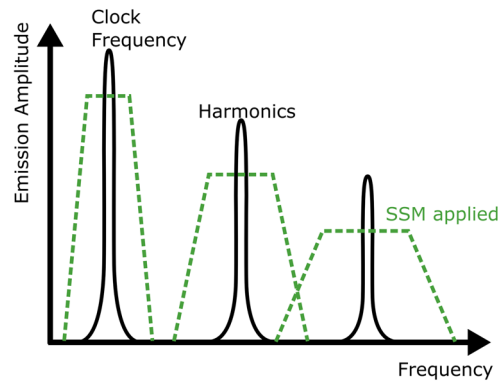


Fig. 3. Frequency domain representation of a clocked circuit's emission, with and without SSM

The output signal $y(t)$ of the PWM with triangular reference signal can be mathematically described as [14]:

$$y(t) = x(t) + \sum_{k=1}^{\infty} \frac{2(-1)^k}{k\pi} \left[\sin\left(2\pi k f_R t + k\pi \frac{x(t)+1}{2}\right) - \sin\left(2\pi k f_R t - k\pi \frac{x(t)+1}{2}\right) \right] \quad (1)$$

with the fundamental frequency f_R of the triangle waveform, and input signal $x(t)$. In typical applications, f_R is at least an order of magnitude higher than the highest frequency in $x(t)$. Thus the resulting signal $y(t)$ can be divided into a low frequency and a high frequency part. The low frequency part of $y(t)$ perfectly encodes $x(t)$, without adding any distortion or unwanted signal components. This feature is used in many power amplifiers processing band-limited input signals. The high frequency part of $y(t)$ consists of harmonics of the reference signal, each being phase modulated by the input signal. This high frequency content is unwanted in most applications and is a root cause of the created emissions. The energy of this unwanted signal content is concentrated around $(k f_R)$ and can propagate to other electronic circuitry via various coupling mechanisms and thereby create interference.

Spread-spectrum modulation (SSM) [6] is a well known technique to reduce interference created by clocked electronic circuits. These circuits, such as synchronous digital electronics often create emission at their clock frequency and multiples of it. A reduction of the created emission amplitudes can be achieved by using a variable frequency clock instead of a fixed frequency one. For instance in digital communication [15] the frequency of the digital clock is modulated with a certain pattern. This causes the emission to no longer being concentrated at fixed frequencies, but being spread over a larger frequency band, resulting in a signal that has a smaller overall amplitude. Figure 3 illustrates the resulting emission spectra.

This idea has been applied to various analog PWM [7–10]. The implementation is as follows: Instead of using a reference generator that creates a triangle signal with a fixed frequency f_R , a variable frequency reference generator is used which has an output frequency confined to $f_R \pm \Delta f$. The variable frequency reference generator can be implemented having either a pseudo-random frequency pattern, or a periodic frequency pattern. Our previous works [16] have revealed that periodic frequency modulation generally leads to better emission reduction for the same frequency deviation Δf . In such periodic SSM implementations, the reference triangle signal is frequency modulated by $\pm \Delta f$ using a periodic modulation signal of frequency f_m . The result is, that the energy of $y(t)$'s unwanted signal

content is no longer concentrated around (kf_R), but is distributed over a larger bandwidth. This bandwidth can be roughly estimated for $k = 1$ using Carson's rule as: $2(\Delta f + f_m)$.

However, quantifying the achieved emission reduction is not straightforward. Sometimes simply the spectrum of the created emission is measured. The obtained results heavily depend on the used measurement instrument, in particular on its effective frequency resolution. Various quantification setups can be found in the literature [7, 9–11] and in datasheets [17] of devices using SSM. This makes comparison of different SSM implementations very difficult if not impossible. We believe, that an EMI-Test-Receiver as specified in CISPR16-1-1 should be used to quantify the emission reduction of an SSM method. These instruments have standardized measurement characteristics and are used in legal emission measurements according to EN/FCC regulations. Thus the use of a CISPR-16 conformal EMI-Test-Receiver leads to fair and comparable results of emission reduction due to SSM. Moreover, it is well known [18–20] how to set the modulation parameters (profile, modulation frequency f_m and deviation Δf) to achieve the best emission reduction for a certain application when measuring with such an receiver.

3. A digital PWM with SSM

In the last years, significant advances were made in the semiconductor industry regarding digital design while analog design could not keep up with this pace. It is therefore only natural that an increasing number of switched-mode power circuits nowadays is digitally controlled. In such circuits digital PWMs are used. In the following an approach how to implement SSM in a digital PWM is presented. The implementation is targeted at fully integrated implementations and all the resulting area and power consumption figures are derived from synthesis of the circuit in a 180 nm CMOS technology, with a supply voltage of 1.8 V and a digital clock frequency f_c of 100 MHz.

A digital PWM in a synchronous design can be implemented [13] using a counter to generate the reference signal $r[n]$ with a sample rate of f_c . For the sake of simplicity, it can be assumed that an up-down counter is used to generate a triangular-like reference signal. This reference signal can be regarded as a stair-step signal approximating an ideal triangular signal. The number of different steps N_S is given by the digital clock frequency f_c and the repetition rate f_R of the triangular-like signal as:

$$N_S = \frac{f_c}{2f_R} \quad (2)$$

It follows, that for a certain fundamental frequency f_R of the reference signal, the resolution of the approximated signal is limited by the digital clock frequency.

The reference signal $r[n]$ is compared to a pulse code modulated digital input signal $x[m]$ to generate the output signal $y[n]$. In contrast to analog PWMs, the pulse width of the output signal is now quantized, according to the N_S of the counter, leading to quantization noise in the output signal, which means that non-linear distortion is introduced. The sample rates of $r[n]$ and $x[m]$ can be different. In many implementations, the sample rate of $x[m]$ is chosen to be f_R , even though this leads to a non-linear signal encoding [14].

To implement SSM, the repetition rate f_R of the reference signal must be modulated. Equation (2) shows two possible ways: One possible implementation is to modulate the frequency f_c of the digital base clock as demonstrated in [12]. However, this can impact the whole electronic system, especially if the digital base clock is also used for several other digital and mixed-signal blocks. A more practical way of modulating f_R , is to change the number of counter steps N_S . In this way, the modulation of f_R can be achieved without

affecting any other circuit blocks. Still, this method has one drawback. The mapping from a digital input code to a duty-cycle on the output is modified by changing the number of counter steps. Therefore, for a certain input signal, an encoding error is introduced when changing N_S . Nevertheless this introduced error is highly deterministic and can be considered a gain error. Therefore it is possible to correct for this error. We thus propose a digital counter-based PWM, that implements SSM by modulating the number of counter steps. An additional error correction circuitry is inserted in front of the PWM to precompensate for introduced errors.

The digital implementation is shown for the following scenario. A 180 nm CMOS technology is used, with a digital clock frequency f_c of 100 MHz. The input signal $x[m]$ is an 8-bit PCM signal in 2's complement representation with a sample rate f_S of $\frac{f_c}{128}$. The PWM shall operate at a fundamental frequency of around 400 kHz. The area estimates are determined after synthesis using a Cadence® design flow. The power figures are estimated by the synthesis tool, using appropriate toggle values for each net, which are generated by simulation. The simulation is run for 1 ms. The input signal $x[m]$ is a 1 kHz sinusoidal PCM signal with an amplitude of 90% of the full scale.

As a reference implementation, a fixed frequency PWM was designed. A 7 bit up-down counter was implemented which results in $f_R = 390.625$ kHz. This leads to $N_S = 128$ and $\frac{f_c}{f_R} = 2$. The counter outputs a 2's complement triangle signal ranging from -64 to 63 which is compared to the input signal. The least significant bit of the input signal is discarded. The implementation consumes $90 \mu\text{W}$ and needs $2300 \mu\text{m}^2$ of silicon area.

The SSM-PWM is intended to achieve a good emission reduction when measured according to CISPR16 with peak detector. For this case, it is well known [18–20] how to choose the modulation parameters to achieve good emission reduction. To reduce peak-detector measurements, modulation with a triangular profile and modulation frequency f_m larger than 10 kHz can be used. To achieve an emission reduction larger than 6 dB, the frequency deviation $\pm\Delta f$ should be larger than $3f_m$ (larger than 30 kHz).

For comparability, it was decided, that the PWM should have $N_S = 128$ on average. Thus the SSM-PWM is implemented using an 8 bit up-down counter with configurable upper and lower bounds. It counts up, until it reaches the set upper bound, then starts counting down until it reaches the set lower bound and vice versa. To implement a triangular modulation profile, the upper and lower bounds have to be increased stepwise and then accordingly decreased. This is achieved with two additional up-down counters to determine the bounds. One of these additional counters is updated whenever the main counter reaches its set upper bound, the other at the set lower bound. Each of the additional counters has N_{SSM} steps. Thus, the upper bound of the PWM counter can be altered by $N_{SSM} + 1$ and the lower bound can be altered by the same amount. Therefore, the main counter has $N_S = 128 \pm N_{SSM}$ steps. As the upper and lower bound is modified at every cycle, N_S changes by two every PWM cycle.

Finally, N_{SSM} was selected to be 14, leading to a triangular modulated PWM with $f_R = 390 \pm 43$ kHz and $f_m \approx 14$ kHz. Figure 4 shows the VHDL simulation of the implemented reference signal with SSM. In the end a third additional up-down counter was added, to track the current number of PWM steps, as this value was needed for error-correction. In the implementation, all the additional counters are clock-gated, as they are incremented infrequently. The implementation consumes $120 \mu\text{W}$ and needs $8100 \mu\text{m}^2$ of silicon area.

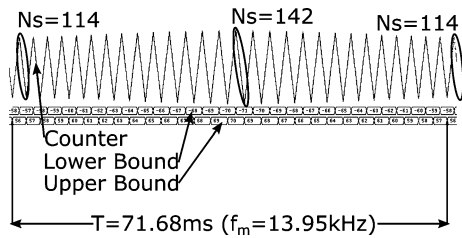


Fig. 4. VHDL simulation of the implemented SSM reference generator

Table 1. Area and power consumption of the digital blocks. Implemented in 180 nm CMOS with 1.8 V supply and clock frequency $f_c = 100$ MHz. Input signal: 8-bit PCM sampled at $f_c/128$

Block	Area [μm^2]	Power [μW]
Reference PWM	2300	90
SSM-PWM	8100	120
Error correction, multiplier	3400	7
Error correction, LUT	38000	40

3.1 Multiplier based error correction

The digital input signal $x[m]$ of a non-SSM PWM with N_{S0} counter steps is mapped to a duty-cycle (DC) of

$$DC = \frac{x[m]}{N_{S0}} \quad \text{with } x[m] \in [0; N_{S0}]$$

Altering the number of counter steps to N_{Sx} leads to an erroneous duty-cycle $DC = x[m]/N_{Sx}$ which can be corrected by multiplying the input value $x[m]$ with a correction factor N_{Sx}/N_{S0} .

Thus, one way to correct for the introduced error is to multiply the input value $x[m]$ with the current number of steps in the counter then divide the result with the average number of steps. In this case, this number is 128 (2^7) and the division can easily be implemented with a right shift operation. The current number of steps is provided by the SSM-PWM, and can be represented by an 8-bit unsigned number, the input signal is a 8-bit 2's complement number. The multiplier and shift operation is added as asynchronous combinational block in front of the SSM-PWM and provides an 8-bit 2's complement number to the SSM-PWM. The multiplier, implemented using a *non-booth* algorithm, consumes 7 μW and needs 3400 μm^2 of silicon area.

3.2 Look-up table based error correction

For comparison, it was evaluated, whether a look-up table (LUT) replacing the multiplier could reduce area and power consumption. The error-correction needs to consider $2 * N_{SSM} + 1 = 29$ possible mappings of all the input values. With 8-bit input values and 8-bit output values, the LUT needs 7.25 kB. For a first estimate, no data reduction was considered. Again, the LUT will be placed as asynchronous combinational block in front of the SSM-PWM. The LUT is implemented as ROM, consumes 40 μW and needs 38000 μm^2 of silicon area. As can be seen, significant data reduction would be needed, to achieve a better performance, than the multiplier. Consequently, for this work the error correction using a multiplier was chosen. Table 1 summarizes all the estimated implementation parameters.

4. A digitally-controlled Class-D audio amplifier

Before going to silicon, a rapid-prototype was developed. In this way the feasibility of the proposed SSM-PWM could be easily evaluated

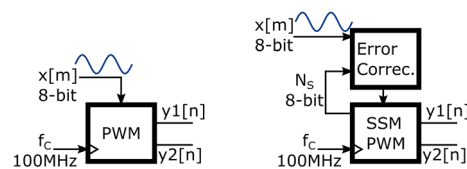
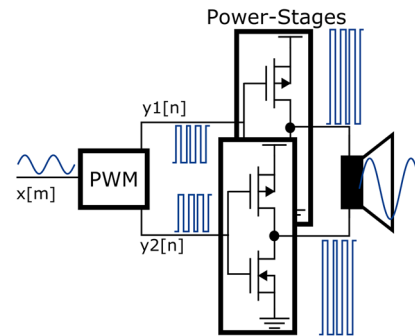


Fig. 5. Upper: block diagram of the Class-D audio amplifier for mobile applications. Lower: the PWM block is implemented in two ways: (a) reference PWM; (b) SSM-PWM with error-correction

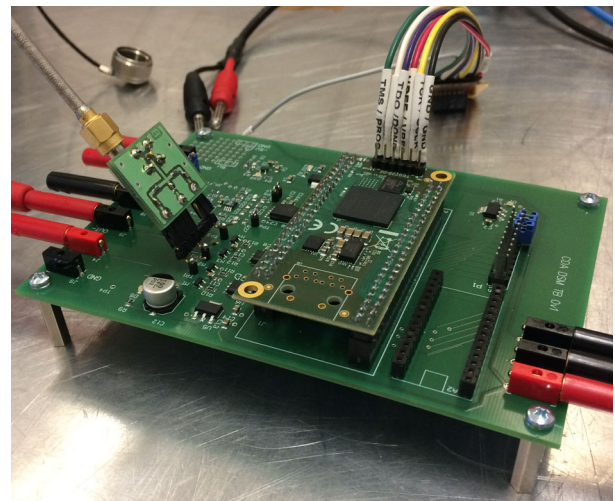


Fig. 6. Picture of the rapid-prototype board

and the actual emission reduction could be measured. The prototype is a PWM based Class-D audio amplifier. These kind of amplifiers have become very popular for driving loudspeakers in a very power efficient way. Figure 5 shows a simple block diagram of the amplifier. The PWM block converts the input signal into a pulse-width modulated signal. It outputs two differential PWM-signals, which drive a switching power-stage. The amplified signal is directly applied to an electrodynamic loudspeaker. The loudspeaker has an intrinsic low-pass behavior, such that only the low-frequency content of the output PWM-signal contributes to the generated sound.

The prototype is built using an FPGA to implement the digital blocks. Figure 6 shows a picture of the prototype. The power stage is built of discrete MOS-transistors controlled by off-the-shelf integrated drivers. The power stage is supplied with 5 V and can drive up to 1.5 W into an 8 Ω loudspeaker. Additionally, a small mixed signal control loop was added around the PWM and power-stage to improve the audio performance. The control-loop mainly suppresses errors induced by the power switches and performs quantization-

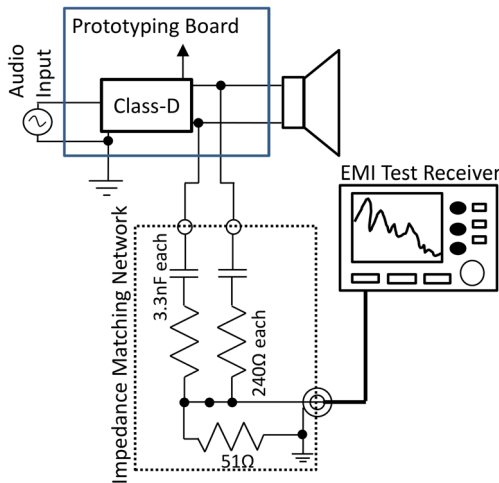


Fig. 7. 150 Ω conducted emission measurement setup, applied to the prototype

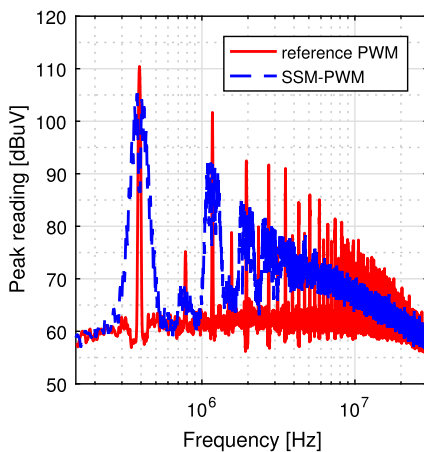


Fig. 8. Measured conducted common-mode emission

noise shaping to achieve a higher dynamic range in the audible bandwidth. As before, the FPGA was clocked at 100 MHz. The described reference PWM and the proposed SSM-PWM are ported to the FPGA. In contrast to the PWM implementations above, a second digital comparator was added to generate the second output signal.

This prototype was used to evaluate the emission reduction when using the proposed PWM with SSM. For the evaluation, the 150 Ω direct-coupling measurement setup according to IEC 61967 was used. Figure 7 shows the setup. This measurement setup is actually intended to measure the emission of integrated circuits. Yet, as this setup allows comparable and repeatable results it was considered very suitable for this task. Using a matching network, the common-mode voltage on the speaker lines is probed. This common-mode voltage is considered one of the root-causes of interference. The signal is measured with a CISPR-16 conformal EMI-Test-Receiver in CISPR-Band B (0.15 MHz to 30 MHz). The peak detector is used with a dwell-time of 10 ms. The amplifier was loaded with a loudspeaker dummy consisting of 8 Ω and 44 μH in series. The measurements were carried out with a 1 kHz input signal, creating 1 W at the load.

Figure 8 shows the emission spectra for the reference PWM and the SSM-PWM. The emission spreading effect is clearly visible. An emission reduction of 5 dB at the fundamental PWM harmonic and 9.5 dB at the third harmonic is achieved.

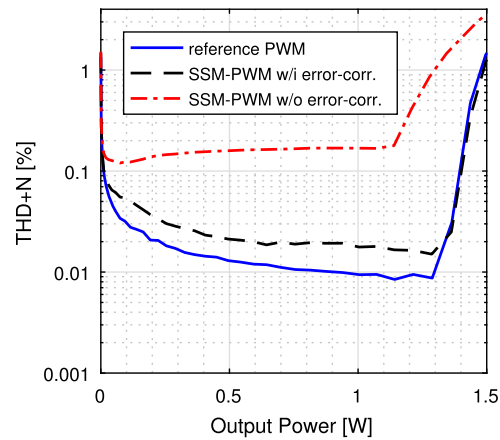


Fig. 9. Measured THD+N vs. output power

Next, the performance of the error-correction circuitry is evaluated. For this reason, the *total harmonic distortion and noise ratio* (THD+N) was measured using an audio analyzer. In this measurement, a high quality sinusoidal signal is applied to the Class-D audio amplifier. The amplifier's output spectrum is measured in the audible range (20 Hz to 20 kHz). Then the power of the amplified sinusoidal signal P_{SIN} is compared to the power of all the additional signals P_{HD+N} present at the output. P_{HD+N} typically consists of harmonic distortion components created by the amplifier's non-linearity and noise components added by the amplifier. THD+N is calculated as:

$$THD + N = \frac{P_{HD+N}}{P_{SIN}} \quad \text{typically notated in \%} \quad (3)$$

For this measurement, the amplifier was again loaded with the loudspeaker dummy and the input signal amplitude was swept. In this way, also the clipping behavior of the amplifier can be evaluated. Figure 9 shows the result for the reference PWM and the SSM-PWM with and without error-correction. The THD+N is plotted versus the power at the dummy load. The implemented error-correction circuitry significantly improves the audio performance. Still there is a small penalty of about 0.006% in THD+N compared to the reference PWM. Without error correction, the amplifier starts clipping very early. Thanks to the error-correction the linear output range is completely restored.

5. Conclusion

In this work, we presented a spread-spectrum implementation for digital PWM which is compatible with highly linear voltage converters. The area and power overhead of the presented emission reduction method was shown for a fully integrated implementation. Finally the proposed implementation was tested on an FPGA prototype, showing impressive emission reduction of up to 10 dB, with only minor impact on the signal conversion performance. Although higher reduction is possible using more elaborate methods, this technique clearly stands out owing to its lightweight implementation with low overhead and low power consumption. For comprehensive emission reduction, the proposed digital SSM implementation can be easily combined with a slew-rate controlled power-stage (such as [4] or [5]). In this way, emission created by the low order harmonics of the PWM's reference signal are reduced by SSM. The high-order harmonics are countered by slew-rate control.

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