Aspect ratio of radiation-hardened MOS transistors

Modelling of the equivalent channel dimensions of integrated MOS transistors in radiation-hardened enclosed layout

V. Bezhenova, A. Michalowska-Forsyth

The reliability of electronics in the proximity of the ionizing radiation is a key requirement in particular in high energy physics, nuclear power or space applications. One way to improve robustness of MOS transistors operating in such environments is to use enclosed layout techniques. This special layout approach helps to maintain leakage current of MOS transistors at low level even after irradiation, in contrast to a linear layout MOS transistor, where leakage current could increase by orders of magnitude. The issue, arising with enclosed layout transistors, is related to channel modelling, since the MOS transistor gate geometry is no more a simple rectangle. In this work, modelling of equivalent width and length dimensions of the MOS transistor channel under the gate is addressed. For this purpose transistors of four types and two layout versions, fabricated in a standard 180 nm CMOS process, are characterized. The accuracy of available models for equivalent channel dimensions is analysed, along with a new simplified geometrical model developed by the authors. They are further compared to the empirically extracted aspect ratio. The improvement possibilities for the considered models are then identified.

Keywords: MOS transistor; radiation hardness; ionizing radiation; enclosed layout; aspect ratio

Kanalgröße eines strahlungsfesten MOS-Transistors. Modellierung der äquivalenten Kanalgröße eines integrierten MOS-Transistors mit strahlungsfestem "enclosed"-Layout.

Die Zuverlässigkeit der Elektronik in der Nähe von ionisierender Strahlung ist eine wichtige Anforderung in Anwendungsbereichen wie z. B. der Hochenergie-Physik, Kernenergie oder Weltraumforschung. Eine der Möglichkeiten, diese Zuverlässigkeit zu gewährleisten, ist der Einsatz der so genannten "Enclosed layout"-MOS-Transistoren, deren Gate eine der anderen Elektroden umschließt. Diese besondere Layouttechnik gewährleistet einen niedrigen Leckstrom des Transistors auch nach der Bestrahlung, im Gegensatz zu einem Standardtransistor, mit einem linearen Layout, dessen Leckstrom sich um einige Zehnerpotenzen vergrößern kann. Dabei entsteht das Problem der Modellierung, da der MOS-Transistor kein einfaches Rechteck ist. Im Zuge dieser Arbeit befassen wir uns mit der Modellierung der äquivalenten Kanalgröße des MOS-Transistors. Dafür werden vier Typen und zwei Layout-Versionen der Transistoren, die in einer kommerziellen 180-nm-CMOS-Technologie gefertigt wurden, charakterisiert. Die Genauigkeit der verfügbaren Modelle der Kanalgrößenbestimmung zusammen mit einem vereinfachten, von den Autoren entwickelten Modell wurde analysiert und mit der experimentalextrahierten Größe verglichen; die Verbesserungsmöglichkeiten der analysierten Modelle sind identifiziert.

Schlüsselwörter: MOS-Transistor; Strahlungsfestigkeit; ionisierende Strahlung; enclosed Layout, Kanalgröße

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1. Introduction

Applications, such as high energy physics, nuclear power or space require high precision and high reliability electronics. Integrated circuit functionality and keeping-to-the-specification is critical in these applications, despite harsh environments and in particular under the ionizing radiation.

Cumulative effects of e.g. X-rays after a long-term exposure can cause damage to integrated circuits. In particular electrical characteristics of single devices can significantly change. One of the parameters that degrades is the leakage current of a MOS transistor. Under high ionizing dose, increase in leakage current by few orders of magnitude can be measured [1–3]. Due to ionization electron-hole pairs are created across the IC volume. Since modern MOS transistor gates are only few nanometres thick, charge carriers can tunnel through the thin insulator. However there are also the few hundred nanometre thick insulating regions of shallow trench insulation (STI) that separate individual devices. Here, electrons with higher mobility are swept from the oxide, but holes get trapped causing the parasitic electric field [4]. The STI-trapped positive charge is a serious issue in N-type MOS transistor, affecting its leakage current. When the transistor is switched off with gate potential at zero volts, the

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radiation-induced electric field under the STI region creates parasitic channel. This is the path for the radiation-induced leakage current in the standard, rectangular gate layout MOS transistor. This is illustrated in Fig. 1. This non-zero potential under STI is not only causing the parasitic channel in the N-type MOS transistor but also can lead to leakage currents between transistors or diodes. Special techniques, like guard-rings might be necessary to mitigate it.

A special layout technique, enclosed layout transistor (ELT), helps in maintaining the leakage current of N-type MOS transistor at low level even after irradiation. In the literature ELT is also referred to as edgeless transistor [5], since this layout avoids the STI edges between drain and source regions. The two most popular versions of ELT are shown in Fig. 2B and C: annular gate and ringed source layout.

In case of the annular gate the top view shows that transistor is highly asymmetric. There is a choice of the inner or the outer terminal as drain. The inner one means lower drain capacitance. This is often desired, both in analog and in digital design. The outer terminal as drain results in lower output conductance, which is theoretically derived from the charge conservation principle [6, 7]. If drain is the external terminal, then drain perimeter is larger than source perimeter. Therefore the channel length is less modulated, even less than in linear transistor. A limitation of the annular gate is that the minimum width is much larger than that of a linear MOS transistor.

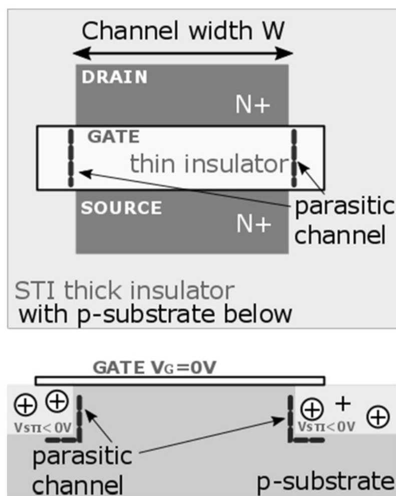

Fig. 1. Top view and cross-section of the N-type MOS transistor with parasitic channel created by STI

So this layout style is particularly interesting for transistors where large *W/L* ratio is required. Also, with larger widths corner effects are more negligible, making it easier to estimate the effective channel dimensions.

The ringed source layout is much easier approximated by a rectangular MOS transistor channel. However the poly-silicon covers larger area (shaded area in Fig. 2C) than the active channel region and the terminal that is enclosed has a high capacitance associated with gate. Therefore this MOS transistor layout is typically arranged with enclosed source, thus the name "ringed source". This layout enables the minimum width to be nearly as small as in case of standard linear MOS transistor. For this reason ringed source might be particularly interesting for designing current mirrors at low currents.

In both cases however the SPICE modelling of the transistor characteristics for circuit simulations needs additional effort, since these are not anymore simple rectangular shapes like the devices included in standard library. With the non-symmetrical layout the main differences to standard linear MOS transistor model are:

- the drain and source capacitances,
- the gate capacitance, including significant changes to the overlap capacitance (that highly differ also between both ELT layout styles),
- the mentioned above channel length modulation, which does not follow the simple linear model any more,
- and, above all, the equivalent channel dimensions assuming that the current-voltage characteristics can be still modelled with the linear layout transistor [8].

As development of new SPICE models comes at high cost, therefore for circuit simulations a macro-model based on existing SPICE model of the rectangular layout is most conveniently used. With this approach the key action is derivation of the effective channel dimensions, or in other words finding such equivalent *W* and *L* of a rectangular layout that meets the current-voltage characteristics of the measured ELT MOS transistor.

In the following steps adjustments to macro-model are necessary, in particular to correct for capacitances and output conductance of the non-symmetrical layout [7, 9]. In this paper we focus on the first step, the equivalent *W/L* ratio calculation. Having done literature studies of the equivalent *W/L* estimation we compare different models and verify experimentally with measurements on both layout types: annular gate and ringed source, fabricated in a commercial 180 nm CMOS process.

2. Experimental structures

Dedicated custom-designed test chip was fabricated in a standard 180 nm CMOS technology and assembled in ceramic package. Fig-

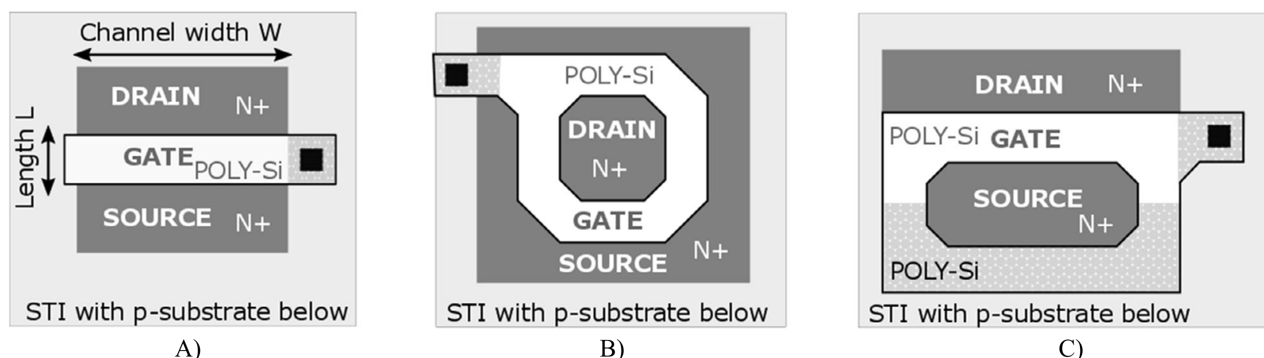

Fig. 2. Standard/linear (A), annular gate (B), and ringed source (C) MOS transistor layouts

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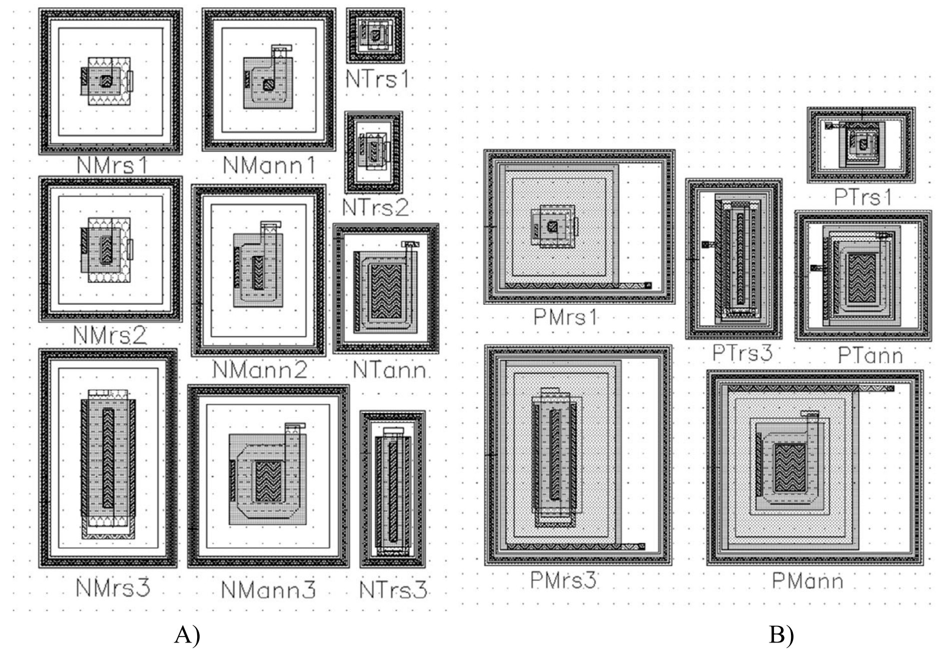

Fig. 3. Physical layout of the MOS transistor test structures: N-type (A) and P-type (B)

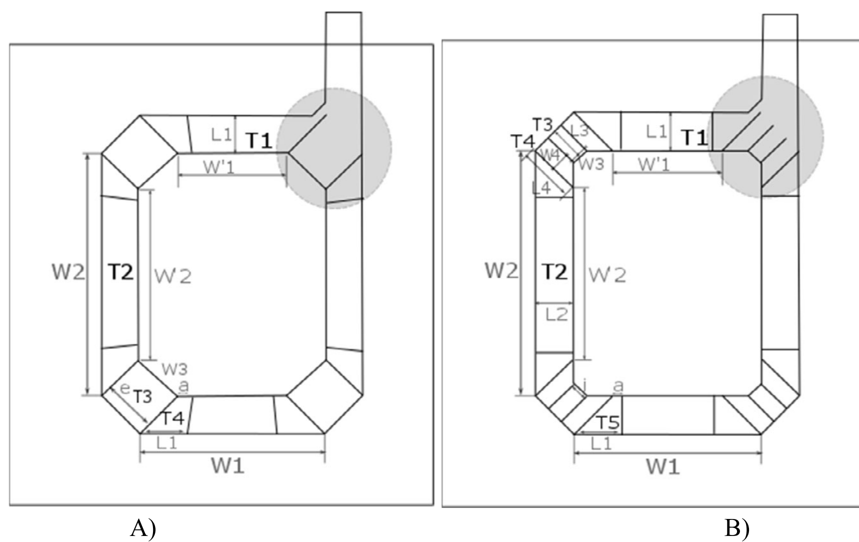

Fig. 4. Annular gate transistor geometrical model after [10] (A) and adapted for this work (B)

ure 3 shows the test structures considered in this work. Transistors of different types, gate oxide thickness and different geometries were implemented on chip. Such variety allows the following:

- validate geometrical approach to estimate the equivalent channel dimensions
- check scalability of this estimation
- explore minimal possible geometries for the given technology

3. Analytical equivalent channel dimensions estimation

3.1 Annular gate

Here we analyse the state-of-the-art models for equivalent channel dimensions estimation, along with our own geometrical model. We consider contributions of Giraldo et al. [10], Xue et al. [11] and Snoeys et al. [12]; additionally we compare simple mid-line approximation and our new equilateral trapezoid transistor approximation methodology.

In their work [10] Giraldo et al. propose to divide the annular gate ELT into 3 types of smaller transistors, as shown in Fig. 4A, based on a conformal mapping technique. In this case, the lengths of the internal and external corner "cuts" are equal (parameter *e* in Fig. 4A), in contrast to Fig. 4B where the additional parameter *i* was introduced. Such geometry however does not allow exploring the minimum feature device. In our work we study an annular gate ELT, where $i \neq e$. This means, the model proposed in [10] has to be adapted, as shown in Fig. 4B. The equivalent *W*/*L* in this case is sum

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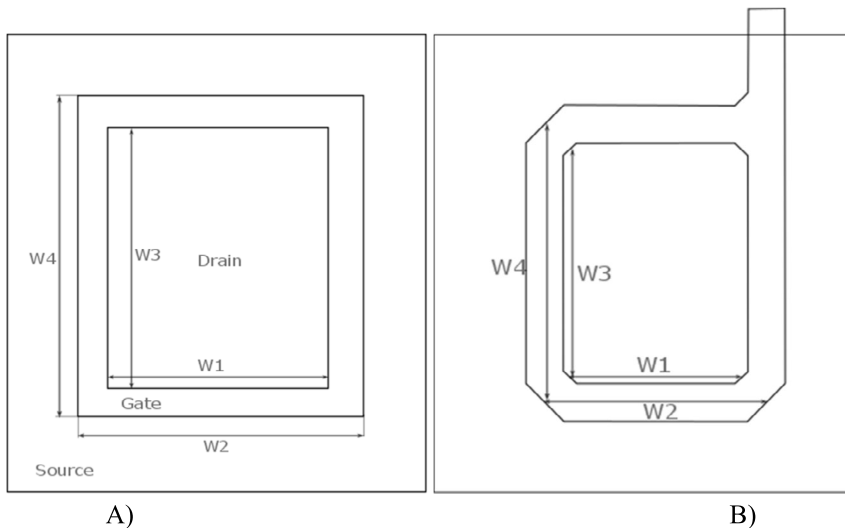

Fig. 5. Annular gate MOS transistor geometrical model after [12] (A) and adapted for this work (B)

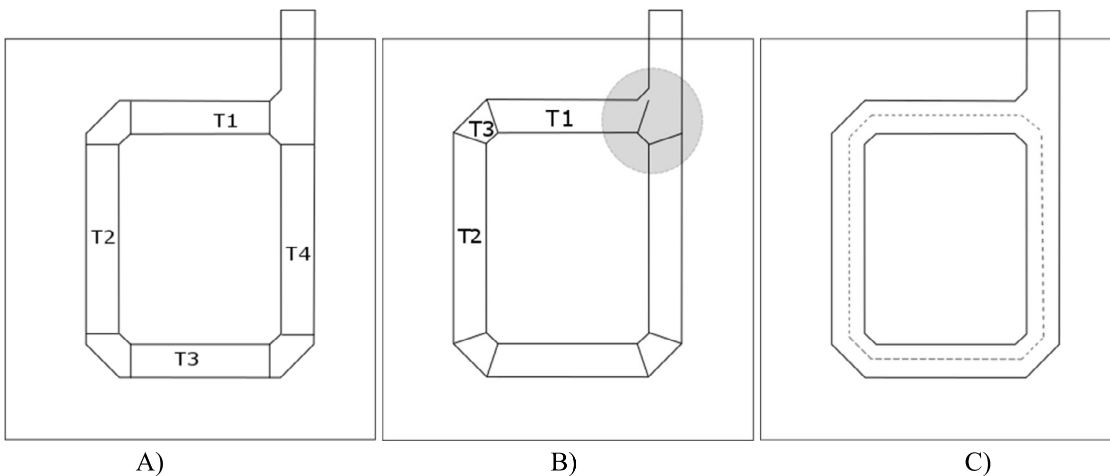

Fig. 6. Annular gate MOS transistor geometrical model after [11] (A), trapezoid transistors (B) and mid-line approximation model (C)

of W/L of 5 transistors, instead of 4 (1):

$$\frac{W}{L}=2\cdot\left(\frac{W}{L}\right)_1+2\cdot\left(\frac{W}{L}\right)_2+4\cdot\left(\frac{W}{L}\right)_3+8\cdot\left(\frac{W}{L}\right)_4+8\cdot\left(\frac{W}{L}\right)_5 \quad (1)$$

Snoeys et al. present in their work [12] a model for rectangular annular gate transistor, as shown in Fig. 5A. For the given geometry of our experimental structures, the parameters W1 and W2 were taken as illustrated by Fig. 5B. The equivalent channel dimensions were then calculated as sum of the 4 transistor sides (2):

$$\frac{W}{L}=\frac{4}{\ln\frac{W_2}{W_1}}+\frac{4}{\ln\frac{W_4}{W_3}} \quad (2)$$

The model presented by Xue et al. [11] proposes to divide annular gate transistor into 4 linear transistors, as in Fig. 6A, and compensate for corners influence with a coefficient C_{ab}, as in Eq. (3):

$$\frac{W}{L}=\sum\frac{W}{L}_i+C_{ab} \quad (3)$$

For the equivalent channel dimension estimation during design stage we have used a simplified model, based on the approach proposed in [10]. In this model we subdivide transistor into 8 trapezoidal sub-devices, as illustrated by Fig. 6B. This approach allows more flexibility and is thus applicable for any design rules.

Finally, the mid-line approximation was also analysed. This method suggests that one can approximate the equivalent channel dimensions of the annular gate transistor by the middle line of the gate area (Fig. 6C).

3.2 Ringed source

In contrast to annular gate transistors, there are much fewer models for the equivalent channel dimensions calculation of the ringed source layout. Here we consider two major contributions – by Nowlin et al. [13], and by Ramos-Martos et al. [14], whereas the latter is a modification of [13].

In both these models, the gate is subdivided into 5 regions: two corner regions, two edge regions, one "as-drawn" length region. It is assumed that only gate to the left of the source region middle is contributing to the total W/L. It is illustrated by Fig. 7A. The effective W/L is then a simple sum of the W/L of the sub-devices. According

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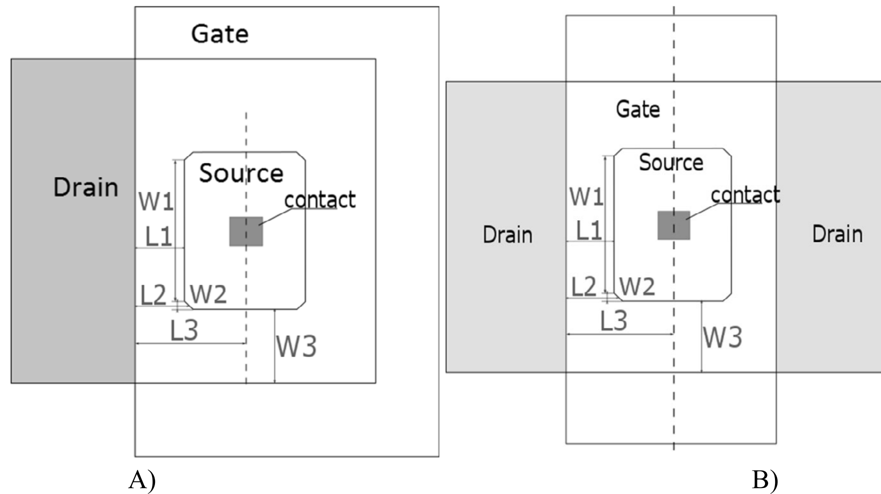

Fig. 7. Ringed source transistor geometrical model after [13] and [14]: single drain (A) and double drain (B)

to [13], the effective *W/L* then is (4):

$$\frac{W}{L} = m \cdot \left(\frac{W}{L}\right)_1 + n \cdot \left(\left(\frac{W}{L}\right)_2 + \left(\frac{W}{L}\right)_3\right) \quad (4)$$

Where m is the number of drains, and n is the number of corners per drain; for example in Fig. 7A: $m = 1$ and $n = 2$.

In their work, Nowlin et al. state that the corner contributions are expected to be overestimated, and suggest that n can be used as fitting parameter to correct for this overestimation.

Another adaptation of the same model is proposed in [14], where the authors introduce additional empirical coefficients to correct for the uncertainties of the corners. For the single drain transistor (5):

$$\frac{W}{L} = \left(\frac{W}{L}\right)_1 + 2 \cdot \left(\left(\frac{W}{L}\right)_2 + \frac{2 \cdot n_c + 3}{4} \cdot \left(\frac{W}{L}\right)_3\right) \quad (5)$$

And for the double-drain transistor (6) (Fig. 7B):

$$\frac{W}{L} = 2 \cdot \left(\frac{W}{L}\right)_1 + 4 \cdot \left(\left(\frac{W}{L}\right)_2 + \frac{n_c + 5}{6} \cdot \left(\frac{W}{L}\right)_3\right) \quad (6)$$

where n_c is number of source contact rows.

4. Experimental estimation of the equivalent channel dimensions

The most common approach to define the equivalent channel dimensions of the ELTs is to compare electrical characteristics of these devices with correspondent characteristics of the standard layout devices. It can be done either by comparing with simulation or with measurement results. Only recently Cardoso and Balen [15] have communicated a study on various models for annular gate ELTs equivalent channel dimensions estimation compared to the equivalent channel dimensions estimation by a commercial design tool. Comparison with simulation of standard devices allows unlimited and precise variation of the dimensions of the standard layout transistors, but this approach doesn't take into account the process variations of the particular produced lot of silicon wafers. Comparison of the measurement results of both ELTs and standard layout MOS transistors takes these variations into account, but in this case, the number of devices within the test chip is limited.

In this work we propose extraction of the equivalent channel dimensions from the electrical characteristics of the ELTs. The drain current of the MOS transistor is directly proportional to its *W/L*. In order to extract the equivalent channel dimensions from experimental data, we have to extract the process and device parameters. First, device parameters, such as threshold voltage are extracted from the transfer characteristics for all the test structures. Then, technology constant K (intrinsic gain) is extracted from transfer characteristics of the transistors with known dimensions (linear layout). Following conformal mapping technique we assume K of the linear layout transistor to be true for each partial linear sub-transistor of the ELT. In the first approximation, neglecting short and narrow channel effects, this value holds true also for the whole ELT. So, the extracted parameters are used as constants to calculate the equivalent *W/L* for a given ELT as in (7).

$$\frac{W}{L} = \frac{I_{ds}}{K \cdot V_{ds} \cdot (V_{gs} - V_{th} - \frac{V_{ds}}{2})} \quad (7)$$

where K is extracted from standard layout transistor transfer characteristics and average from 15 samples is used for further calculations; and V_{th} is extracted from the particular ELT transfer characteristic. All device and process parameters were extracted be means of linear extrapolation [16]. Further we analyse average equivalent channel dimensions over 15 samples. Figure 8 illustrates accuracy of the aspect ratio extraction.

On the plot A the comparison of the current over extracted aspect ratio of the annular gate transistor and of the similar feature standard layout transistor is shown; a transistor with similar *W/L* and *L* was chosen as a reference.

On the plot B the same comparison for a ringed source transistor is done. Here we observe significant discrepancy between ringed source layout MOS transistor and standard layout MOS transistor of the same length. This suggests that the effective length of the ringed source layout is influenced by corner and edge regions of this transistor. Additional comparisons on Fig. 8B demonstrate better fit with standard layout transistors with longer channel.

On plots C and D, the absolute error between characteristics of the annular gate and ringed source transistors to the correspondent standard layout transistors over 15 samples is demonstrated. The mean value is indicated in grey line with o-markers, and the $\pm 3\sigma$ curves are indicated in grey dashed lines. The difference between ELT characteristics and linear layout transistors characteristics is less than 10% for all 15 samples.

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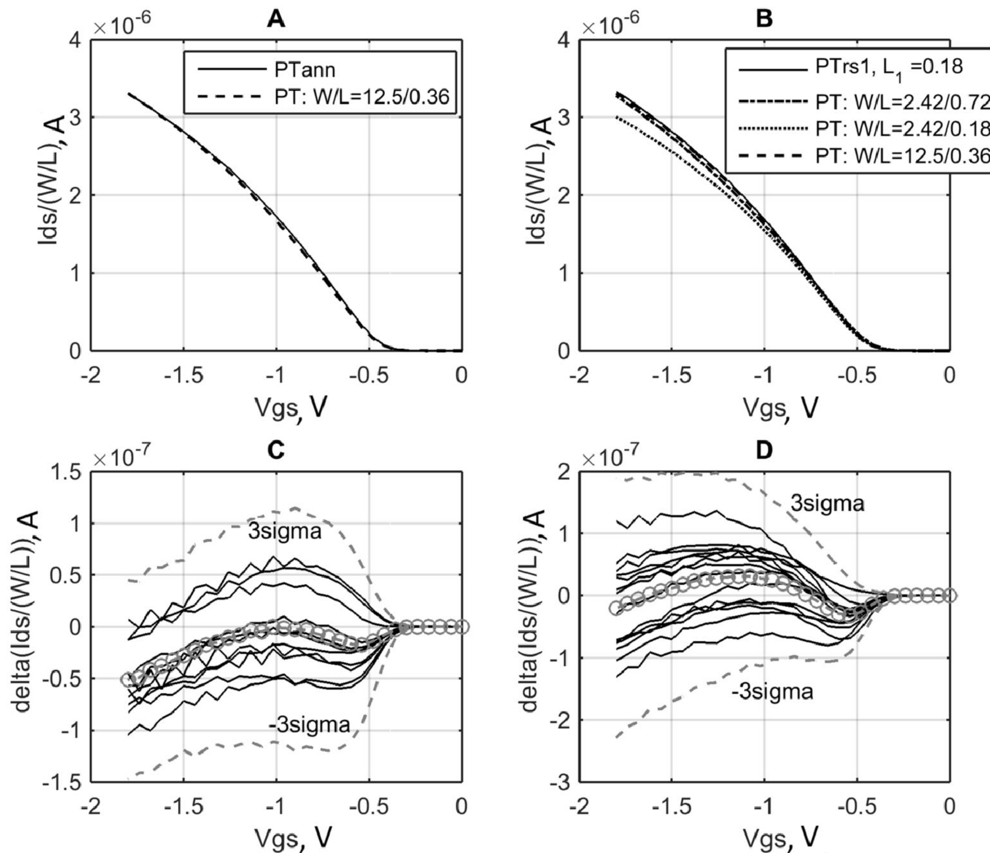

Fig. 8. Drain current (I_{ds}) at $V_{ds} = 0.05$ V over extracted aspect ratio as a function of gate-source voltage (V_{gs}) of annular gate and standard layout transistors (A), of ringed source and standard layout transistors (B); absolute error between Ids over extracted W/L of the standard layout PMOS with $W/L = 12.5/0.36$ and PTann (C) and between standard layout PMOS with $W/L = 2.42/0.72$ and PTrs1 (D) as a function of V_{gs} for 15 samples

Table 1. Equivalent channel dimensions of the annular gate transistors

Device name	Trapezoid *W/L*	*W/L* after [12]	*W/L* after [10]	*W/L* after [11]	*W/L* mid-line	Extracted *W/L*
PTann	34.7	36.2	36.2	34.5	35.1	31.6
PMann	17.9	22.6	19.3	19.9	18.6	17.2
NTann	34.7	36.2	36.2	34.5	35.1	34.9
NMann1	6	6.7	6.7	7.9	7.0	6.9
NMann2	8.9	11.0	13.4	11.7	10.8	12.3
NMann3	13.9	12.9	15.3	13.1	12.9	13.8

5. Results and discussion

We have applied the described above models and methods to the test structures. The results are summarized in Table 1 (for annular gate devices) and Table 3 (for ringed source devices).

All considered models deliver acceptable results for some transistor sizes and geometries. However, not all are universal. The model after [10] is most suitable for small feature devices, but loses the accuracy as the device scales up. It is also not universal for different device geometries. In this study, the original model had to be adjusted; this adjustment may not be optimal and could have influenced the result. The model after [12] is optimized for square device, and thus does not take into account the broken corner. The model after [11] relies on empirical coefficient (in our case 0, whereas the authors of [11] propose a value between 1 and 2), which is obviously technology dependent. The mid-line approximation is a trade of between accuracy and simplicity. It is still not suitable for sensitive designs, where accuracy better than 3% is required. The trapezia transistor approximation used by us in the design phase is very accurate for transistors with high *W/L*, but not reliable for small feature transistors. The relative error of *W/L* estimation related to extracted *W/L* is presented in Table 2.

For the ringed source devices, accuracy of the considered models strongly depends on the drawn length of the transistor (L1 in Fig. 6). Also, Ramos-Martos model [14] has a better fit for large devices, than for small, whereas Nowlin model [13] fits better for the smallest feature size thin oxide devices (where also lower channel length is possible). Calculations after [14] rely on empirical coefficients; by adjusting these coefficients, a better fit can be found. This, however,

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Table 2. Relative error in the *W*/*L* estimation related to extracted *W*/*L*

Device name	Trapezoid *W*/*L*	*W*/*L* after [12]	*W*/*L* after [10]	*W*/*L* after [11]	*W*/*L* mid-line
PTann	+0.6%	−14.4%	−14.3%	−2.8%	−11%
PMann	−4%	−31.9%	−12.3%	−15.8%	−8.6%
NTann	+0.6%	−3.7%	−3.5%	+1.24%	0.5%
NMann1	+13.6%	+3%	+3%	−13.2%	−1.4%
NMann2	+27.8%	+10.2%	−9.3%	+4.3%	+11.8%
NMann3	−0.4%	+6.3%	−10.7%	−1.8%	+7%

Table 3. Equivalent channel dimensions of the ringed source transistors

Device name	*W*/*L* after [14]	*W*/*L* after [13]	Extracted *W*/*L*
PTrs1	4.9	4.6	4.3
PTrs3	42.9	39.4	38.6
PM1rs	2.7	2.4	2.9
PM3rs	26.3	22.1	25.7
NTrs1	4.1	4.6	4.5
NTrs2	8.6	7.7	8.2
NTrs3	42.9	39.4	43.5
NMrs1	2.1	1.9	2.3
NMrs2	4.5	3.3	4.1
NMrs3	19.3	16.2	19.9

could solve the problem only for a particular technology with its specific design rules. So, as until now, there is no universal model for ringed source transistor equivalent channel dimensions calculation.

The inaccuracy of the calculations for the single drain devices can be explained by the significant contribution of the "edge" transistor, meaning further adjustment of W3 and L3 (Fig. 7) is needed – it is possible that the region right-hand to the source is also active to some extent. For the double-drain transistor this effect should already be included. However, here the opposite current directions within the device might cause the discrepancy between the physical behaviour and the geometrical calculations, because of anisotropy of the silicon crystal on which the IC is fabricated. These are the aspects that have to be investigated further.

6. Conclusions

In this work we have analysed different geometrical approaches to equivalent channel dimension estimation of ELTs. We have compared results of the state of the art analytical formulas with empirically extracted equivalent channel dimensions.

The empirical extraction of the equivalent channel dimension can be used as reliable evaluation reference for the analytical models. Still, its accuracy depends on the accuracy of the process and device parameters extraction, used in calculations, such as threshold voltage and intrinsic gain.

The critical point in the calculation of the annular gate transistors equivalent channel dimensions are the corners. Most of the models correct for them with help of empirical coefficients, which may not be true for every technology and device geometry. The simple methods, such as the newly proposed equilateral trapezoid transistors and mid-line are robust against technology influence, but are accurate only for devices with high *W*/*L*.

For the ringed source, accuracy of both models depends strongly on the drawn length of the transistor: the smaller the length, the more accurate the estimation. Additionally, the influence of the third, edge transistor part has to be considered. For the double-drain, the influence of the current direction has to be investigated further and possibly taken into account in modelling.

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