Elektrotechnik & Informationstechnik (2018) 135/1: 69–75. https://doi.org/10.1007/s00502-017-0569-0

Design and theoretical comparison of input ESD devices in 180 nm CMOS with focus on low capacitance

A. Michalowska-Forsyth, P. Schrey, B. Deutschmann

With the last decade's advances in sensor technologies and packaging techniques, there are several applications where the input capacitance and the leakage current of the integrated circuit (IC) front-end limit the readout accuracy of sensor systems. In particular, optimization of the electrostatic discharge (ESD) protection devices at the IC input could improve performance. Specifically, such optimization should involve reduction of parasitic capacitance and leakage current while maintaining the ESD robustness. Several ESD devices have been analyzed against input capacitance, leakage current and robust ESD performance. The first device of interest is a diode, as the simplest solution and then there are three MOS transistor based devices, gate-grounded NMOS (GGNMOS), gate-coupled NMOS (GCNMOS), and substrate pump NMOS (SPNMOS). The target fabrication process is 180 nm CMOS. Theoretical analysis of capacitance simulated with Cadence® in 180 nm CMOS design kit including layout extracted parasitics in combination with TCAD Sentaurus® simulations of current density and temperature is presented for selected ESD devices.

Keywords: electrostatic discharge; integrated circuit; robust; ESD diode; GGNMOS

Design und theoretischer Vergleich von ESD-Schutzstrukturen in 180 nm CMOS mit Schwerpunkt auf geringen Eingangskapazitäten.

Mit den Fortschritten des letzten Jahrzehnts in Sensor- und IC-Package-Technologien gibt es vermehrt Anwendungen, bei denen die Eingangskapazität und der Leckstrom des integrierten Schaltkreises (ICs) die Auslesegenauigkeit von Sensorsystemen begrenzen. Eine entsprechende Optimierung der Schutzstrukturen gegen elektrostatische Entladungen (ESD) an den Eingängen der ICs könnte die Performance verbessern. Eine solche Optimierung sollte insbesondere eine Verringerung der parasitären Kapazität und des Leckstroms beinhalten, während die ESD-Robustheit beibehalten wird. Mehrere ESD-Schutzstrukturen wurden auf ihre Eingangskapazität, ihren Leckstrom und die Robustheit gegen ESD analysiert. Die erste Schutzstruktur, die untersucht wurde, war eine Diode, die als einfachstes Schutzelement gilt. Des Weiteren wurden drei auf MOS-Transistoren basierende Schutzstrukturen, nämlich gate-grounded NMOS (GGNMOS), gate-coupled NMOS (GCNMOS) sowie substrate pump NMOS (SPNMOS) analysiert. Alle Schutzstrukturen basieren auf einem 180-nm-CMOS-Prozess. Die theoretischen Analysen der mit Cadence® simulierten Kapazitäten sowie die durch das Layout extrahierten Parasiten werden in Kombination mit TCAD Sentaurus®-Simulationen von Stromdichte und Temperatur für ausgewählte ESD-Schutzstrukturen vorgestellt.

Schlüsselwörter: elektrostatische Entladung; Integrierte Schaltung; Robustheit; ESD-Schutz; GGNMOS

Received September 15, 2017, accepted November 26, 2017, published online January 10, 2018
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1. Motivation and methods

ESD protection devices shield integrated circuit from damage during an ESD event. Although the most powerful events should be typically handled by the system-level off-chip protection device, but ESD protection concept is obligatory already at the component-level (Fig. 1). ESD robustness is characterized by applying standardized tests [1]. These tests differ for components and systems. On the one hand, component-level ESD tests evaluate if a single component, e.g. an IC, is able to withstand fabrication, package, handling, and assembly. The device under test (DUT) in a component-level test is not powered. Hence, malfunctions cannot be detected and component-level tests cover physical damage, so called hard failures only. On the other hand, system-level ESD tests aim to detect any malfunction of an electronic system, e.g. mobile phone. These are not restricted to hard failures and include any disturbance of operation like an unintentional reset or display black-out. These failures are known as soft failures. System-level ESD tests usually feature more power than component-level ESD tests and are the more challenging threat [2].

IC internal ESD protection has to pass component-level ESD tests. Due to the ongoing trend of integration, system engineers start asking for ICs robust against system-level ESD tests. This would safe board area and costs. But IC designers cannot qualify their products right from the beginning according to system-level ESD standards as they usually do not have any information on the final system during the concept and design phase of the IC.

Each input/output (IO) pin of an integrated circuit must be protected. The ESD pulse energy as well as its transient shape will largely vary depending on the circumstances [3]. ESD device should be de-

Michalowska-Forsyth, Alicja, Graz University of Technology, Institute of Electronics, Inffeldgasse 12/I, Graz 8010, Austria (E-mail: alicja.michalowska@tugraz.at); **Schrey, Patrick,** Graz University of Technology, Institute of Electronics, Inffeldgasse 12/I, Graz 8010, Austria; **Deutschmann, Bernd,** Graz University of Technology, Institute of Electronics, Inffeldgasse 12/I, Graz 8010, Austria

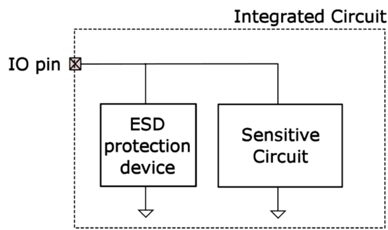

Fig. 1. IC IO pin protected by on-chip ESD device

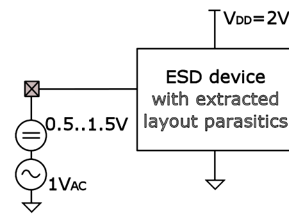

Fig. 2. Simulation circuit for obtaining input capacitance contributed by ESD device at IC operating condition

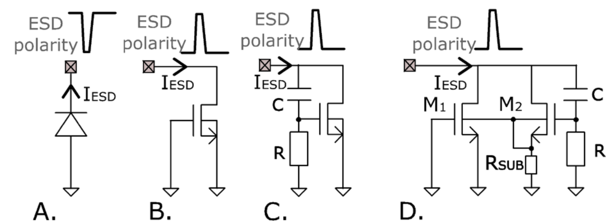

Fig. 3. Schematics of ESD devices optimized and designed in 180 nm CMOS design kit with indication of ESD event polarity considered in the simulations: (A) diode, (B) GGNMOS, (C) GCNMOS, (D) SPNMOS

signed for low on-resistance to handle large currents and for large spread of pulse rise times in case of edge-triggered devices to maintain ESD-functionality over a wide range of potential ESD events. For electrical characterization an extended Wunsch-Bell characteristic acquired with transmission line pulse (TLP) is recommended, an approach is summarized in [4]. It helps in identifying the ESD pulses types that the device under test can handle. The method uses a parameterized trapezoidal test pulse of variable duration, amplitude and rise time. For compliance between the computer-aided design (CAD) verification and measurement results, a TLP model is used as the input signal both in Cadence (IC design and verification environment) and in TCAD Sentaurus (suite of tools to simulate device characteristics including various physical processes).

This work focuses on on-chip component-level ESD protection devices and in particular on applications, where the input capacitance is important. In case of, for example ultra-wideband data transmission and radio technology [5, 6], microwave communications, ultrasound imaging [7], oscilloscope probe amplifiers or radiation detectors [8, 9], the parasitic capacitance at the input pin can dramatically degrade performance [10]. These applications involve signal sensing and processing, therefore low noise is a key parameter in the above examples. Meanwhile gain and noise are parameters particularly sensitive to input capacitance. By adding an on-chip ESD protection at the input sense-port, unwanted parasitic capacitance and leakage current are added. The presented investigation is addressing demands set by wide-band sensor applications. It focuses on optimizing the input ESD protection devices with respect to their ESD robustness and minimized parasitic capacitance and leakage current. Furthermore, it is desired that the ESD protection device parasitics do not change over the lifetime. This is particularly important for radiation detectors, where the interaction of X-rays or ionizing particles with the IC can increase parasitic leakage currents, leading to increased power consumption or shift in DC operating point.

Over twenty ESD protection devices of different types and dimensions have been designed in 180 nm CMOS IC process. The test-chip fabrication is planned in order to deliver experimental data from ESD stress. Cadence IC design and verification environment and TCAD Sentaurus finite element simulation suite for semiconductor devices were employed in the optimization process. Advantages of this approach have been demonstrated in [11]. Although it is difficult to get reliable device response to an ESD event with TCAD Sentaurus, the software can be used to identify the compromises in device layout, spacing and to evaluate the differences in ESD performance between different device types (diode-based, NMOS-based, etc.). Once the test-chip is fabricated, the ESD performance will be characterized experimentally, primarily with TLP tests. Independently also device capacitance will be measured. Consequently it will be possible to evaluate the ESD current to input capacitance ratio (I/C) for different ESD devices. A device with high I/C ratio is capable to conduct large ESD current while being almost transparent to other circuits thanks to its low parasitic capacitance.

Cadence was used to design the physical layout of the ESD protection devices, to optimize R-C time constants (if relevant), and to determine the parasitic input capacitance. The parasitic input capacitance is obtained from AC simulation at a given DC operating point including the layout-extracted parasitic capacitance, as shown in Fig. 2.

ESD structures discussed in this paper are depicted in Fig. 3. Details on the operation of diode, GGNMOS and GCNMOS as ESD devices can be found in [12], while operation of the SPNMOS is covered and further referenced below in this work. The paper is organized as follows: in the next part the optimization of a diode (Fig. 3A) as ESD device is presented. Afterwards optimization of a GGNMOS (Fig. 3B) and its upgrades to GCNMOS (Fig. 3C) and SPNMOS (Fig. 3D) ESD protections, are discussed. In both cases a summary of device geometries and capacitances are given. Consequently, at the end the results are analyzed and devices performance is compared in terms of I/C. It should be noted, that these devices are optimized for one-directional ESD protection. This means the diode is investigated for negative ESD events only, while GGNMOS, GCNMOS, and SPNMOS are subject to positive ESD events only. However, GGNMOS, GC-NMOS and SPNMOS can act as ESD protection in both directions, where the parasitic drain-bulk diode provides protection in case of the negative ESD event.

2. Diode: stripe, square or octagonal

The diode is a simple ESD protection and significantly less sensitive to voltage stress compared to MOS transistor-based protections with ultra-thin gate oxide. During normal operation, the ESD input-to-ground diode is reverse-biased, but under ESD event it becomes forward biased and provides a path to ground for the ESD current. Its ESD performance relies on the geometry-dependent current density distribution. Due to the positive temperature coefficient of silicon's electric conductivity, regions in silicon with increased temperature conduct more current and the temperature increases even further. This forms a positive feedback known as thermal runaway. As the current density is not perfectly uniform along the device edge, at high current densities this positive feedback may lead to local formations of current filaments in the diode. Consequently a local in-

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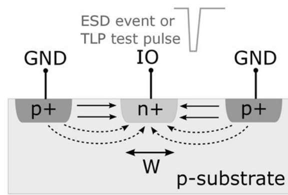

Fig. 4. Cross-section of N+ in substrate ESD diode indicating the preferred, low resistance current path under negative ESD event (*continuous arrows*)

Table 1. Three diode layouts: linear, square and octagonal with respective geometric parameters: perimeter and area

	A) Linear	B) Square	C) Octagonal
Perimeter	$P_l = 2a$	$P_s = 4a$	$P_o = 4a - 8x + 4 \cdot x\sqrt{2}$
Area	$A_l = w \cdot a$	$A_s = a^2$	$A_o = a^2 - 4 \cdot \frac{1}{2}x^2$
P/A	$\frac{P_l}{A_l} = \frac{2}{w}$	$\frac{P_s}{A_s} = \frac{4}{a}$	$\frac{P_o}{A_o} = \frac{4a-8x+4 \cdot x\sqrt{2}}{a^2-4 \cdot \frac{1}{2}x^2}$

crease in temperature eventually reaches the meltdown point and leads to destruction. Therefore, uniform current density distribution and minimized on-resistance along the current path are the main issues in optimizing any semiconductor-based ESD device. The ESD current through a diode will flow along the path of least impedance. As a result, the current concentrates along the diode edge on the surface, as the cross section in Fig. 4 (continuous arrows) shows, rather than deeper in the bulk (dashed arrows).

Optimization of the I/C parameter of ESD diode is intended to maximize the perimeter and at the same time aiming as low as possible capacitance of the reverse-biased N+ region in the normal circuit operation for a near-transparent ESD protection.

Table 1 summarizes the three variants of diode layouts considered: linear, square, and octagonal. Assuming that most of the current is concentrated at the diode's edges, the perimeter to area ratio P/A should be maximized. Consequently large I/C parameter should be obtained for diode ESD device with large P/A ratio. From the geometries shown in Table 1, the linear layout is the least advantageous due to its smaller P/A ratio, while the square diode has the highest P/A ratio. Additionally, the P/A ratio gets better for smaller square diodes.

This analytical statement was verified with TCAD Sentaurus simulations. A two-dimensional diode model, shown in Fig. 4, has been implemented. This two-dimensional diode model matches the cross section of any of the three analyzed diode structures in Table 1. The width of the N+ region was set as the simulation parameter and a TLP-like trapezoidal current pulse was applied to the N+ region. Figure 5 shows the obtained current density distribution for N+ region widths of 0.2 µm, 0.6 µm, and 1.2 µm. The TLP current was scaled with the width of the N+ region to 1 mA, 3 mA, and 6 mA, respectively. In all cases the highest current density is at the edge of the N+ region, as expected. A fraction of the current reaches deeper into the N+ region, though it becomes less significant for larger diodes. However, in case of the smallest diode, where the opposite edges come close together, effectively the volume under the N+ region

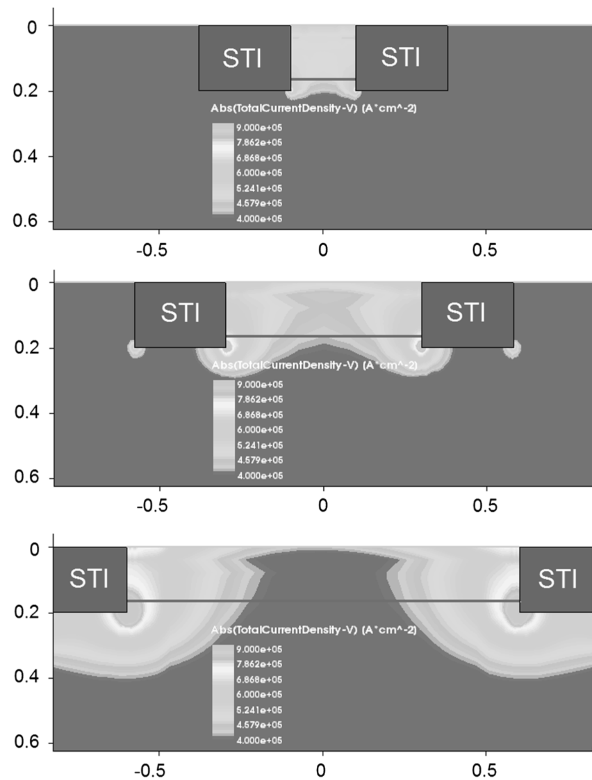

Fig. 5. Cross section of N+ in substrate diode, with N+ width set to: (A) 0.2 µm, (B) 0.6 µm and (C) 1.2 µm implemented in TCAD Sentaurus. Simulation result of current density at the plateau of TLP-like current pulse scaled with the N+ width: (A) 1 mA, (B) 3 mA, (C) 6 mA

contributes to current conduction. This geometry better exploits the IC layout area used for the N+ region, associated with capacitance. In order to achieve good ESD performance with large current capability, a complete ESD device is composed of multiple tiny diode segments. Up to now, the ESD performance only was investigated, while the capacitance was not considered. Nevertheless, the simulation result from Fig. 5 shows that the geometrical optimization of diode P/A ratio is not necessarily equivalent to optimization of the electrical I/C parameter.

Having found the properties of current density distribution at the diode cross section level, a TCAD Sentaurus 3D simulation of a N+ in substrate diode has been performed. This time, the optimization was targeting selection between the square and octagonal layout in Table 1. For this purpose the corner cut was introduced as a parameter with values between 0.1 and 0.5, meaning this fraction of the side-wall of the square diode was cut at the corner forming an octagonal diode. Results of this simulation for three different widths, 0.2 µm, 0.4 µm, and 0.6 µm, are shown in Fig. 6. The ESD current was set to 1 mA, 2 mA, and 3 mA. In case of the geometries with large N+ width, it is clearly observed that the edge cut can bring significant improvement, restricting the temperature increase. However with decreasing N+ width the advantage of octagonal shape fades.

In case of the CMOS IC process used in this design, the minimum width of the N+ region, given by the design rules, was in between the simulated values. This also meant that tailoring of the edges to get octagonal shape is not possible, as N+ region size approaches the design rules limits.

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Table 2. Summary of designed ESD protection diodes (N+ in substrate). The capacitance was obtained with Cadence environment including parasitics from the layout extraction

Diode	Segment geometry	No. of segments	Total N+ perimeter	Total N+ junction area	Capacitance at 10 kHz, 1 V
1	0.4 μm × 20 μm	4	163 μm	32 μm^2	107 fF
2	0.4 μm × 0.4 μm	200	320 μm	32 μm^2	166 fF
3	0.84 μm × 0.84 μm	45	151 μm	31.75 μm^2	37 fF
4	1.72 μm × 1.72 μm	11	76 μm	32.54 μm^2	31 fF
5	0.4 μm × 0.4 μm (doubled N+ spacing)	200	320 μm	32 μm^2	157 fF

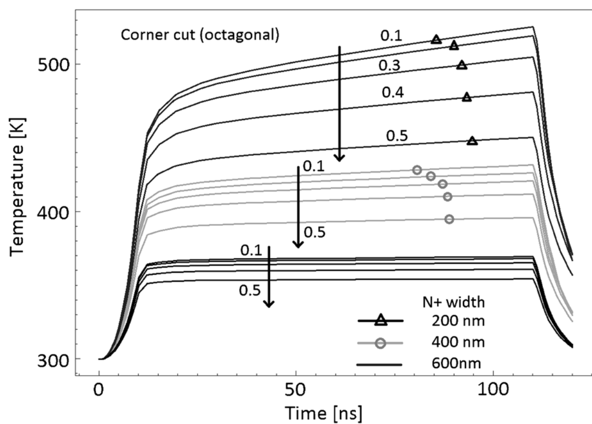

Fig. 6. Simulation results of the edge-cut-parameterized (0.1 to 0.5) 3D octagonal diode with TCAD Sentaurus – maximum temperature during a 100 ns long ESD event for different widths of the N+ region: 0.2 μm, 0.4 μm, and 0.6 μm, with the corresponding ESD current of 1 mA, 2 mA, and 3 mA

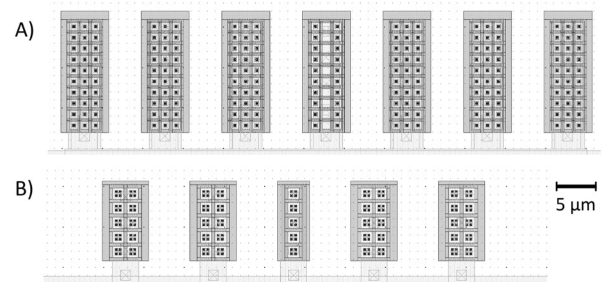

Fig. 7. Layout view of square diodes: (A) Diode 2 (0.4 μm width, 200 segments) and (B) Diode 3 (0.84 μm width, 45 segments)

For the planned IC test chip submission, several diodes were designed with dimensions summarized in Table 2. The linear diode 1 is the reference device. All other ESD devices are designed to have the same total N+ area of 32 μm^2 at the ESD input node. The layouts of diode 2 and diode 3 are shown in Fig. 7. The total number of segments in diode 3 is five times smaller than in diode 2, due to the difference in single segment geometry.

The capacitances obtained with Cadence simulations including the layout extracted parameters of designed ESD devices show large variation despite identical N+ areas. Diode 2 with the smallest width has the largest capacitance. This is related to considerable sidewalls capacitance of a large perimeter diode. Therefore, despite the highest current capability for the same N+ area, the I/C ratio might not be the best. A similar effect was reported in [13]. Nevertheless, if the perimeter translates to ESD current capability then I/C of the smallest square diode would still be better than I/C of the linear diode. The best candidate might be diode 3 – the square diode with 0.84 μm width. Any further increase of the diode width brings large reduction of perimeter without significant capacitance reduction (the N+ area is kept constant for a reasonable comparison).

TCAD simulations of diode 2 give a maximum ESD current of 10 mA/segment, or 2 A for the 200 segments. This allows estimation of the ESD robustness against standardized qualification tests, like the Human Body Model (HBM) according to IEC 60749-26:2013. The robustness is usually given as the maximum pre-charge voltage of the stress generator. In case of diode 2, HBM is estimated to carry 0.67 A/kV current. Thus, the expected ESD robustness for this diode would be up to 3 kV. However, these results might be far off from the planned measurement, since the TCAD Sentaurus setup was not calibrated with the real process data. The TCAD simulation results presented in this work are only used for optimization of potential solutions, rather than getting the actual value of the maximum ESD current or ESD robustness.

3. NMOS-based ESD structures

In case of diode ESD protection, current is conducted close to the silicon surface. This results in a higher local current density than in ESD devices where the current flows deeper inside the substrate. Current conduction deeper inside the substrate can be achieved using the bipolar effect, for example triggering the parasitic NPN of an NMOS transistor. GGNMOS, GCNMOS, and SPNMOS operation is based on the bipolar effect. These devices are also interesting candidates for low capacitance input ESD protection. As a further advantage, it should be highlighted that NMOS-based protection can conduct ESD events with positive and negative polarities: positive ESD event via the parasitic NPN transistor, as well as negative ESD event via the N+ in substrate diode associated with drain. The previously discussed ESD diode requires addition of a complementary diode for such full protection.

GGNMOS (Fig. 3B) is typically built with multiple fingers. Its main drawback is that only some fingers might be triggered during an ESD event. There are two reliable ways to improve the operation; both are discussed in [14]. Firstly, gate bias can be used. Secondly, substrate bias can be applied. Gate bias is used in GCNMOS, substrate bias in SPNMOS, among others. Both improvements facilitate triggering the bipolar effect in all NMOS fingers simultaneously.

GCNMOS (Fig. 3C) highly relies on dynamic parameters of the transient pulse. Before the gate voltage is discharged by the resistance to ground, the MOS action dominates. When gate voltage is discharged by the RC network, MOS action fades but the ESD current is efficiently conducted by the bipolar mechanism of the parasitic NPN. However, for some ESD events with long rise times, the

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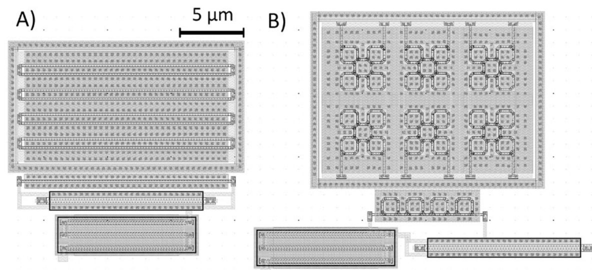

Fig. 8. Layout view of SPNMOS: (A) linear 8:1 and (B) enclosed 8:1

MOS action is prolonged. The high ESD current concentrates in the channel near the surface over a longer time and due to high local current density thermal damage may occur.

SPNMOS (Fig. 3D) is the third NMOS-based protection included on the test-chip. It is a combination of a large GGNMOS transistor (M1) and a much smaller substrate pumping GCNMOS transistor (M2). This device was originally proposed in [15]. The increase in M2 gate voltage initially triggers MOS action of M2 and sinks ESD current into the substrate. This leads to local increase in the substrate potential. Consequently, the base potential of the parasitic NPN transistor increases, triggering the bipolar action of M1. Therefore, even if the M2 MOS action is prolonged, the bipolar effect of the much larger M1 is fully on, ensuring safe operation for different current pulses. For the proposed test-chip several versions of SPNMOS were implemented with different ratios of M1 and M2: 16:1 and 8:1 (in terms of W/L dimensions), as well as with linear and with enclosed NMOS layout (both shown in Fig. 8).

2D TCAD simulations were performed in order to optimize the geometry of the cross section and electrical parameters for a wide range of ESD pulse rise times. Fig. 9 shows response to TLP pulses of rise time ranging from 0.1 ns to 10 ns. This spread should cover rise times of real ESD events [16].

Figure 10 shows the SPNMOS current density in response to the 10 ns rise time TLP. After 10 ns the channel is built under M2 indicating MOS action (Fig. 10A). At the end of the 100 ns long plateau the MOS action has vanished (Fig. 10B), since the M2 gate voltage has returned to zero volts (as shown in Fig. 9 waveforms). At this point in time both transistors M1 and M2 are in the bipolar mode, efficiently conducting the test-pulse current with low on-resistance.

For all discussed above NMOS-based ESD devices, the N+ drain area was designed to be 32 µm^2 like for diodes described in section 2. Table 3 summarizes the NMOS-based devices with their capacitance including parasitics from Cadence layout extraction. The summary includes also special-purpose ESD devices based on the enclosed-layout MOS transistors, for which the layout capacitance extraction was not possible, because of software limitations. Full comparison is thus left for future measurements on silicon.

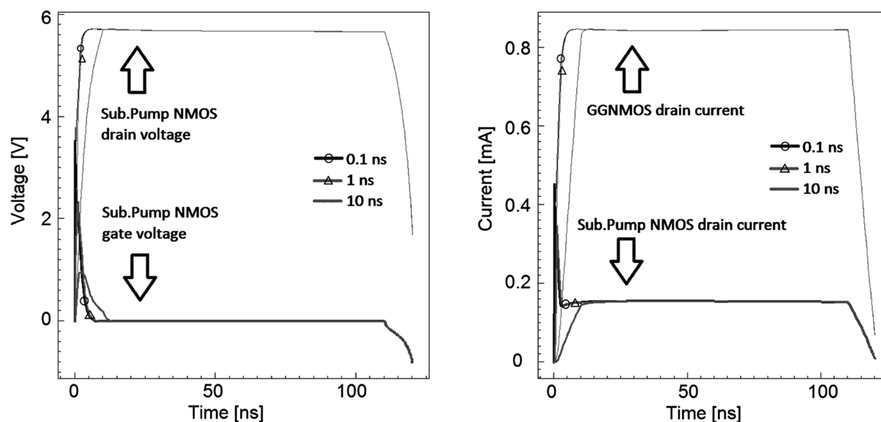

Fig. 9. SPNMOS response to 100 ns long TLP-like current pulse with 0.1 ns, 1 ns, and 10 ns rise times simulated with TCAD. *Left*: voltage waveforms at drain and gate of the substrate pumping NMOS (M2). *Right*: Drain currents through the GGNMOS transistor (M1) and through the substrate pumping transistor (M2). Total current 1 mA/µm of device width (Z-axis in Fig. 10) corresponds to maximum lattice temperature of 360 K

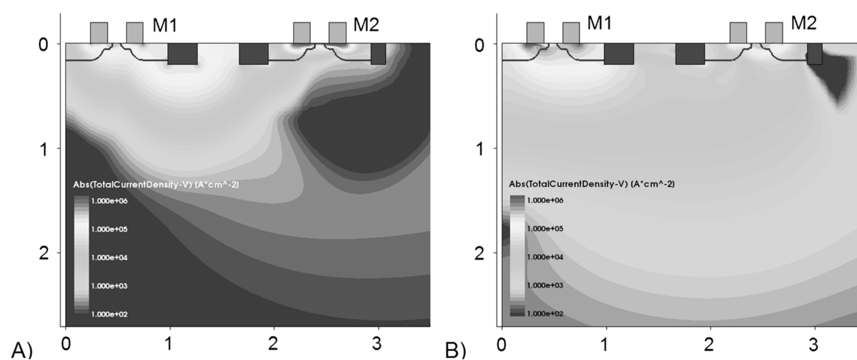

Fig. 10. SPNMOS response to 100 ns long TLP-like current pulse with 10 ns rise time simulated with TCAD. (A) At the beginning of 100 ns plateau with MOS action of M2, (B) At the end of the 100 ns plateau with bipolar action of M1 and M2

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Table 3. Summary of designed ESD NMOS protection devices (GGNMOS, GCNMOS and SPNMOS). The capacitance was obtained with Cadence including parasitics from the layout-extraction

NMOS	Type	No. of fingers	Total channel width	Total N+ junction area	Capacitance at 10 kHz, 1 V
1	GGNMOS enclosed A	8	130 μm	33.3 μm^2	–
2	GCNMOS linear	4	64 μm	16.6 μm^2	173 fF
3	GCNMOS linear	8	128 μm	33.3 μm^2	220 fF
4	GCNMOS enclosed A	30	130 μm	33 μm^2	–
5	GCNMOS enclosed B	30	132 μm	31.8 μm^2	–
6	SPNMOS 8:1 linear	8	132 μm	33.3 μm^2	250 fF
7	SPNMOS 16:1 linear	8	132 μm	33.3 μm^2	240 fF
8	SPNMOS 8:1 enclosed A	30	130 μm	33 μm^2	–

Table 4. Summary of designed ESD devices of different categories with simulated input capacitance (including layout parasitics) and with expected qualitative ESD performance

No.	(*) Devices of comparable area	(**) Input capacitance	Expected ESD performance
1	Diode linear	1	**+**
2	Diode square 2	1.6	**+ +**
3	Diode square 3	0.4	**+**
4	GGNMOS enclosed	–	**+ +**
5	GCNMOS linear	2.2	**+ + +**
6	SPNMOS linear	2.4	**+ + + +**

(*) Input N+ junction area equal for all devices

(**) Capacitance from circuit simulation including layout extracted parameters. Unit is arbitrary with the linear diode as reference.

4. Summary of the results and outlook

Over twenty ESD devices optimized for low capacitance have been designed in a 180 nm CMOS process. All of them have been designed with care that the number of drain contacts, number of top metal vias and metal interconnection width are similar. This minimizes the risk of failure at the metal level and gives more accurate comparison of the ESD performance. The selection includes diode-based and NMOS-based protection devices. The summary of key devices from each category is presented in Table 4. It shows the input capacitance obtained with Cadence simulation, including layout-extracted parasitics as well as the expected ESD performance improvements with respect to the linear diode. The latter is based on the literature studies and on TCAD Sentaurus simulation results.

The obtained results show that the small square diodes are promising candidates for the best I/C parameter. However as the diode of minimum feature size (diode 2) has considerable parasitic sidewall capacitance, diode 3 might be found to be a better candidate. NMOS-based devices have much larger capacitance, which is mainly related to the linear passive capacitor within the RC network of GCNMOS and SPNMOS. As in GGNMOS, there is no RC network and the capacitance is expected to be much smaller. However, the simulation of the enclosed-layout transistor (selected for special purposes) including the layout parasitics was not possible due to software limitations. Therefore, the capacitance of this device type has to be determined with measurements. Once the devices are available in silicon, ESD performance and capacitances will be characterized. Eventually an experimental evaluation the I/C parameter will be possible. As a final step, to obtain a complete ESD solution optimized for low capacitance, a protection circuit capable of conducting ESD current in both directions will have to be designed. It might mean further optimization of the NMOS-based structure in terms of N+ layout, in order to be robust also in case of negative ESD events. Otherwise involving a complementary diode to positive power supply (with P+ at the input node) or a PMOS-based protection structure, in addition to one of the evaluated low-side structures, might have to be considered.

5. Conclusions

Theoretical studies of low capacitance input ESD protection structures have been presented. The input capacitances have been determined with Cadence IC design environment including parasitics extracted from layout. The ESD robustness in terms of current capability has been evaluated using TCAD Sentaurus simulations. The devices considered are linear diode, square diodes of different sizes as well as three types of NMOS-based ESD protections. Even though the latter ones have much larger input capacitance comparing to diode-based solutions, their superior ESD current capability makes them also important candidates for the low capacitance input ESD protection. ESD performance characterization along with measurements of the capacitance, are planned once the samples are available.

Acknowledgements

Open access funding provided by Graz University of Technology.

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Authors

Alicja Michalowska-Forsyth
received her M.Sc. degree in electronic engineering at Lodz University of Technology in Poland in 2006. She has four years of experience as analog IC design engineer in the microelectronic industry. Her Ph.D. thesis (2013), realized in cooperation with CEASaclay and CNES-Toulouse in France, was oriented towards developing integrated read-out circuits for X-ray spectro-imaging. She currently works at the Institute of Electronics of Graz University of Technology, Austria, focusing on robust IC design.

Patrick Schrey
received his M.Sc. degree in electronics and advanced materials science from Graz University of Technology, Austria, in 2015. He is now working as a university assistant at the institute of electronics, Graz University of Technology towards his Ph.D. His research interests are transient disturbances in micro-electronics and electronic systems.

Bernd Deutschmann
has received his M.Sc. degree and the Ph.D. degree in telecommunication engineering from the Graz University of Technology, Austria, in 1999 and 2002, respectively. In 2006, he joined the Automotive Power EMC Center of Infineon Technologies AG, where he worked on the improvement of the EMC of ICs for automotive power applications. Since 2014 he has been with the Graz University of Technology, as a full professor with the Institute of Electronics. During his research activities, he has applied for several patents and has authored and co-authored numerous papers and technical articles in the field of electromagnetic compatibility of integrated circuits.

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