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Uniformity study of wafer-scale InP-to-silicon hybrid integration

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Abstract In this paper we study the uniformity of up to 150 mm in diameter wafer-scale III–V epitaxial transfer to the Si-on-insulator substrate through the O_2 plasma-enhanced low-temperature (300°C) direct wafer bonding. Void-free bonding is demonstrated by the scanning acoustic microscopy with sub-μm resolution. The photoluminescence (PL) map shows less than 1 nm change in average peak wavelength, and even improved peak intensity (4% better) and full width at half maximum (41% better) after 150 mm in diameter epitaxial transfer. Small and uniformly distributed residual strain in all sizes of bonding, which is measured by high-resolution X-ray diffraction Omega-2Theta mapping, and employment of a two-period InP–InGaAsP superlattice at the bonding interface contributes to the improvement of PL response. Preservation of multiple quantum-well integrity is also verified by high-resolution transmission electron microscopy.

1 Introduction

Progressive developments in the semiconductor industry since the invention of integrated circuits has resulted in high-quality mirror polished, flat large area semiconductor wafers which meet the requirements for good large-scale wafer bonding [1, 2]. Wafer-scale bonding is an at-

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tractive approach in hybrid integration for low-cost, large-throughput electronic and optoelectronic production. The hybrid silicon platform developed recently [3, 4] relies on the high-quality InP-based multiple quantum-well (MQW) active region transfer to the silicon-on-insulator (SOI) substrate through a low-temperature direct wafer bonding [5, 6]. Bonding uniformity over the entire bonded area is of great importance to ensure device yield and performance uniformity, particularly for dissimilar material bonding with different coefficient of thermal expansion. In this paper we study the direct bonding uniformity of 50, 100 and 150 mm in diameter InP-based as-grown epitaxial layers transferred onto the SOI substrate. Parameters of interest, including the distribution of interfacial void, strain, photoluminescence (PL) response, and bonding interface, are characterized by the high-resolution scanning acoustic microscopy (SAM), X-ray diffraction (XRD) wafer mapping, PL wafer mapping and transmission electron microscopy (TEM), respectively.

2 Experiment

Standard 100 and 150 mm in diameter (001) SOI wafers were used for mating with InP-based epitaxial wafers in 50, 100 and 150 mm diameters. Waveguide circuits and vertical outgassing channels [6] were patterned on the silicon-on-insulator (SOI) wafers prior to bonding process. The 150 mm in diameter III–V wafer contained a metallorganic chemical vapor deposition (MOCVD)-grown, diode laser structure with 8-period, compressively strained (1%), undoped InGaAsP quantum wells ($\lambda_g = 1.54$ μm) and doped InP layers. III–V wafers in smaller sizes are composed of the MOCVD-grown, undoped 2 μm InP and 100 nm InGaAs etch stop layers. Thorough wafer cleaning and the O_2 plasma surface activation are conducted, followed by mating at room temperature and anneal at 300°C with 1–2 MPa external coaxial pressure. Then the InP substrate is selectively removed in a wet etch, leaving ∼2 μm thick III–V epilayers on the SOI substrate with InGaAs etch stop layer on the surface. Detailed III–V epitaxial layer structure and bonding process can be found in [6, 7]. Figure 1(a) shows the photo of thin III–V epilayers with different size (1 cm^2, 50, 100, 150 mm in diameter) on the SOI, demonstrating >98% area transfer and mirror-like III–V surface with a typical root mean square (RMS) surface roughness of 0.6–0.7 nm [7]. Further device process proceeded on the 150 mm bonded sample. After putting a layer of 300 nm plasma-enhanced chemical vapor deposition (PECVD) SiN_x at 260°C, standard projection photolithography and dry etch patterned the racetrack ring laser layout with each device die (2×2 cm^2). Wet etch then removed surface InGaAs layer in exposed area, giving us access to PL response from the active region. No extra delamination is observed during thermal cycling and wet processing, indicating strong, robust III–V-to-Si bonding.

3 Results and discussion

Typically, we spot any interfacial voids after removing the thick InP substrate under the optical microscope in Normaski-mode whose resolution is good enough to resolve sub-μm voids. Void-free bonding is achieved in randomly selected area in all bonded wafers due to vertical outgassing channels [7] to absorb the gas byproducts (H_2O, H_2) from interfacial polymerization reactions and trapped N_2, CO_2, etc. [6]. Here we utilize the high-resolution SAM with sub-μm resolution (X-axis: 0.5 μm, Y-axis: 0.25 μm, Z-axis: 0.5 μm) to show the entire wafer-scale images of 50 and 100 mm bonded wafers in Fig. 2. Only are few relatively large voids (highlighted in red circles) were observed. They are close to the wafer edge and likely to be from surface particles during manual wafer handling. No uniformly distributed, gas byproducts-resulted voids are found, which is compatible with previous inspection in Normaski microscopy in selected areas [7]. Void-free bonding was observed in >99% of area. The misleading contrast and some vertical lines highlighted in SAM images in Fig. 2 are from the wafer chuck related to the SAM tool.

From a device point of view, preservation of designed active region after epitaxial transfer is most important to our interest. PL ($\lambda_{pump} = 532$ nm) maps measured at room temperature for the 150 mm InP MQW wafer prior to and after epitaxial transfer in Fig. 3 are compared to study the potential material gain change from bonding and thermal process. Average PL peak wavelength of 1539.6 nm, average peak intensity of 5.444 V and average spectrum full width at half maximum (FWHM) of 67.9 nm of the as-grown InGaAsP MQW epitaxial wafer are measured prior to the bonding. As mentioned before, the removal of the top InGaAs ($\lambda_g \sim 1.62$ μm) layer except the individual device die margin allows probing the true multiple quantum-well (MQW) luminescence data. The PL response from chip margin (i.e., PL response of the top InGaAs layer) is removed in the image and statistics for accurate comparison. Average PL peak wavelength, peak intensity and FWHM after bonding and initial device processing are 1540.4 nm, 5.666 V and 36.8 nm, respectively. Nearly no average PL wavelength shift is measured (left column), indicating the small residual strain. Peak intensity (center column) and FWHM (right column) are even improved by respective 4% and 41% after epitaxial transfer. Similar improvement has been reported in the InP-to-GaAs bonded sample with placing several periods of the InP-lattice-matched InGaAsP/InP superlattice at the bonding interface [8], which is also implemented in this work. It is believed that superlattice serves as a gettering site

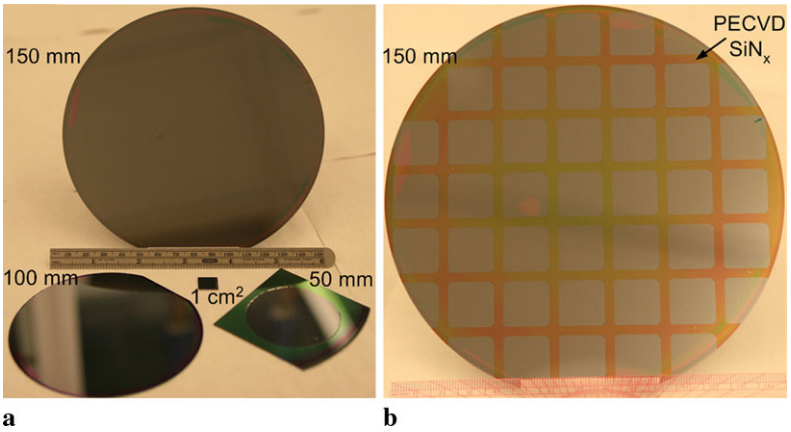

Fig. 1 (**a**) Photographs of the thin InP epi-layer of 1 cm^2, 50, 100 and 150 mm in diameter bonded on the SOI substrate. (**b**) Photograph of the processed 150 mm III–V-to-Si bonded wafer, showing individual device dies

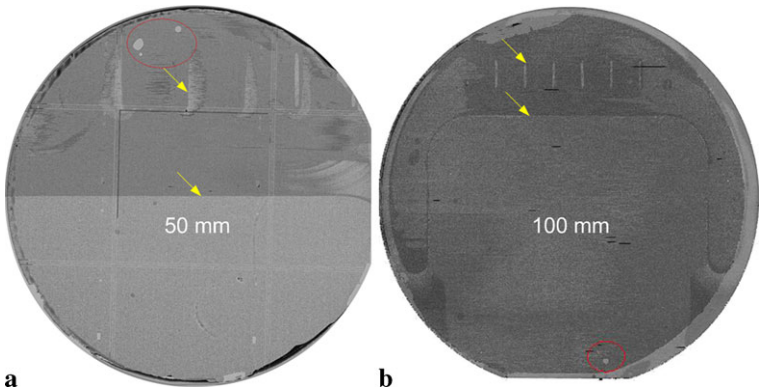

Fig. 2 SAM images of the (**a**) 50 mm and (**b**) 100 mm InP-to-Si bonded wafers. Interfacial voids are highlighted in *red circles* and *yellow arrows* to indicate the vertical scan lines and a pattern from the wafer chuck related to the tool

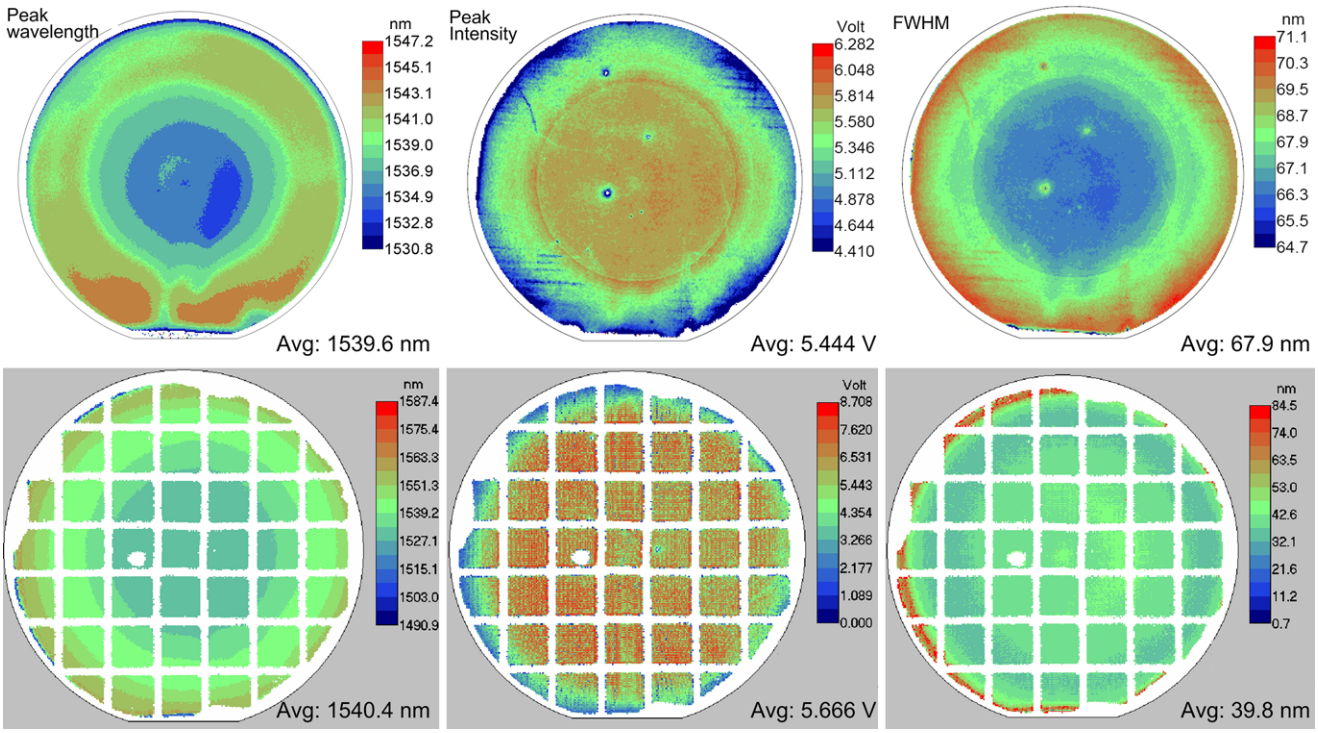

Fig. 3 Comparison of PL maps before (*top row*) and after (*bottom row*) epitaxial transfer. *Left column*: peak PL wavelength; *center column*: peak PL intensity; *right column*: FWHM. The margin between 2×2 cm^2 chips is removed in order to eliminate the error from InGaAs PL response in these areas

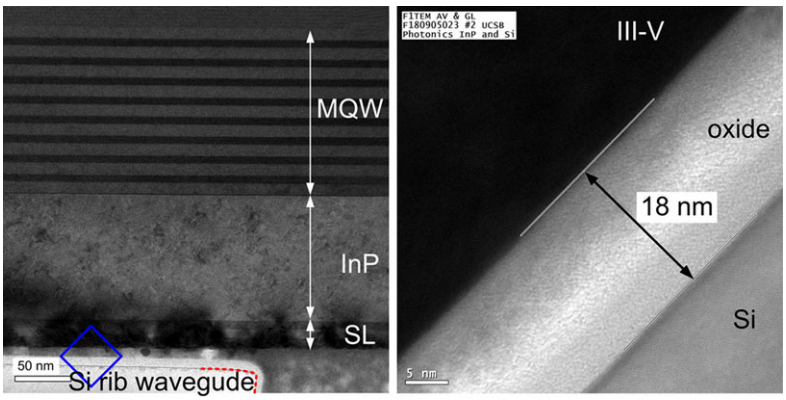

Fig. 4 (**a**) Cross-sectional TEM image of the transferred III–V MQW structure close to the Si waveguide rib edge (highlighted by *red dash line*). (**b**) High-magnification TEM image of *blue box* in (**a**), showing the 18 nm interfacial oxide, III–V and Si

for defects, in "competition" with the strained MQW region for defect and dopant aggregation [8]. The 300°C thermal annealing during the bonding process is well below the typical post-growth anneal temperature (>550°C) to cause annihilation of the as-grown defects for InP-based materials [9, 10] and it is also low enough to keep dopant diffusion constant extremely small to prevent dopant (e.g., Zn) entering undoped MQW [11]. It would be helpful to identify whether implementation of superlattice at bonding interface, rather than bonding anneal step or even introduced strain, solely accounts for this improvement, if a sister III–V wafer (i.e., grown simultaneously in the same reactor) was available for experiencing the same thermal cycle without any bonding process. It, however, is not practical in this work. Nevertheless, it is fair to say that the number of any bonding strain-induced defects formed or diffused into MQW has to be zero or less than that of any possibly annihilated growth defects as well. It is also verified by the high-resolution TEM images in Fig. 4. Good uniformity is visible in central area while degradation is concentrated on the periphery, starting from 10 mm to the edge, primarily due to the increasing shear stress upon bonding. The edge zone is normally excluded in practical device fabrication.

The cross-sectional TEM image in Fig. 4(a) shows no threading dislocations formed and penetrating into the MQW active region. Clear contrast between quantum wells and barriers results in small FWHM in Fig. 3. The lattice constant and crystal structure difference and the thermal expansion mismatch between InP (4.8×10^{-6}/K) and Si (2.6×10^{-6}/K) contributes to form interface defects, especially in the III–V contacting with Si waveguide 90° rib angle where the maximum stress is concentrated. It is, however, noted that two periods of InGaAsP/InP superlattice seem to pin the defects at the interface and prevent them from growing towards the MQW [8], which agrees with the comparison of PL in Fig. 3. Figure 4(b) is a close-up image of the bonding interface where a layer of 18 nm oxide composed of the native oxide of Si, In and P is sandwiched by the III–V and Si.

The high-resolution X-ray diffraction (XRD) rocking curve measurement was used previously to qualify the 150 mm in diameter MQW active region transfer. Comparing the simulated InP (004) Omega scan vs. experimental data measured at the *center* of the 150 mm InP epilayer before and after bonding, the InP main peaks and all MQW satellites are very well aligned, showing well-preserved quantum-well integrity [7]. A 17 MPa residual tensile strain was also obtained by measuring the wafer curvature, which is much smaller than the typical 200 nm PECVD SiO_2 or SiN_x-induced thin film stress in the order of 20–200 MPa [7]. In order to study the *global* wafer-scale strain distribution, a XRD wafer map technique is employed in this work to probe the lattice information of the transferred InP epilayer at different locations. The commercial software for the strain analysis of heteroepitaxy is used to combine individual 2Theta-Omega scans to make a strain matrix map. Since the strong bonding is resulted from a ∼18 nm thick bridging native oxides (Fig. 4(b)) of the InP and Si, no covalent bonds form between the InP and Si atoms directly. On the other hand, all bonding-induced strain should concentrate completely in the thin (∼2 μm) III–V epilayer after removing the InP substrate. Determining the shift of transferred 1.5 μm (in 150 mm wafer) or 2 μm (in 50, 100 mm wafers) InP peak position to its theoretical value therefore unfolds the strain picture. In order to construct a strain situation similar to the heteroepitaxial growth where epitaxial layers are not lattice-matched to the substrate exactly, the measured InP peak is labeled as the epitaxial layer peak while a fiducial InP substrate peak is manually placed at its theoretical train-free (004) 2Theta position of 63.3382°. The internal XRD tool error is corrected by offsetting the (004) Si peak measured from SOI substrate because the Si substrate does not affected by the bonding-induced strain.

Figure 5 exhibits the wafer map of offset between measured InP 2Theta peak and theoretical InP (004) peak for (a) 50 mm, (b) 100 mm and (c) 150 mm diameter bonding. The mean offset value for the 50, 100 and 150 mm bond are 0.04693°, 0.01037° and 0.08183°, respectively.

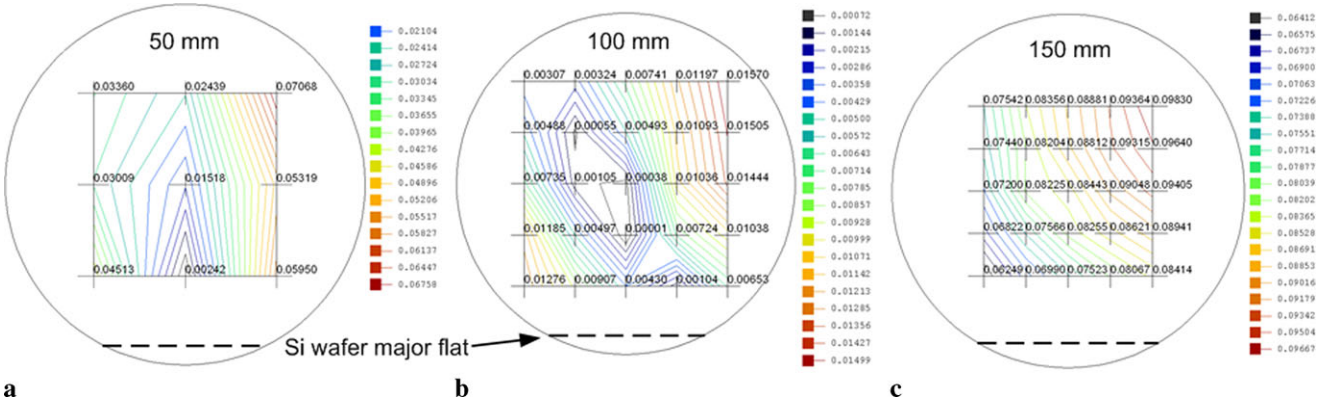

Fig. 5 Wafer maps of offset between measured InP 2Theta peak and theoretical InP (004) peak for (**a**) 50 mm, (**b**) 100 mm and (**c**) 150 mm diameter bonding. Offset value of each point is labeled. *Dash lines* indicate the major flat for the SOI substrates

The corresponding bonding-induced strain (d-spacing mismatch) are therefore only 662, 146 and 1154 ppm for 50, 100 and 150 mm bonding, all extremely small compared with typical strain engineering in the heteroepitaxy, for example 1–2% (10000–20000 ppm) lattice mismatch. Smaller strain observed in the 100 mm bond than those in the 50 and 150 mm is due to intrinsic smaller bowing in the 100 mm SOI wafer [12]. Both the 50 and 150 mm bonds are formed on the 150 mm SOI wafers with a larger bowing. The standard deviations of strain distribution are 0.012, 0.0035 and 0.011 for 50, 100 and 150 mm bonds, respectively, indicating excellent uniformity over the measured area. The different strain contours shown in Fig. 5 are correlated with the surface contour of the SOI substrate since the thin III–V epilayer is forced to conform to the thick SOI substrate after epitaxial transfer. Similar contours (data not shown) are noticed in the SOI substrate when Si (004) peak is detected.

4 Conclusion

In conclusion, we have studied the wafer-scale uniformity of InP-to-Si direct wafer bonding using the non-destructive scanning acoustic microscopy (SAM), the X-ray diffraction and the photoluminescence (PL) mapping techniques. Wafer-scale void-free bonding has been verified in the SAM. PL maps exhibit nearly no PL peak wavelength shift after bonding. The MQW gain and emission spectral purity are improved in the transferred epitaxial layers are probably due to combination effect of the negligible bonding-induced thermal strain, the InGaAsP/InP superlattice at the bonding interface, and the annihilation of the as-grown defects in bonding anneal process. Low bonding-induced strain is observed in the transferred thin III–V epilayers on SOI with diameter of 50, 100 and 150 mm, because of low-temperature anneal at 300°C where thermal stress of InP-to-Si bonding is smaller than critical stress for dislocation generation in the InP [13]. Uniform epitaxial transfer is also shown by demonstrating 0.3–1.2% global strain variation. The reported data here is a precondition for high-yield, wafer-scale manufacturing of hybrid silicon evanescent devices. This hybrid silicon process has been used to make the distributed feedback and distributed Bragg reflector lasers [14], mode locked lasers [15] and low threshold ring lasers [16].

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