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# Hybrid silicon evanescent approach to optical interconnects

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**Abstract** We discuss the recently developed hybrid silicon evanescent platform (HSEP), and its application as a promising candidate for optical interconnects in silicon. A number of key discrete components and a wafer-scale integration process are reviewed. The motivation behind this work is to realize silicon-based photonic integrated circuits possessing unique advantages of III–V materials and silicon-on-insulator waveguides simultaneously through a complementary metal-oxide semiconductor fabrication process. Electrically pumped hybrid silicon distributed feedback and distributed Bragg reflector lasers with integrated hybrid silicon photodetectors are demonstrated coupled to SOI waveguides, serving as the reliable on-chip single-frequency light sources. For the external signal processing, Mach–Zehnder interferometer modulators are demonstrated, showing a resistance-capacitance-limited, 3 dB electrical bandwidth up to 8 GHz and a modulation efficiency of 1.5 V mm. The successful implementation of quantum well intermixing technique opens up the possibility to realize multiple III–V bandgaps in this platform. Sampled grating DBR devices integrated with electroabsorption modulators (EAM) are fabricated, where the bandgaps in gain, mirror, and EAM regions are 1520, 1440 and 1480 nm, respectively. The high-temperature operation characteristics of the HSEP are studied experimentally and theoretically. An overall characteristic temperature ($T_0$) of 51°C, an above threshold characteristic temperature ($T_1$) of 100°C, and a thermal impedance ($Z_T$) of 41.8°C/W, which agrees with the theoretical prediction of 43.5°C/W, are extracted from the Fabry–Perot devices. Scaling this platform to larger dimensions is demonstrated up to 150 mm wafer diameter. A vertical outgassing channel design is developed to accomplish high-quality III–V epitaxial transfer to silicon in a timely and dimension-independent fashion.

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## 1 Introduction

Silicon is the second most abundant element on Earth, and has dominated the microelectronic industry for nearly a half century. Continuous technological advances in circuit design and device manufacturing enable complementary metal-oxide semiconductor (CMOS) chips with increasingly high integration complexity to be fabricated in an unprecedently scale and economical manner. Optical interconnects have also revolutionized telecommunications over the past few decades as single-frequency lasers, high-speed detectors, fiber optics and dense wavelength division multiplexing (DWDM), etc. open up the era of high-speed Internet. Behind the compelling impetus of lower manufacturing cost, higher performance and better energy efficiency, optical interconnects are favored as an alternative medium for data transmission in and between microprocessors. Larger bandwidth, lower power consumption (i.e., lower heat dissipation), smaller interconnect delays, and higher tolerance to

electromagnetic interference are attractive advantages over the conventional metallic (Cu and Al) electrical interconnects.

A large research effort has been invested worldwide high-quality, direct-bandgap compound semiconductors on silicon [1–5] in order to overcome the intrinsically poor light emission efficiency of crystalline silicon. The recently developed hybrid silicon evanescent platform (HSEP) [6, 7] represents one promising approach to equip active optical functionality onto silicon-on-insulator (SOI) substrates. Electrical injection lasers [6, 8–10], amplifiers [11, 12], photodetectors [13] and modulators [14–16] have been realized on silicon using this approach. More detailed reviews about this platform can be found in [17, 18].

In this paper we first review the key components needed to fulfill necessary functions of optical signal generation and external modulation in optical interconnects. Integrated hybrid silicon distributed feedback (DFB) and distributed Bragg reflector (DBR) lasers, and Mach–Zehnder interferometer (MZI) modulators and electroabsorption modulators (EAMs) are demonstrated. Quantum well intermixing (QWI) technique is also applied to this platform, enabling multiple III–V bandgaps for larger integration freedom. The studies on thermal performance of the devices are conducted experimentally and theoretically, revealing the high temperature operation perspective of HSEP. After the discussion of the device aspect for hybrid silicon optical interconnects, wafer-scale integration of III–V epitaxial layer to the SOI substrate is studied. Up to 150 mm diameter III–V-to-silicon epitaxial transfer is shown through an efficient, low-temperature wafer bonding process. The integrity of III–V multiple quantum well active region after the bonding process is characterized through X-ray diffraction photoluminescence measurements.

## 2 Integrated single-frequency light sources

Single-wavelength light sources are essential in WDM systems both for long-haul telecommunications and short-reach optical interconnects in silicon. Single wavelength sources can be multiplexed together to enable high aggregate bandwidth data links while their intrinsically small linewidth and phase noise reduce the signal crosstalk dramatically. The lasers discussed here have gratings patterned in the silicon waveguide using standard photo-lithography. Meaning the Bragg wavelength, cavity length, apodization and phase-shifts can all be defined on a single mask with all these parameters varying across a die. Grating-based laser cavity design enables excellent frequency stability and monolithic on-chip integration.

### 2.1 Hybrid silicon DFB lasers

Figure 1(a) shows a schematic device layout of a hybrid silicon DFB laser [19] with integrated photodetectors connected to both facets (only one shown). The III–V mesa region above the silicon waveguide consists of a 200 μm long gain region plus 80 μm long tapers. The tapers adiabatically transform the optical mode from the hybrid waveguide to the passive silicon waveguide allowing for losses on the order of 1.2 dB per taper and reflections on the order of $6 \times 10^{-4}$ [11]. The integrated photodetectors are 240 μm long including two 80 μm long tapers. A ∼25 nm deep surface corrugated grating with a 238 nm pitch and 71% duty cycle is formed on the silicon waveguide by electron beam lithography and dry etching. The grating stop-band is designed around 1600 nm in order to account for the spectral shift seen in previous devices due to device heating [20]. The silicon waveguide has a width, height, and rib etch depth of 1.5, 0.7, and 0.5 μm, respectively, resulting in a quantum well confinement factor of 5.2% and a silicon confinement factor of 59.2%. Figure 1(b) shows a cross-sectional scanning electron microscope (SEM) image of the fabricated device. The effective indices of the unetched and etched regions are calculated using the film mode matching method to be 3.3688 and 3.3441, respectively. This results in a $\kappa$ of $\sim$309 $cm^{-1}$. The $\kappa$ of these gratings are large when compared to the 91.81 $cm^{-1}$ $\kappa$ of surface corrugated gratings on silicon rib waveguides of similar dimensions since the index perturbation of air is quite large and the grating is located near the center of the mode. The grating is 340 μm long with a $1/4$ wavelength shift in the center in order to break the modal degeneracy.

The light–current ($L$–$I$) characteristics are measured on chip by collecting light out of both sides of the laser with integrated photodetectors. A 100% internal quantum efficiency of the photodetectors is assumed in order to conservatively assess the laser output power. Figure 2 shows a minimum lasing threshold of 25 mA with a maximum output power of 5.4 mW at 10°C. The maximum lasing temperature is 50°C. The lasing spectrum is measured by dicing off the right photodetector, polishing, and anti-reflection coating the silicon waveguide output facet. Light is collected with a lensed fiber into an HP spectrum analyzer with a 0.08 nm resolution bandwidth. The spectrum in Fig. 2 inset exhibits a lasing peak at 1599.3 nm with 30 mA injection current with a 50 dB side mode suppression ratio. Accurate spectral linewidth is measured by using the delayed-self heterodyne method [21]. A narrow linewidth of 3.6 MHz is observed (data not shown), which is a typical value for commercial III–V DFB lasers.

### 2.2 Hybrid silicon DBR lasers

In contrast to DFB lasers, the longer lasing cavity of DBR lasers reduces their thermal impedance and consequently en-

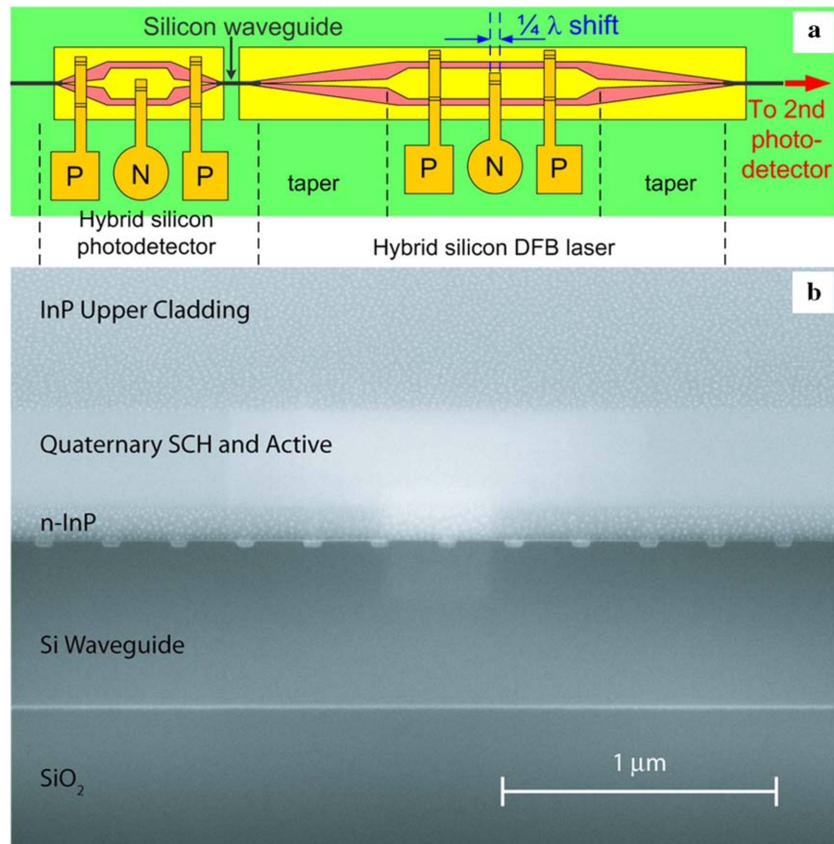


**Fig. 1** (**a**) Schematic layout of hybrid silicon DFB devices. (**b**) SEM image of longitudinal cross-section

hances their output powers. As shown in Fig. 3, the device layout includes two passive Bragg reflector mirrors placed 600 µm apart to form an optical cavity. As for the DFB lasers, two 80 µm long tapers sandwich the 440 µm long silicon evanescent gain region. The back and front mirror lengths are 300 and 100 µm long, respectively. The silicon waveguide has a width, height, and rib etch depth of 2, 0.7, and 0.5 µm, respectively. This results in silicon and quantum well confinement factors of 66% and 4.4% in the hybrid region. The surface corrugated gratings have an etch depth and duty cycle of 25 nm and 75%, respectively, with an upper cladding of SU8 leading to a grating strength, $\kappa$, of 80 $cm^{-1}$. The power reflectivities of back and front mirrors are calculated to be 97% and 44%, respectively.

The laser output power is measured with an integrating sphere at the front mirror of the laser. The front mirror $L$–$I$ characteristic is shown in Fig. 4. The device has a lasing threshold of 65 mA and a maximum front mirror output power of 11 mW, leading to a differential efficiency of 15%. Based on our estimations of the material and laser properties, calculations show that the taper loss of 1.2 dB [11] increases the threshold current by a factor of 2 due to the accumulated loss through four taper transitions in one round trip through the cavity. The laser operates up to a stage temperature of 45°C. The kinks in the LI are because longitudinal mode hop caused by the laser wavelength red-shifting due

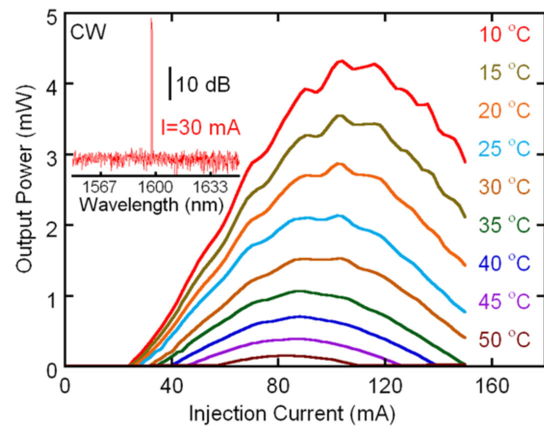


**Fig. 2** $L$–$I$ curve for stage temperatures of 10 to 50°C. *Inset*: The lasing spectrum at 30 mA injection current, showing a single-mode operation span over a 100 nm

to self-heating. The lasing spectrum is shown in Fig. 4 inset with a lasing peak at 1597.5 nm and 50 dB SMSR when driven at 200 mA.

Direct modulation characteristics of the device is studied by using a bias-T to drive the laser simultaneously with a DC bias current and an radio frequency (RF) signal while measuring the electro-optic (EO) response on a photodetector. Figure 5 shows the photodetected EO response of the laser under small signal modulation of −10 dBm. S11 mea-

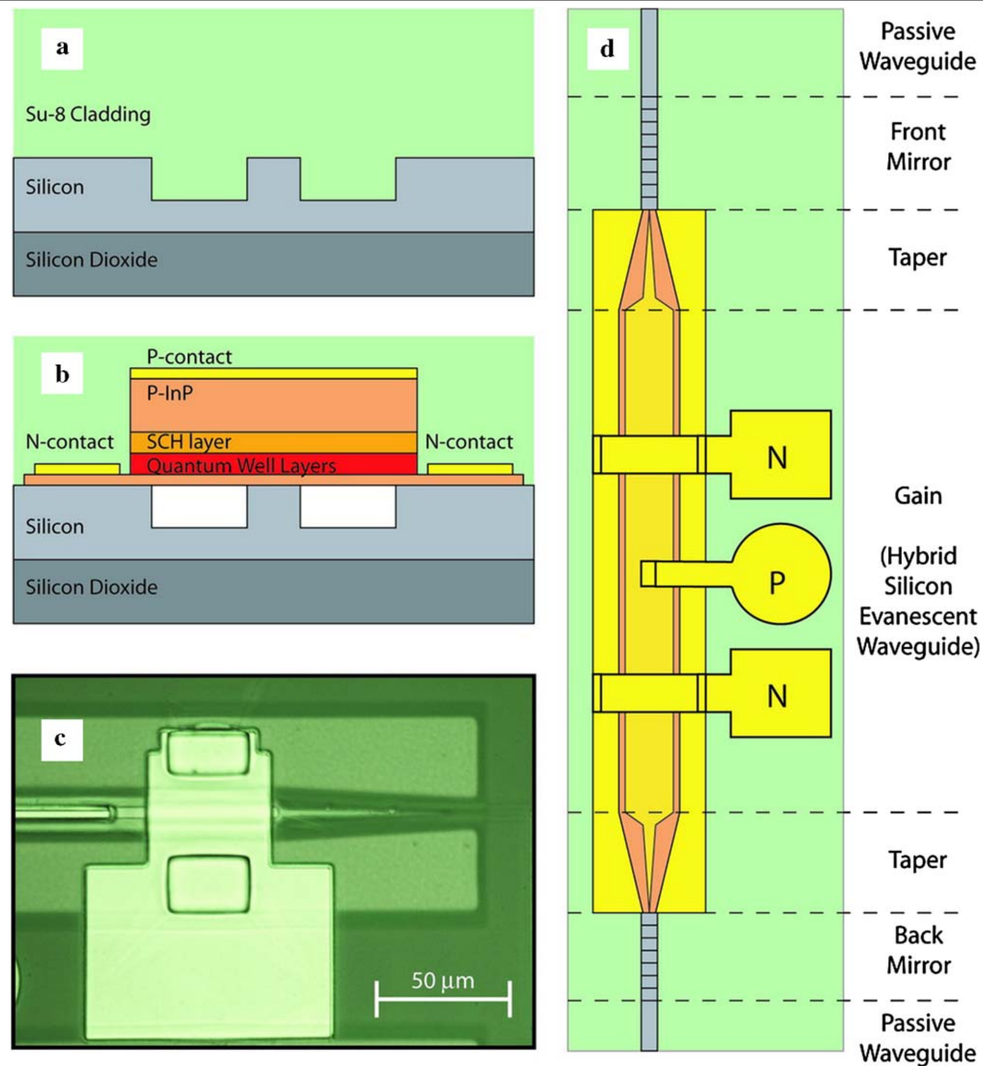


**Fig. 3** (**a**) Passive silicon rib and (**b**) Hybrid silicon evanescent waveguide cross-section; (**c**) Microscope image of a hybrid to passive taper; (**d**) DBR-SEL top-view topographical structure

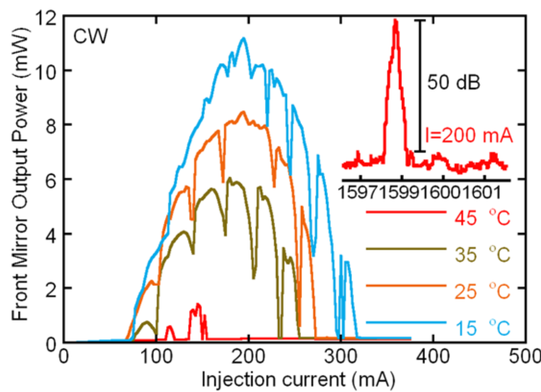


**Fig. 4** DBR laser $L$–$I$ curve for various temperatures measured out of the front mirror. *Inset*: The lasing spectrum at 200 mA injection current, showing a single-mode operation with 50 dB SMSR

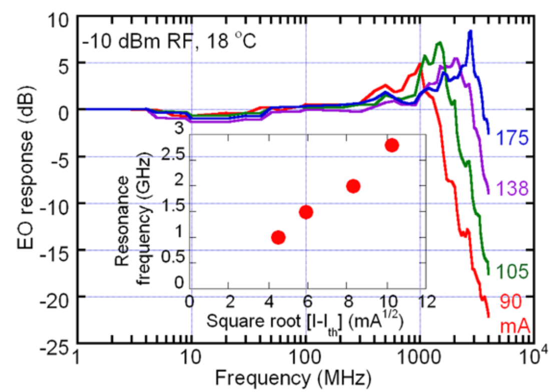


**Fig. 5** Photodetected frequency response of the DFB-SEL for 3 different bias currents with a stage temperature of 18°C and (*inset*) plot of resonance frequency versus the square root of current above threshold

surements indicate that the electrical contact geometry is not limiting the performance of the device, so reflected power has not been factored out of these curves. A 2 pF device capacitance was extracted from the S11 measurement, resulting in an RC limited bandwidth of 7 GHz. Figure 5 inset shows the resonance frequency versus the square root of DC

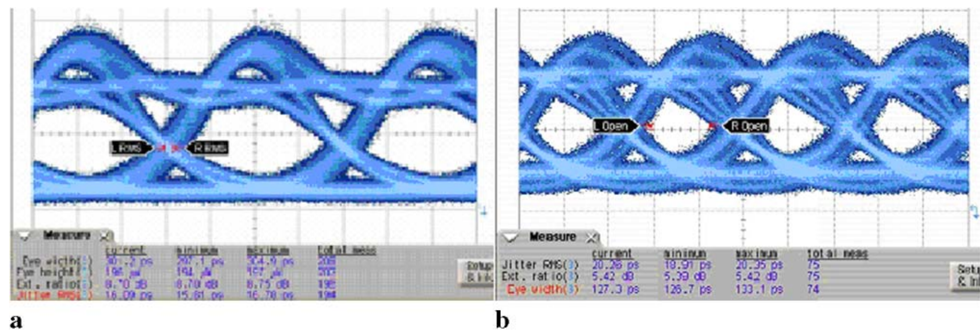

**Fig. 6** Eye diagrams of a directly modulated DBR-SEL at (**a**) 2.5 Gb/s and (**b**) 4 Gb/s

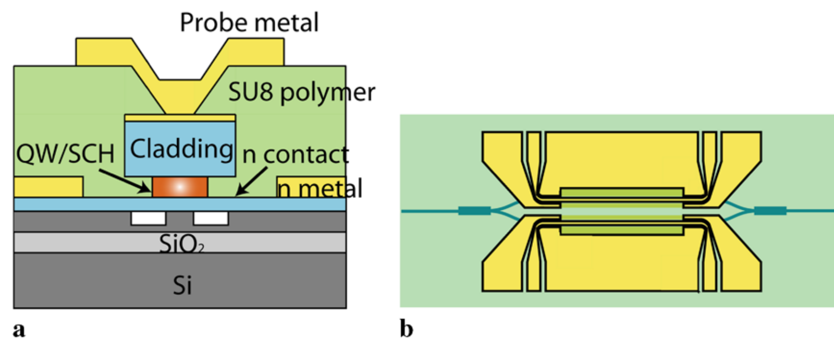


**Fig. 7** (**a**) Schematic cross section of MZM at the hybrid section. (**b**) Schematic top view of a MZM

drive current above threshold, which has a roughly linear dependence as expected. Under higher modulation powers the resonance peak becomes significantly dampened. The 3 dB electrical bandwidth at 105 mA is ~2.5 GHz.

The eye diagram in Fig. 6(a) represents the modulation signal of the device biased at 105 mA DC current with a 2.5 Gb/s, $2^{31}-1$ PRBS electrical signal with 20 mW of RF power. The extinction ratio is 8.7 dB and the fiber coupled output power is ~0.7 mW when cooled to 18°C. Although the output power and modulation bandwidth increase at higher DC currents, the extinction ratio decreases unless larger corresponding RF modulation powers are used. For example, Fig. 6(b) shows an eye diagram at 4 Gb/s that can be obtained with a DC bias of 135 mA and an RF power of 39 mW. However, in this case the extinction rate (ER) is close to 5.5 dB. Improving the laser design to decrease the threshold current and increase the differential gain is expected to significantly improve the modulation bandwidth in future devices.

## 3 Optical signal processing: modulation

While direct modulation is conceptually the simplest means to produce a modulated light source it has drawbacks of (i) limited bandwidth and (ii) lower efficiency at larger (10 Gbit/s) bandwidths. A better use of energy is to bias the laser to close the loss budget for the link being considered and use an external modulator to encode data. Silicon-based modulators are of interest because of their potential to be manufactured in high volume and at a low cost using standard CMOS processing technology. These modulators typically utilize the electroabsorption (EA) and electro-optic (EO) effects inside the silicon waveguide to deliver the necessary phase shift (or extinction ratio) needed for modulation. Exciting results recently reported on modulating light in silicon include electroabsorption modulators (EAM) based on the Franz–Keldysh effect in strained SiGe [22], and Mach–Zehnder (MZ) or ring modulators based on carrier effects [23]. One of the challenges associated with the SiGe EAMs is overcoming additional loss caused by the indirect bandgap absorption of Ge under zero bias. Silicon ring modulators that utilize carrier injection to introduce index shift have the advantage of being small and can operate up to 12.5 Gb/s by applying pre-emphasized electrical signals [23]. However, their bandwidth is fundamentally limited by carrier lifetime (~ns) due to the relatively slow recombination process. In addition, the optical bandwidth of such a structure is narrow because of the resonant nature of the ring structure. Mach–Zehnder modulators (MZM) with refractive index shift introduced by the carrier depletion effect can increase the electrical bandwidth up to 40 Gb/s and have reasonable optical bandwidths at the expense of higher voltage-length product: 40 V-mm [24]. The tradeoff between bandwidth and modulation efficiency is more difficult compared to conventional III–V modulators [25, 26]. Multiple merits of high bandwidth, large modulation efficiency, high power and wide optical bandwidth can be achieved by wafer bonding III–V material on silicon waveguides. Here we focus on the hybrid silicon MZM, which can modulate differ-

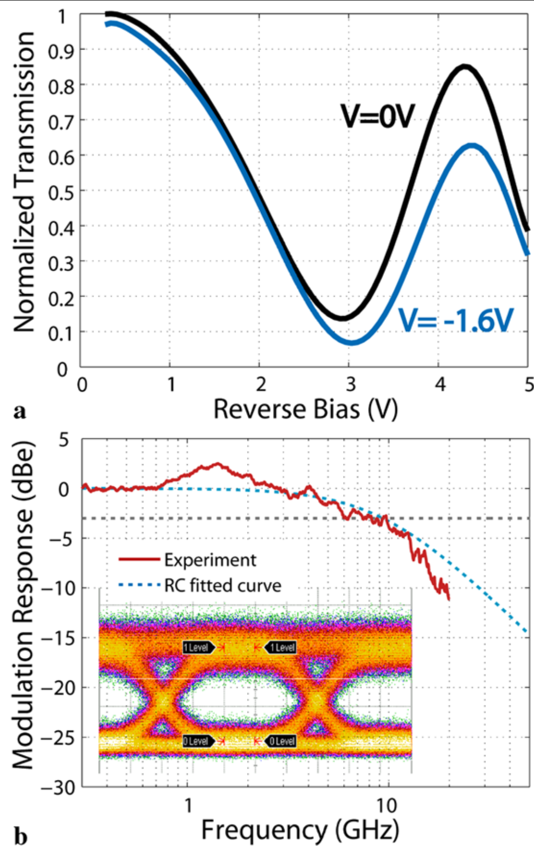


**Fig. 8** (**a**) DC characteristic of a 500 µm MZM. (**b**) Frequency response and 10 Gb/s eye diagram with $2^{31} - 1$ PRBS

ent wavelengths channels by changing the MZI bias, where the EO effect is introduced through the III–V material. The hybrid silicon EAM is demonstrated previously in [15, 18].

### 3.1 Mach–Zehnder interferometer phase modulators

The schematic cross-section of an MZM device is shown in Fig. 7(a). Two techniques were used to get better high speed performance. First, the quantum well and separate confinement heterostructure layers were under-cut to 2 µm so that the total device capacitance of the device is reduced while the cladding mesa is maintained at 4 µm to deliver a large tolerance for lithographic alignment. Next, a 5 µm thick SU8 polymer was applied to provide additional mechanical support to the thin bonding layer; and to reduce the parasitic capacitances and implement the desired electrode design. In addition, two 60 µm long tapers are added to minimize reflection and increase coupling efficiency due to the mode mismatch between the passive and hybrid sections as described in DFB and DBR lasers above.

The top view of a 500 µm MZM is shown in Fig. 7(b) with coplanar waveguides (CPW) used as contacts in order to achieve high speed performance. As can be seen in Fig. 8(a), the modulation efficiency of this device is 1.5 V mm. The extinction ratios (ER) with a bias of 0 V and −1.6 V are 8.65 and 11.6 dB, respectively. The difference in ER is due to the loss imbalance introduced between the two arms as the quantum-confined Stark effect (QCSE) becomes more significant for applied voltages greater than 3 V. The small signal response with a 25 Ω termination is shown in Fig. 8(b) and indicates a 3 dB cutoff frequency of 8 GHz. The device is then driven with 10 Gb/s pseudorandom bit sequence (PRBS) NRZ to explore the response of large signal modulation. The output signal is shown in the inset of Fig. 8(b) and is measured to have 6.3 dB ER at 3 V swing. The bandwidth of this MZM is currently RC limited, and may be improved by applying the proper traveling wave electrode design and termination. These hybrid silicon modulators can be integrated with tunable lasers to generate data streams at multiple wavelengths, and applied to WDM systems.

### 3.2 Quantum well intermixing and electroabsorption modulators

One limitation of the MZI phase modulators above is that its III–V epitaxial structure must be different to the laser to ensure low optical loss. This requires bonding multiple dies with different epitaxial structures to integrate MZM with other components. One solution to this problem involves using a quantum well intermixing technology (QWI) to shift the as-grown quantum well (QW) bandgap across the III–V wafer before bonding [14]. Using the bandgap shifted III–V material, components such as EAMs and low loss passive regions can be integrated together with hybrid silicon DBR, DFB, or tunable lasers.

The quantum well intermixing technique used in this work combines selective removal of an InP buffer with implant enhanced intermixing [27]. An outline of the as-grown III–V QWI base structure along with details of the intermixing process is shown in Fig. 10. The QWI process begins with a blanket phosphorous implant into the patterned III–V base structure as shown in Fig. 9(a). The implant is used to generate vacancies which act as a catalyst in the QWI process. A 400 nm thick plasma-enhanced chemical vapor deposition (PECVD) $SiN_x$ dielectric is used to mask certain regions of the III–V during the implant to preserve the as-grown material bandgap. The implant energy (200 kV) is chosen to generate vacancies that are localized in the InP buffer layer without penetrating into the quantum well active region. Following the implant, the vacancies generated during the implant are diffused through the quantum wells and barriers via a rapid thermal anneal (RTA) (Fig. 9(b)). The vacancy diffusion causes atomic interdiffusion between the wells and barriers, modifying their potential profile, and hence bandgap. Once a desired bandgap has been reached, the InP buffer layer can be selectively etched to remove

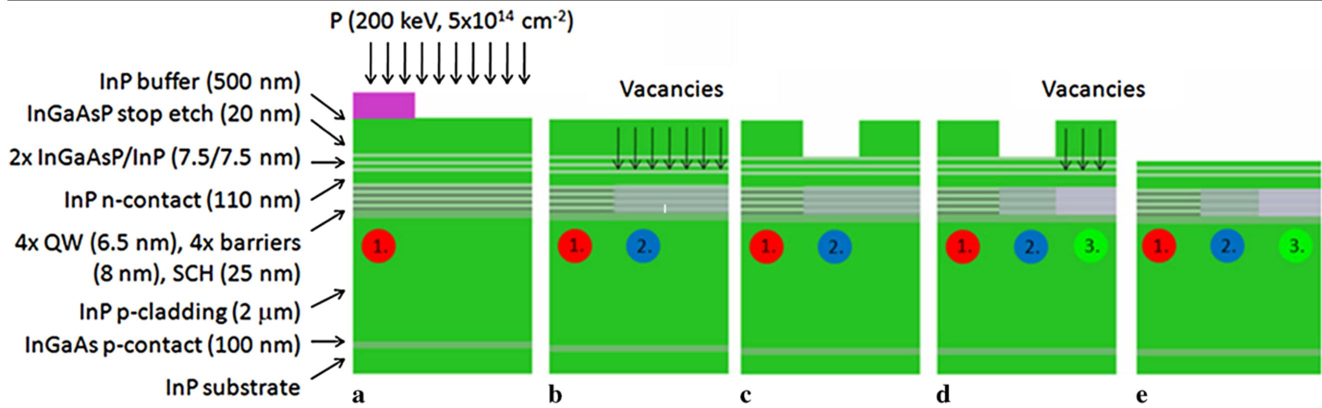


**Fig. 9** Overview of the hybrid laser QWI process. The three realized bandgaps are numbered 1, 2, and 3. (**a**) Implantation of P into InP buffer with $SiN_x$ mask to preserve the as-grown bandgap. (**b**) Diffusion of vacancies through quantum wells and barriers for bandgap 2. (**c**) Removal of InP buffer layer to halt intermixing. (**d**) Diffusion of vacancies via RTA for bandgap 3. (**e**) Removal of InP buffer layer and InGaAsP stop etch layer before bonding

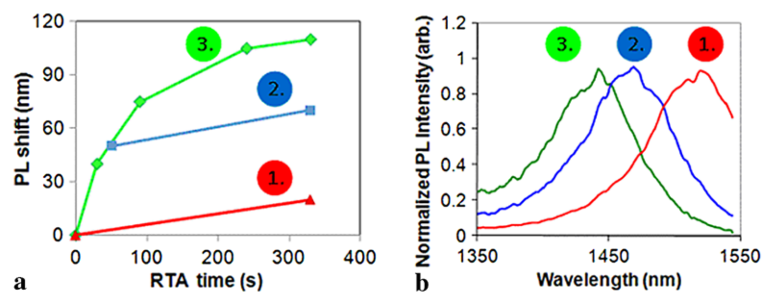


**Fig. 10** (**a**) PL shift as a function of RTA time for III–V regions that have been protected from the implant (region 1), partially intermixed (region 2), and fully intermixed (region 3) at 725°C. (**b**) Normalized PL spectra from the three bandgaps utilized in the SGDBR-EAM devices

the vacancies from the intermixing process (Fig. 9(c)). Additional RTA steps are then used to continue shifting the bandgap in regions where the InP buffer remains (Fig. 9(d)–(e)). Using an RTA temperature of 725°C, a 90 nm photoluminescence (PL) shift from the as-grown material bandgap can be achieved after a 330 s anneal. Halting the anneal after 45 s and removing the InP buffer allow an intermediate bandedge to be defined for integrated electroabsorption modulators (Fig. 10(a)).

In order to prove the feasibility of the QWI process on the HSEP, integrated sampled grating DBR-EAMs are fabricated. The bandgaps of the gain, mirror and EAM regions are 1520, 1440, and 1480 nm, respectively, as shown in Fig. 10(b). Good uniformity of the PL full width half maximum for all three bandgaps, indicates consistent material quality [28].

Fabrication of the QWI sampled grating DBR lasers is divided into pre-bonding, bonding, and post-bonding steps. Prebonding includes QWI, patterning and etching first order gratings into the bandgap shifted III–V passive regions, and patterning shallow etched waveguides into the SOI. Following prebonding, the SOI and III–V wafers are bonded together using the low temperature plasma assisted bonding process. Following bonding standard III–V fabrication is done including patterning and etching III–V mesas, depositing n and p metal contacts, proton implantation, and probe metallization [6]. Modulators include an additional lithography to etch away the n-InP contact layer to minimize parasitic capacitance. Proton implantation is used to electrically isolate the laser sections and provide current confinement. After backside processing, the laser waveguides are diced at a 7 degree angle, polished, and antireflection (AR) coated. Additional descriptions of the fabrication process can be found in [14].

SGDBR-EAM CW LI characteristics are shown in Fig. 11. CW Operation up to 45°C is achieved with output power up to 0.5 mW at 10°C. Discontinuities in the output power characteristics are a result of temperature induced cavity mode hops [29]. DC extinction characteristics from the integrated EAM are shown in Fig. 12. Greater than 5 dB extinction is achieved at −6 V reverse bias depending on the wavelength of operation. Shorter wavelengths show more efficient operation than longer wavelengths due to the proximity between the modulator bandedge and the operating wavelength. The bandwidth of the integrated modulators is 2 GHz with a −6 V bias.

The MZMs and EAMs discussed in this section enable the external signal coding capability in HSEP. While conventional III–V lasers rely on the substrate or wire-bond with junction-side down to dissipate heat, these typical approaches are impractical for HSEP. The BOX layer in the

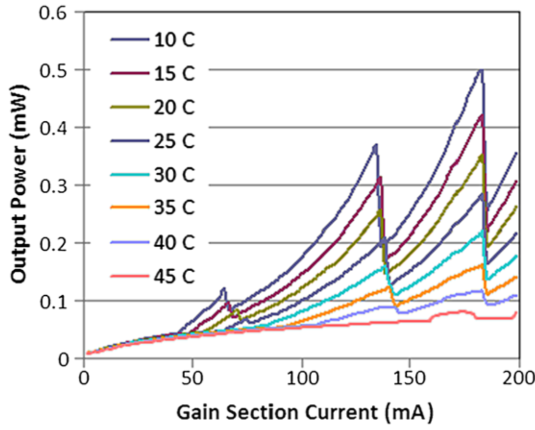


**Fig. 11** DC extinction characteristics of integrated EAM in the SGDBR-EAM with a 2.5 μm wide Si waveguide

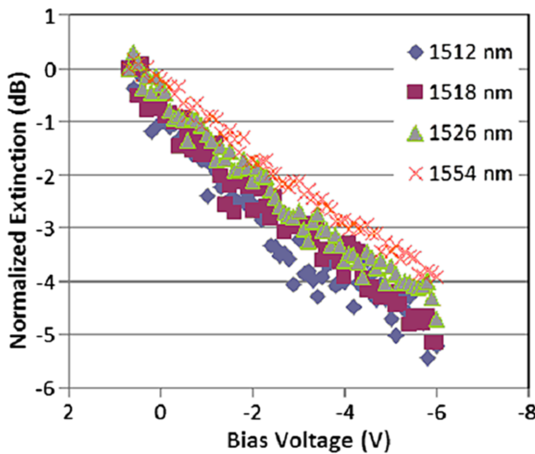


**Fig. 12** Electrical to optical small signal response of integrated electroabsorption modulators in the SGDBR-EAM with a 2.5 μm wide Si waveguide

SOI substrate is a thermal insulator with a thermal conductivity $k_{\mathrm{SiO_2}} \sim 1.3$ W/m/K, 100× lower than that of crystalline Si. The integration with other electronic components makes heat-sinking from the junction side very challenging. The experimental and theoretical thermal analysis of a hybrid silicon evanescent Fabry–Perot (FP) laser is reviewed in the following section.

## 4 High temperature operation

The hybrid laser threshold current and differential efficiency as a function of temperature can be characterized using an overall characteristic temperature ($T_0$) and an above threshold characteristic temperature ($T_1$) [1]. These characteristic temperatures are described in (1) and (2), where $I_0$ and $I_{\mathrm{P0}}$ are fitting parameters:

$$I_{\mathrm{th}} = I_0 e^{T/T_0}, \tag{1}$$

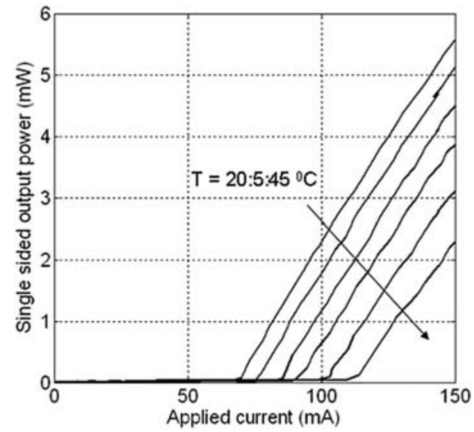


**Fig. 13** Single facet pulsed LI measurements for the 850 μm long FP hybrid laser. Results are shown for stage temperatures from 10 to 50°C and are in 10°C steps

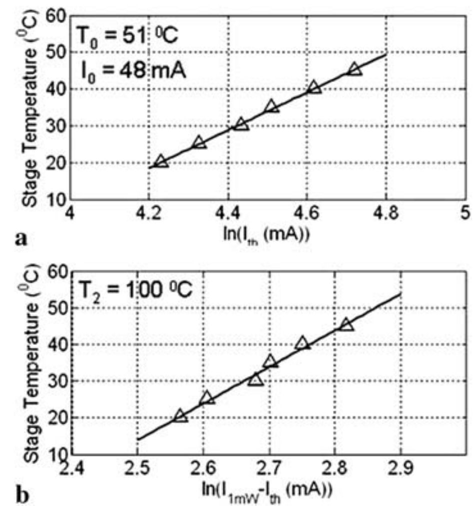


**Fig. 14** (**a**) Natural log of $I_{\mathrm{th}}$ as a function of stage temperature. (**b**) Natural log of the current required above threshold for an output power of 2 mW

$$I - I_{\mathrm{th}} = I_{\mathrm{P0}} e^{T/T_1}. \tag{2}$$

To extract characteristic temperatures, pulsed output power vs. applied current (LI) measurements (1 kHz rep rate, 1% duty cycle) were performed with the device placed on a temperature controlled stage with thermal paste. The pulsed measurement ensures that there is limited additional heating from power dissipation in the laser other than that provided by the stage. Measurements results are shown in Fig. 13 for stage temperatures ranging from 10 to 50°C. Using (1), $T_0$ can be extracted by fitting the natural log of threshold current vs. the stage temperature. Results are shown in Fig. 14(a) and give an overall characteristic temperature of 51°C. Fitting data for difference in current between threshold and that required for 2 mW of output power allows the above characteristic temperature to be deter-

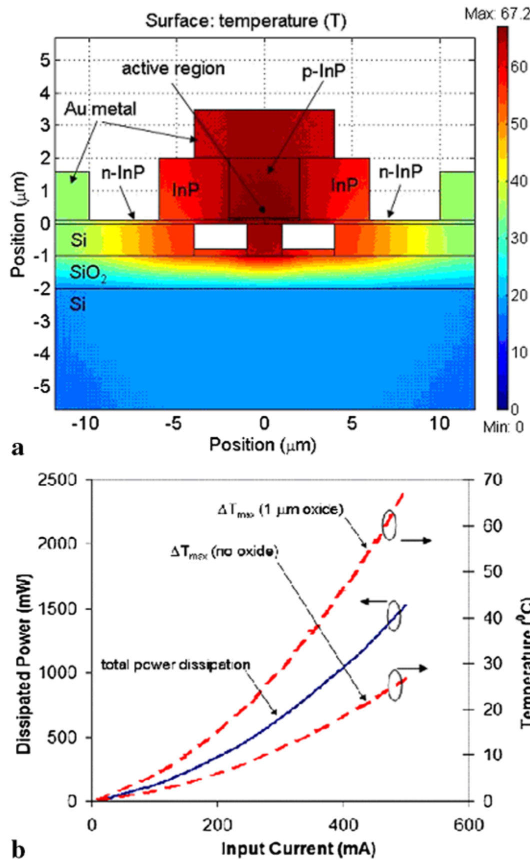


**Fig. 15** (**a**) Two-dimensional temperature profile in the hybrid laser at a bias current of 500 mA. (**b**) Theoretical predictions for the dissipated electrical power in the various laser sections along with the predicted temperature rise in the active region as a function of contact current

mined. Results are shown in Fig. 14(b) and yield a $T_1$ of 100°C.

The hybrid laser thermal impedance is measured using two experiments. The first set of measurements is used to establish a baseline for the shift in lasing wavelength as a function of active region (stage) temperature ($d\lambda/dT$). This experiment is performed pulsed to minimize device heating other than what is provided by the temperature controlled stage. The second measurement is performed CW, and is used to measure the shift in wavelength as a function of applied electrical power to the laser ($d\lambda/dP$). To extract $Z_T$, the measured $d\lambda/dT$ is combined with $d\lambda/dP$ results as shown in (3):

$$Z_T = \left(\frac{d\lambda}{dT}\right)^{-1}\left(\frac{d\lambda}{dP}\right). \quad (3)$$

Experimental results for wavelength shift as a function of stage temperature for the pulsed measurements show a $dl/dT$ of 0.067 nm/°C. For the second set of CW measurements, the experimental shift in lasing wavelength as a function of applied power is 2.8 nm/W. Combining the results in Fig. 14(a) and (b) gives a hybrid laser thermal impedance of 41.8°C/W.

The thermal performance of the hybrid laser depends on several factors. These include the amount and location of heat that is generated, the thermal conductivity of the layers surrounding the heat sources, and the operating temperature of the laser active region. To model the temperature rise in the device as a function of applied bias, we have employed a two dimensional finite element modeling technique. The thermal conductivities of the various hybrid laser regions used in this model are $k_{\mathrm{InP}} = 68$ W/m/K, $k_{\mathrm{Si}} = 130$ W/m/K, $k_{\mathrm{SiO_2}} = 1.3$ W/m/K, and $k_{\mathrm{QWs}} = 5$ W/m/K (active QWs).

A simulated two dimensional temperature profile in the hybrid laser operating at a bias current of 500 mA is shown in Fig. 15(a). The predicted temperature rise in the laser active region as a function of applied current is shown in Fig. 15(b). Using the simulated temperature rise and dissipated electrical power, the thermal impedance of the laser is calculated to be 43.5°C/W, which is in agreement with experimental results.

To show the effect of the buried oxide on the thermal impedance, Fig. 15(b) also includes a simulation of the temperature rise in the device when the buried oxide has been removed. Although removal of the BOX has detrimental effects on the optical waveguiding, replacing this layer with silicon would result in a thermal impedance of 18.3°C/W.

## 5 Wafer-scale integration

All the individual components discussed so far were fabricated on a 1 $\mathrm{cm}^2$ chip scale. While wafer-scale processing of SOI and InP wafers is common, large wafer-scale (>100 mm diameter) transfer of III–V epilayer to silicon for hybrid integration has not appeared commercially. Typical wafer-scale bonding of similar materials, such as Si-to-Si [30] or GaAs-to-GaAs [31] requires high (>800°C) or moderate (400–800°C) temperature annealing. This is prohibited in bonding of dissimilar materials, with different thermal expansion coefficients, as in the case of InP-to-Si bonding discussed here. In addition to the stress issues high temperature annealing can also alter the desired doping profile or initiate III–V material degradation, and low-temperature (<400°C) bonding is therefore required. An $O_2$ plasma-assisted low-temperature bonding process is used in this work to form strong covalent bonds at an anneal temperature of 300°C [7, 32]. One issue with using such a low anneal temperature is that it is too low to drive gas by-products ($H_2O$ and $H_2$) out of the interface [33], causing interfacial voids with a surface density as high as 55 000 $\mathrm{cm}^{-2}$ [34]. Typical void size varies from 1 to 200 μm, which can result in weak bonding and may result in significant scattering and circuit discontinuity. Resolving this outgassing issue is a key step towards high-yield mass production.

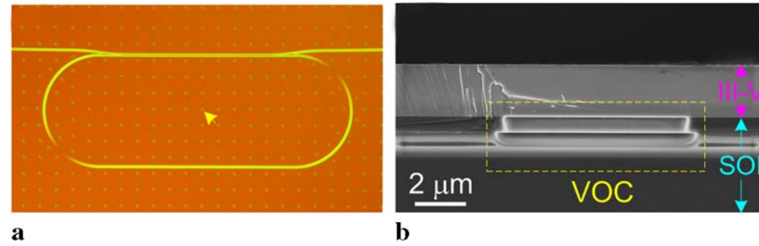


**Fig. 16** (**a**) Microscopic image of racetrack ring resonator geometry and uniformly patterned VOCs (8 × 8 μm$^2$, 50 μm spacing) as a *yellow arrow* points at; (**b**) SEM cross-sectional image of a VOC (*yellow box*) with thin III–V epitaxial layer bonded on the top

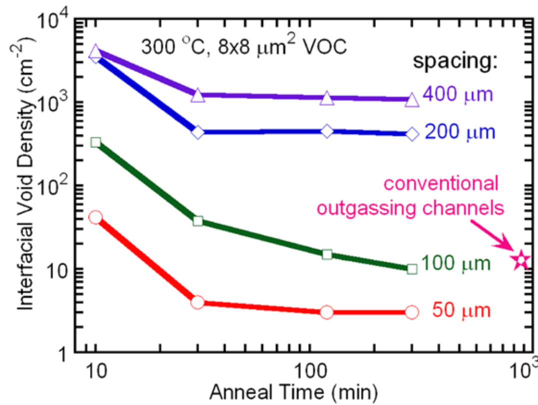


**Fig. 17** Interfacial void density vs. anneal time for VOC center-to-center spacing of 50, 100, 200, and 400 μm. The star data point represents a typical void density after 15-hour anneal by using the conventional outgassing channels

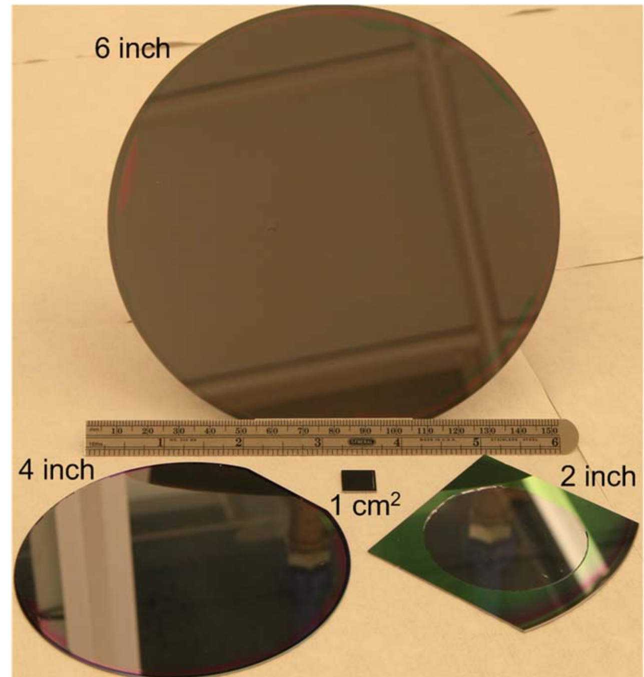


**Fig. 18** Image of the 1 cm$^2$, 50 (2 inch), 100 (4 inch) and 150 mm (6 inch) in diameter, ∼2 μm thick InP-based epitaxial layer transferred to the SOI substrate

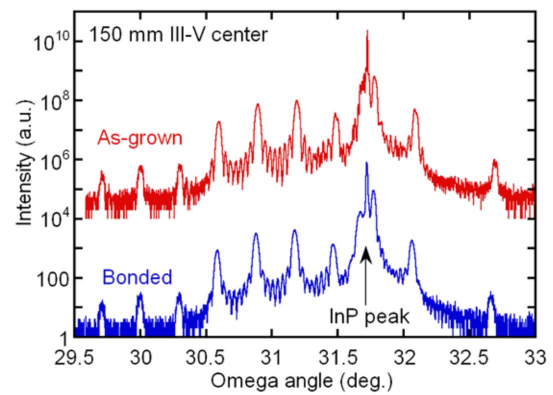


**Fig. 19** XRD rocking curve measurement of the 150 mm as-grown (*top*) and transferred (*bottom*) InP epitaxial wafer center with (004) InP peak as the reference peak

A vertical outgassing channel (VOC) design has been developed to eliminate the outgassing issue [34]. VOCs are essentially an array of holes etched through the top Si device layer to the buried oxide layer (BOX) of the SOI substrate. Gas trapped at the bonding interface can diffuse into the vertical channels while the $SiO_2$ also facilities the diffusion and absorption of $H_2O$ and $H_2$ in the BOX layer. Due to strong optical confinement of the SOI rib waveguides, VOCs have no effect on the light propagation in the waveguide circuits as shown by the microscopic image in Fig. 16(a). Their distribution depends on the waveguide circuit, offering great freedom for layout design. Figure 16(b) shows the SEM cross-sectional image of a VOC with a thin III–V epitaxial layer tightly bonded on the top.

Figure 17 shows the interfacial void density as a function of anneal time for various VOC center-to-center spacing. A threshold of required anneal time lies around 30 min, which is believed to be limited by the gas molecule diffusion to the nearby VOCs through the bonding interface. Further anneal time reduction in this temperature is believed to be attainable by further reducing VOC spacing. Small spacing values of 50 and 100 μm, therefore, show much stronger outgassing suppression capacity than large spacing values of 200 and 400 μm. We note here that it requires 15-hour or longer anneal to obtain the similar bonding quality as 100 μm VOC offers when using a conventional in-plane outgassing channels due to much lower outgassing capacity. More comparison of two approaches can be found in [34]. The size of the VOC has much weak impact to the bonding quality [34]. An optimal VOC design of 8 × 8 μm$^2$ square-

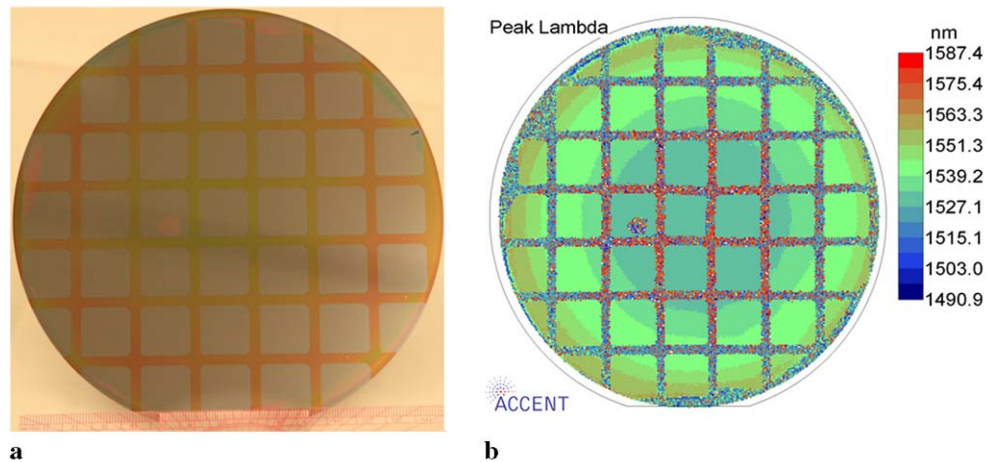


**Fig. 20** (**a**) Photo of 150 mm $SiN_x$-patterned III–V epilayer bonded on the SOI substrate. (**b**) Corresponding PL peak wavelength map of (**a**), showing uniform PL wavelength distribution and an average peak wavelength of 1540.7 nm

shape holes with 50 μm center-to-center spacing, is used in the wafer-scale bonding experiments.

Wafer-scale bonding starts with thorough cleaning by striping off any organic residue on the prepatterned SOI substrate in $H_2SO_4$:$H_2O_2$ (3:1) at 80°C for 10 min. After deionized (DI) water rinse and spin dry, a 350 nm $SiO_2$ hardmask is then removed in HF:$H_2O$ (7:1), leaving a spotless hydrophobic surface. The III–V epitaxial wafer is firstly cleaned in Acetone and Isopropyl-alcohol, followed by DI water rinse and spin dry. The III–V epitaxial wafer is then immersed in a $NH_4OH$ (39%) solution for 1 min to etch off the InP native oxide, further removing any small surface contamination. The SOI and InP wafers are then loaded into a commercial EVG 801 LowTemp Plasma Activation System sequentially. Thirty seconds $O_2$ plasma results in a thin layer of highly active native oxide on both SOI and III–V surfaces. The two wafers are then DI rinsed and spin-dried in a modified microcleanroom [35]. The DI rinse knocks off the newly attached surface particles during $O_2$ plasma treatment, and also serves as the last activation step to passivate both surface with a high density of hydroxyl groups (–OH). Following a 10 min spin dry, the face-to-face stacked wafers, which are separated by four spacers in a specially designed fixture, are placed in a covered shallow glass beaker for a final 150°C bake on a hotplate for 10 min. This is to evaporate all DI water trapped in VOCs to prevent debonding in the following 300°C anneal. Upon cooling down in ambient air, spontaneous bonding is performed to initialize InP–Si mating at room temperature. No intentional alignment is conducted during spontaneous bonding. The mating pair is annealed in a $N_2$ purged oven at 300°C for 1–2 hours typically. A selective wet etch in HCl:$H_2O$ (3:1) removes the InP substrate and stops at the InGaAs layer, resulting in ∼2 μm thick III–V epilayer transferred onto the pre-patterned SOI substrate.

Figure 18 is a photo showing the mirror-like InP-based epilayer transferred to the SOI substrates of 1 $cm^2$, 50, 100, and 150 mm in diameters. It is noted that 150 mm diameter is the currently largest InP substrate to our knowledge. Nearly 100% area transfer is achieved regardless of the bonding size. Identical void-free bonding obtained from the same process indicates that the outgassing issue is completely eliminated and this III–V-to-Si hybrid integration approach is wafer- dimension independent.

As an example, the 150 mm InGaAsP-based multiple quantum well device structure on Si after bonding and substrate removal is characterized by high-resolution X-ray diffraction rocking curve measurement. The detailed III–V epitaxial structure can be found in [36]. The (004) diffraction peak from 1.5 μm thick InP cladding layer is used as the reference. Figure 19 represents the direct comparison of Omega-2Theta scans at center of the as-grown and transferred epitaxial layer. All MQW satellites are able to be probed at nearly identical positions with no peak broadening, indicating the well-preserved crystalline structural integrity.

The 150 mm post-bond device process begins with a 300 nm PECVD $SiN_x$ deposition at 260°C (1 hour). No interfacial void or cracks occurred after this thermal and stress-inducing step except a 5 mm diameter void in the wafer center due to a surface defect on the original III–V epilayer or a surface particle, again showing strong bonding. Device mesa and chip border were then patterned and transferred to PECVD $SiN_x$ by dry etch shown in Fig. 20(a). The 200 nm InGaAs layer was subsequently removed from unpatterned area in the $H_3PO_4$ solution in order to capture the correct PL information. Pump laser wavelength and output power are 532 nm and 38.5 mW, respectively. Figure 20(b) displays the corresponding photoluminescence (PL) peak wavelength map. Compared with the as-grown epilayer, the transferred epilayer shows uniform peak wavelength with a 1.09% standard deviation and a 1540.7 nm average peak wavelength, leading to a 1.1 nm red shift within the measurement error regime. The protected chip border shows the PL wavelength peak of InGaAs layer (∼1600 nm) instead.

## 6 Conclusions

In this paper, we have reviewed a series of discrete key components realized on the hybrid silicon evanescent platform (HSEP) and the wafer-scale manufacturing perspective of this hybrid integration approach. DFB and DBR lasers with integrated photodetectors have been demonstrated from the hybrid waveguide structure where a direct bandgap III–V epilayer is bonded to low-loss SOI waveguides. The CW minimum thresholds of 25 and 65 mA, and up to 5.4 and 11 mW output powers were obtained in DFB and DBR devices, respectively. 50 dB SMSR, over 100 nm single-mode operation span and 3.6 MHz linewidth in hybrid silicon DFB devices are comparable to their commercial III–V counterparts. The hybrid silicon DBR device generates open eye-diagrams under direct modulation at data rates up to 4 Gb/s. Both DFB and DBR devices are appropriate single-frequency light sources for optical interconnects in silicon.

Optical signal manipulation is demonstrated by hybrid silicon MZMs. A 3 dB electrical bandwidth up to 8 GHz which is RC limited and a modulation efficiency of 1.5 V mm was obtained. Open eye-diagrams up to 10 Gb/s were observed as well. The EAMs integrated with the SGDBR lasers are realized in a multiple III–V bandgap structure by implementing the conventional quantum well intermixing technique to HSEP. The integrated modulator in the SGDBR-EAM showed DC extinction $>5$ dB with 6 V reverse bias and a 3 dB bandwidth up to 2 GHz.

Experimental and theoretical thermal analysis of a hybrid silicon evanescent FP laser is conducted to show the characteristic high temperature operation of HSEP. For an 850 μm long device, measurements show an overall characteristic temperature ($T_0$) of 51°C, an above threshold characteristic temperature ($T_1$) of 100°C, and a thermal impedance ($Z_T$) of 41.8°C/W. Theoretical predictions of the thermal impedance give a $Z_T$ of 443.5°C/W, which is in excellent agreement with experimental results. A theoretical model is also used to investigate the effect of the buried oxide on the device thermal impedance. It is found that the buried oxide layer accounts for 25.2°C/W of the devices thermal impedance.

With the aid of a vertical outgassing channel (VOC) design, wafer-scale integration up to 150 mm was demonstrated in the final section. VOCs enabled strong bond formed at low anneal temperature of 300°C without causing interfacial voids due to inevitable bonding reactions-induced gas byproducts ($H_2O$ and $H_2$). A void-free bonding can be attained after only 30 min anneal by reducing the channel center-to-center spacing down to 50 μm. Both high-resolution X-ray diffraction measurement and photoluminescence map indicated the preservation of the 150 mm diameter multiple quantum well structure transferred to silicon.

From both device and manufacturing aspects, HSEP has shown success in leveraging unique advantages of III–V materials, low-loss SOI waveguides and mature microelectronics infrastructure. The demonstrated merits of HSEP makes it a promising candidate for optical interconnect in silicon.

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