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Reliability evaluation of a novel fault tolerant multilevel inverter with reduced components

Niraj Kumar Dewangan[1] · Deepak Verma[2] · Rakeshwri Agrawal[3] · Dhananjay Kumar[4] · Krishna Kumar Gupta[5]

Abstract

Safety–critical applications rely heavily on multilevel inverters. This article introduces a fault tolerant (FT) multilevel inverter sustaining an uninterrupted operation with an open switch fault occurred in a single and multiple power switches. Power semiconductor devices used in dc-ac converters increased in numbers to obtain high-quality voltage waveform which makes them vulnerable to failure. As a result, reliability is one of the biggest challenges in the utilization of multilevel inverters (MLIs) in many industrial applications. At the same time, reduced component multilevel inverters can achieve the highest resolution in output voltage waveform by compromising significant features (such as fault tolerance ability, charge balance control, etc.) but it is required to be preserved. For effective fault tolerant operation of MLIs, redundant switching states have given the highest priority in terms of switch level failures. A study is being undertaken to develop a novel fault-tolerant MLI, in the event of an open circuit fault on single and multiple switches. Therefore, the proposed FT-MLI structure can fulfill the operational requirement for a time being and claimed to be reduced components. A valid fault tolerant switching technique along with appropriate fault clearance is employed to obtain the desirable output voltage waveforms. In order to determine the feasibility of FT-MLI, performance evaluations are carried out based on results obtained under normal and abnormal operating conditions through the use of a laboratory prototype.

✉ Niraj Kumar Dewangan
   niraj.dewangan@manipal.edu

   Deepak Verma
   deepakverma16@gmail.com

   Rakeshwri Agrawal
   rakeshwri.pal19@gmail.com

   Dhananjay Kumar
   dhananjayk00@gmail.com

   Krishna Kumar Gupta
   kkg.manit@gmail.com

1   Department of Mechatronics, Manipal Institute of Technology, Manipal Academy of Higher Education, Manipal, Karnataka 576104, India

2   Department of Electrical and Electronics Engineering, Birla Institute of Technology, Mesra (Jaipur Campus), Jaipur, India

3   Electrical and Electronics Engineering, Trinity Institute of Technology and Research, Bhopal, India

4   Department of Industrial Research Design and Development (IRDD), Aartech Solonics Ltd, Mandideep 462046, India

5   Electrical and Instrumentation Engineering Department, Thapar Institute of Engineering and Technology, Patiala, India

1 Introduction

Preserving the reliability and continuity of dc-ac converters, fault-related issues are important and challenging subjects in industrial processes and energy systems. Owing to this fact based on power converters, nowadays fault tolerant structures are designed in such a way that reliability improvement and system availability would be given the highest priority. Multilevel inverters (MLIs) are a versatile and high-performance power electronic converter which is popular in medium voltage to high power applications for their unique characteristics. A power electronic converter is used in many research, academic, and industrial applications—for example, in HVDC, renewable energy systems, adjustable speed drives, hybrid electric vehicles, AC motor drives, diversification of solar energy, and unified power quality correction and so on [1]. Moreover, the reliability of the whole converter system is in the challenge as widespread and increasing demand in various applications. MLIs are more popular than two-level inverters because of their advantages such as their capability to have medium voltage to high power

output, low harmonic contents, less common mode voltage and lower dv/dt stress on load, reduction in filter size, wide range of power operation, better electromagnetic compatibility, reduced voltage stress on switches, draws input current with low distortion, less switching losses and higher efficiency.

The basic configurations of inverters commercially available are neutral point clamped (NPC) or diode clamped, flying capacitor (FC) or capacitor clamped and cascaded H-bridge (CHB) converters. One of the most widely used converters is CHB due to its modular design. Complex circuitry, reduction in efficiency and low reliability are the major complications in these basic inverters as the number of levels increased.

According to a survey on multilevel converter topologies, it is concluded that all these topologies encounter an increased number of component count and require huge capacitors leading to sophisticated control techniques [2]. In the current scenario, advancement in inverter circuits which can meet the issues above is greatly recommended. To overcome these drawbacks, a new breed of MLI topologies is developed with reduced component (RC) and improved performance to further advancement in converters.

RC-MLIs offer significant advantages over conventional converters such as a minimum number of switches requirement, protection circuit and heat sink, fewer diodes as the number of output level increases. Hence, results in low cost, reduced circuit complexity and reduced weight to RC-MLIs. Each of these has its pros and cons proposed in various literature [3, 4]. Due to the significant upswing in voltage levels with a reduction in power switches, RC MLIs can be considered as a good alternative for converters to be used in power applications. However, comparing with other inverter structures containing a large number of components, MLIs have lower reliability resulting in a higher possibility of malfunctioning. Anyone of the single open switch fault (OSF) may cause abnormal operation of the electrical drive systems. Practically, open circuit and short circuit faults are associated with the types of faults arises in the power switches. The system is fatally damaged when a power switch experiences a short circuit and requires extra circuitry to safeguard. To analyse open circuit faults in power switches, this work considers open circuit faults in power switches. In case of RC-MLIs lowering the components tend to a reduction in redundant states that means any device failure directly affects the whole system interruption. In recent years, a new pace in topologies design has been attracting attention with the specific objective of reducing component counts. An improved voltage waveform can be obtained by adding more levels at the output [5]. Moreover, reduction in device count is achieved, but certain features such as reduction in several switching states and loss of control complexity can be affected. As a result, many RC-MLIs suffered from lack of charge balance control, incapable of sustaining in fault scenarios. Additionally, preserving an aspect of redundant states is being actively pursued in addition to reducing device count.

Fault tolerant solutions are presented by several investigators to commercially available MLIs (NPC, FC, and CHB) with multilevel voltage output [6]. In recent times, the issues related to failures in MLIs are getting attention of investigators. These concerns are to be resolved to fulfill the operational requirements of the system. The subject of reliability in MLIs is prevalent as they have a more significant number of devices resulting in a high probability of fault occurrence. The main reason behind overall inverter failure is the failure of active power semiconductor devices, drivers, and sources [7, 8]. Due to the large number of components used in converters, it is always possible for an open circuit fault to occur concurrently at one or more components. Therefore, it is required to stop the operation of the system to prevent damage. Additionally, it may be possible to provide continuous power supply to the load and tolerate open circuit faults in order to maintain an acceptable output voltage.

Various FT topologies are proposed to address the reliability issue in DC-AC converters [9]. The main disadvantage of traditional two-level inverters is their low reliability; they are being replaced by MLIs. An increase in switching devices and their vulnerability leads to this issue [10]. A bidirectional switch or relay is connected to CHB inverter to isolate the faulted cell from the primary system [11]. NPC structure is made FT with the use of switching elements in place of the clamping diodes [12]. Bidirectional switches are included in the modified NPC 3-Φ structure [13]. A hybrid structure is proposed in [14] by combining one leg of a diode-clamped inverter with a half bridge and the addition of a bidirectional switch. This structure is capable of tolerating faults in case of switch/source failure along with equal power sharing, thereby increasing the overall number of device count and cost of the inverter. In [15, 16], FT structure of FC is presented. Although, the circuit itself has capability of fault ride through, however, the major issues of concern are increase in devices and complexity in capacitor balancing technique. In case of short circuit faults in switches, additional circuitry is required to protect the inverter as they are catastrophic faults [17].

A brief review is included in [18, 19] regarding the operation and control of MLIs with reduced components. According to a survey presented in [20], 21% and 13% MLIs being used in several industrial appliances are found to be prone to the power switch and soldering failures, respectively. Thus, an overall failure of 34% of the device module can be observed leading to whole system dysfunction. Another study shows a total of 38% of variable speed ac drives malfunction due to power switch failure [21]. A study mentioned in [22–24] examined the switching device failure rate and
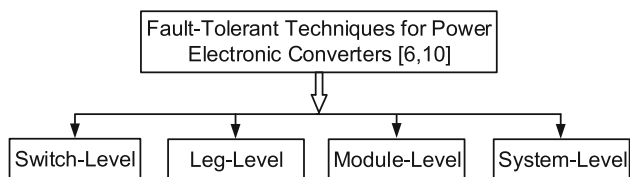
Fig. 1 Chart of fault-tolerant methodology for power electronics converter

reliability of MLI configurations. From the past literature, several solutions that are found to meet fault tolerant operation are discussed in [22, 25–29]. In general, power electronic converters are divided into four categories based on their fault tolerance capability and depending upon hardware redundancy as depicted in Fig. 1. This study is confined to a switch-level fault, i.e. OSF in the proposed novel reduced components dc-ac converter.

The overall system can shut down and take a longer time to get back to normal after failure of any single/multiple device in RC-MLIs, despite the reduction in semiconductor device count. These limitations bring the need for fault tolerance strategy to the affected systems to maintain its operation continuously by supplying power to the load. Hence, in this paper, a FT RC-MLI structure is proposed. RC-MLIs are compromising itself in terms of redundant states and therefore, OSF may cost substantial loss by system interruption. The proposed FT structure generates required redundant states (RS). The redundant states play a strategic role in case of switch level fault occurrence. The stated paper fills the gap by developing novel fault tolerant RC-MLI.

A single phase form of the proposed FT-MLI is presented in this work to address earlier discussed subjects of concern. To make it more reliable and fault-tolerant, the least changes in the switching pattern is accomplished. The minimum probability of possible power device failure is given in tabulation of the presented FT-MLI. In the event of OSF, the minimum levels required to maintain the functionality of the systems with acceptable output voltage levels are generated. A sufficient number of desired redundancy can be generated by the proposed FT-MLI. It confirms the continuation of operation of the structures in instance of OSF. A brief discussion is presented in the next section. A comparative study based on the component count, FT feature and reliability analysis are presented for the proposed FT-MLI with some recently published structures. Detection and identification of faults are not covered and kept out of the scope of this research work. Figure 2 shows a flow chart in relation to working of fault tolerant operation of proposed MLI in the event of OSF.
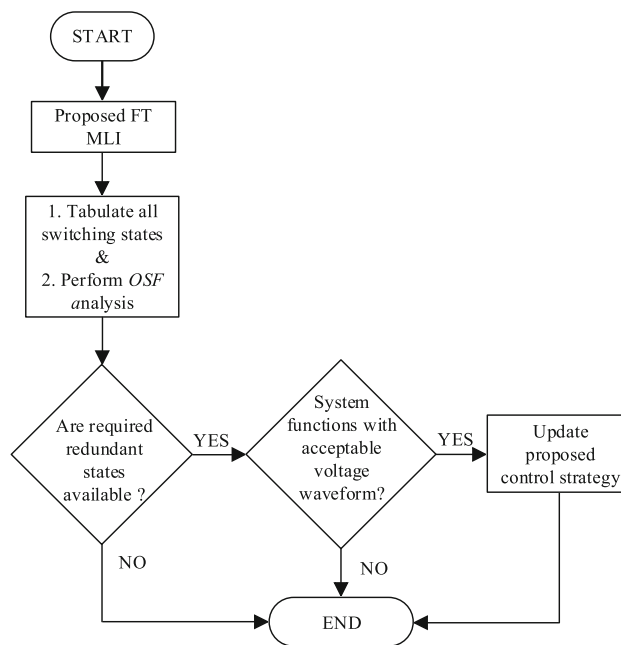

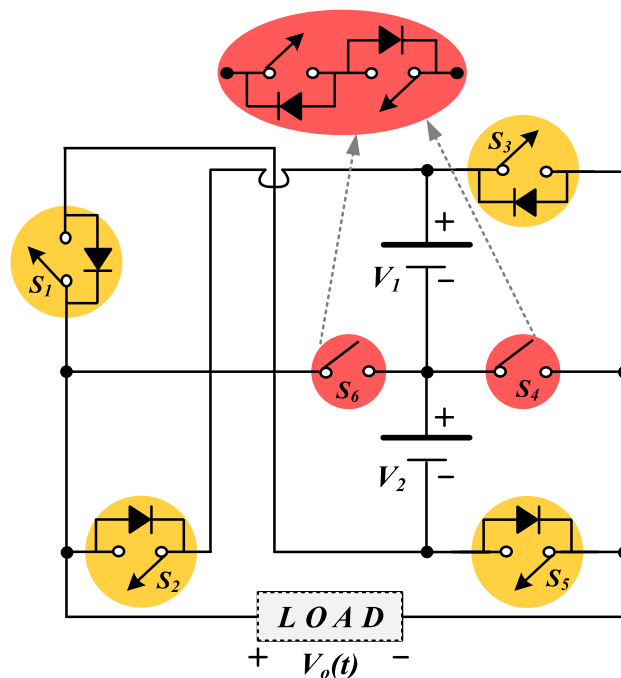**Fig. 2** Flow chart illustrating fault tolerant operation of proposed FT-MLI

Fig. 3 The Proposed FT MVSI structure

2 Switching states analysis for the proposed novel FT-MLI under OSF

In this section, the proposed FT-MLI is briefly analysed based on their various combination of ON state switches and evaluated accordingly to sustain faults in one of the switches. The

single phase form of the proposed FT structure is outlined for simplicity of operation.

2.1 Proposed novel FT-MLI

A fault-tolerant multilevel voltage source inverter (FT-MVSI) with an innovative design is introduced. The proposed power circuit minimizes the overall device count and maximizes the output voltage levels. The FT-MVSI significantly reduces power losses compared to classical inverters. Figure 3 illustrates the proposed basic inverter unit. The inverter circuit includes two input DC voltage sources (V_1, V_2) of same value, four unidirectional (S_1, S_2, S_3, S_5) and two bidirectional (S_4, S_6) power switches accompanied by gate drivers. A number of combinations of switching states are shown in Table 1 for generating corresponding levels at output voltage for the basic inverter unit. From Table 1, it can be seen that there are more than one switching states for each voltage level ($+ V$ and $- V$). These redundant switching states enable fault-tolerant operation of the proposed FT structure.

According to Table 2, the occurrence of OSF in single and multiple switches cannot interrupt the function of the converter and able to generate acceptable output voltage waveforms by altering switching combination with a reduction in magnitude. Moreover, failure of S_1 and/or S_2 leads to the presence of levels such as 0 (state α_3), $+ V_2$ (state α_5), $- V_1$ (state α_7). Fault in S_1 and/or S_4 able to synthesize levels like 0 (state α_1), $+ V_2$ (state α_5), $- V_1$ (state α_7) and $+ V_1 + V_2$ (state α_8). Open circuit fault in S_1 and/or S_5 can accommodate 0 (state α_1), 0 (state α_3), $+ V_1$ (state α_4) and $- V_1$ (state α_7) voltage levels, respectively. Furthermore, fault in S_2 and/or S_3 able to provide voltage levels 0 (state α_2), 0 (state α_3), $+ V_2$ (state α_5) and $- V_2$ (state α_6), respectively. OSF in S_2 and/or S_4 can avail voltage levels such as 0 (state α_2), $+ V_2$ (state α_5), $- V_1$ (state α_7) and $- V_1 - V_2$ (state α_9). Open circuit failure of S_3 and/or S_5 that cause the FT MVSI to synthesize 0 (state α_3), $+ V_1$ (state α_4), $- V_2$ (state α_6) voltage levels. In addition, S_3 and/or S_6 faults are capable of supplying voltage levels 0 (state α_2), $+ V_1$ (state α_4), $- V_2$ (state α_6) and $+ V_1 + V_2$ (state α_8), respectively. Also, Fault in S_4 and/or S_6 can supply voltage levels 0 (state α_1), $+ V_1 + V_2$ (state α_8), $- V_1 - V_2$ (state α_9). The fault in S_5 and/or S_6 can provide voltage levels 0 (state α_1), $+ V_1$ (state α_4), $- V_2$ (state α_6) and $- V_1 - V_2$ (state α_9). Thus, by updating the proposed FT switching scheme timely, output voltage levels with reduced magnitude can be generated in the case of failure of some of the switches in the aforementioned analysis. In these cases, the available redundant states provide the required voltage levels to support the operation by altering the faulty switches. The failure of different switches mentioned above thereby enables the proposed structure to be partial fault tolerant in fault scenarios.

Similarly, if any one of the switches S_4 or S_6 fails, the FT structure synthesizes five-level output voltage level for reliable operation of the proposed circuit from the available redundant states. The failure of these switches (if any) assures full fault-tolerant operation of the proposed unit. The fault tolerant operation can be possible for the proposed FT topology in a similar way by updating the switching strategy.

The theoretical evaluation justifies the desired level of operation after OSF to the presented topology as per expectation. The alteration to three from five level output voltage waveform occurred for some of the switches except S_4 and S_6.

3 Detailed analysis

3.1 Calculation of losses

Switching losses (P_{Sw}) and conduction losses (P_{Con}) are considered to calculate losses for the proposed FT MLI.

3.1.1 Switching losses

The switching losses (P_{Sw}) is the power dissipated during switch transition from ON to OFF and vice-versa. The linear approximation model of an ideal switch is used to calculate the switching losses for typical power devices (IGBTs and Diodes) [19]. Turn-on and turn-off energy losses $\left(E_{on,\,T},\ E_{off,\,T}\right)$ for switch can be calculated as:

$$E_{on,\,T} = \int_{0}^{t_{on}} v(t)i(t)\mathrm{d}t = \int_{0}^{t_{on}}\left[\left(\frac{V_{sw}t}{t_{off}}\right)\left(-\frac{I_1(t - t_{on})}{t_{on}}\right)\right]\mathrm{d}t$$

$$= \frac{1}{2}V_{SW}I_1 t_{on} \tag{1}$$

$$E_{off,\,T} = \int_{0}^{t_{off}} v(t)i(t)\mathrm{d}t = \int_{0}^{t_{off}}\left[\left(\frac{V_{sw}t}{t_{off}}\right)\left(-\frac{I_2(t - t_{off})}{t_{off}}\right)\right]\mathrm{d}t$$

$$= \frac{1}{2}V_{SW}I_2 t_{off} \tag{2}$$

where V_{SW} represents the voltage across switch before turning-on or after turning-off. Furthermore, the numbers of switches which undergo ON/OFF during a fundamental period T are denoted by N_{on} and N_{off}. The switching losses are expressed according to Eq. (4).

$$P_{Sw} = \frac{1}{T}\left(N_{on}E_{on} + N_{off}E_{off}\right) \tag{3}$$

Table 1 Different switching states of the proposed FT MVSI

State	Switching Sequence (ON = 1, OFF = 0)						$V_o(t)$
	S_1	S_2	S_3	S_4	S_5	S_6	
α_1	0	1	1	0	0	0	0
α_2	1	0	0	0	1	0	0
α_3	0	0	0	1	0	1	0
α_4	0	1	0	1	0	0	$+ V_1$
α_5	0	0	0	0	1	1	$+ V_2$
α_6	1	0	0	1	0	0	$- V_2$
α_7	0	0	1	0	0	1	$- V_1$
α_8	0	1	0	0	1	0	$V_1 + V_2$
α_9	1	0	1	0	0	0	$- V_1 - V_2$

Table 2 Switching states for open switch fault (OSF) under normal, single and multiple switch failed cases

Failed switches	Unavailable states	Possible states	Number of levels in output	Output power
Normal operation	$\alpha_1, \alpha_2, \alpha_3, \alpha_4, \alpha_5, \alpha_6,$ $\alpha_7, \alpha_8, \alpha_9$	–	Five	Full
S_1 and/or S_2	$\alpha_1, \alpha_2, \alpha_4, \alpha_6, \alpha_8, \alpha_9$	$\alpha_3, \alpha_5, \alpha_7$	Three	Full
S_1 and/or S_4	$\alpha_2, \alpha_3, \alpha_4, \alpha_6, \alpha_9$	$\alpha_1, \alpha_5, \alpha_7, \alpha_8$	Three	Full
S_1 and/or S_5	$\alpha_2, \alpha_5, \alpha_6, \alpha_8, \alpha_9$	$\alpha_1, \alpha_3, \alpha_4, \alpha_7$	Three	Full
S_2 and/or S_3	$\alpha_1, \alpha_4, \alpha_7, \alpha_8, \alpha_9$	$\alpha_2, \alpha_3, \alpha_5, \alpha_6$	Three	Full
S_2 and/or S_4	$\alpha_1, \alpha_3, \alpha_4, \alpha_6, \alpha_8$	$\alpha_2, \alpha_5, \alpha_7, \alpha_9$	Three	Full
S_3 and/or S_5	$\alpha_1, \alpha_2, \alpha_5, \alpha_7, \alpha_8, \alpha_9$	$\alpha_3, \alpha_4, \alpha_6$	Three	Full
S_3 and/or S_6	$\alpha_1, \alpha_3, \alpha_5, \alpha_7, \alpha_9$	$\alpha_2, \alpha_4, \alpha_6, \alpha_8$	Three	Full
S_4	$\alpha_3, \alpha_4, \alpha_6$	$\alpha_1, \alpha_2, \alpha_5, \alpha_7, \alpha_8, \alpha_9$	Five	Full
S_4 and/or S_6	$\alpha_2, \alpha_3, \alpha_4, \alpha_5, \alpha_6, \alpha_7$	$\alpha_1, \alpha_8, \alpha_9$	Three	Full
S_5 and/or S_6	$\alpha_2, \alpha_3, \alpha_5, \alpha_7, \alpha_8, \alpha_9$	$\alpha_1, \alpha_4, \alpha_6, \alpha_9$	Three	Full
S_6	$\alpha_3, \alpha_5, \alpha_7$	$\alpha_1, \alpha_2, \alpha_4, \alpha_6, \alpha_8, \alpha_9$	Five	Full

3.1.2 Conduction loss

The conduction losses in a switch ($P_{\text{loss, con, sw}}$) and a diode ($P_{\text{loss, con,} d}$) can be written as follows [23]:

$$P_{\text{loss, con, sw}} = V_{\text{on, sw}} I_{\text{sw, avg}} + R_{\text{on, sw}} I_{\text{sw, rms}}^2 \tag{4}$$

$$P_{\text{loss, con,} d} = V_{\text{on,} d} I_{d, \text{avg}} + R_{\text{on,} d} I_{d, \text{rms}}^2 \tag{5}$$

$$P_{\text{con}} = P_{\text{loss, con, sw}} + P_{\text{loss, con,} d} \tag{6}$$

where $V_{\text{on, sw}}$ and $V_{\text{on,} d}$ are the power switch and anti-parallel diode ON-state voltages, respectively. The average and rms currents across the switch and anti-parallel diode are represented by $I_{\text{sw, avg}}$ and $I_{d, \text{rms}}$, respectively. The equivalent resistances of the power switch and anti-parallel diode are $R_{\text{on, sw}}$ and $R_{\text{on,} d}$, respectively.

Thus, the total power loss of MLI is evaluated by using Eqs. (3), and (6). In addition, efficiency (η) is obtained from Eq. (7):

$$\eta = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{loss}}} \tag{7}$$

where P_{out} and P_{in} are output and input power of the inverter respectively [19]. The IGBT (*GW30NC120HD*) is used to hardware implement the proposed topology. Figure 4 shows the efficiency and power losses of the propesed FT MLI under healthy and various OSF conditions.

3.2 Comparision on the basis of reliability

Reliability (denoted by $R(t)$) of an inverter is the probability that it will perform the desired functions during a certain time period (t). There is a range of reliability between 0 and 1.
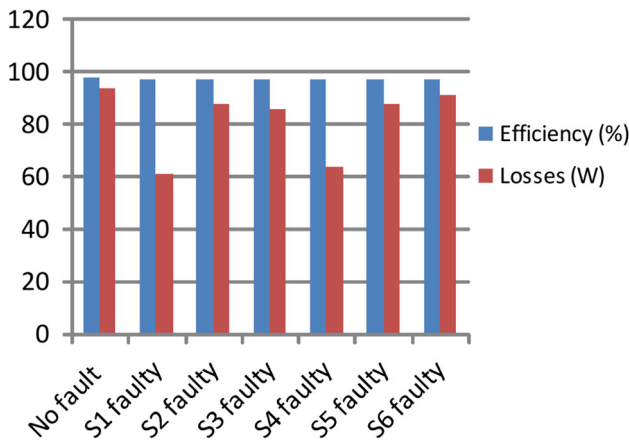
Fig. 4 Efficiency and power losses of the propesed topology under healthy and various single OSF conditions
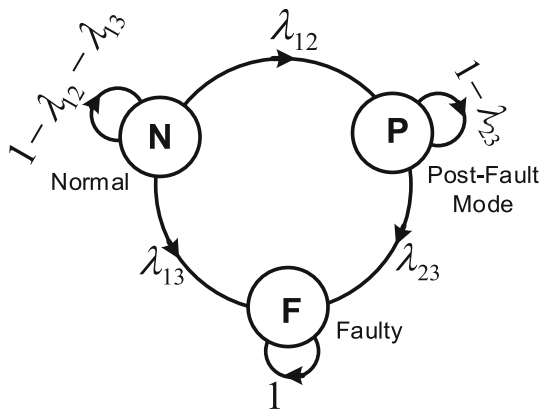

Fig. 5 Markov state transition model

$R(t)$ can be calculated using the following equation:

$$R(t) = e^{-\lambda t} \tag{8}$$

where 'λ' represents the failure rate, and 't' represents the time elapsed until the first failure occurs. Markov chain reliability analysis can be used to evaluate and compare the reliability of various power electronic systems and devices. The Markov state transition model is formulated as presented in Fig. 5. In this Markov state transition model, three states have been considered: Normal state (N), post-fault state (P) and complete failure state (F).

In this case, the probability of state transition rate is defined as the sum of all possible states. Accordingly, λ_{12}, λ_{23} and λ_{13} are the probabilities of state transition from Normal State (N) to the post-fault state (P), post-fault state (P) to complete failure state (F) and Normal State (N) to complete failure state (F).

$$\text{MTTF} = \frac{1}{\lambda} = \frac{1}{\lambda_{12} + \lambda_{23} + \lambda_{13}} \tag{9}$$

where MTTF is mean time to failure.

3.3 Calculation of failure rate

The failure rates of the power semiconductor switch (MOSFET IRF640N) are estimated according to [22]. This paper uses the Military reliability handbook MIL-HDBK-217F [23] to estimate the failure rate of each component, which is defined as the number of components that fail over the course of time. Further, the required parameters of the components and values from their datasheets are provided in Table 4 [22]. The Military Reliability Handbook is used to determine the relative enhancement in MTTF, despite the fact that the handbook itself has received so many criticisms for numerous reasons. The following equation can be used to calculate the failure rate of each component:

$$\lambda_{\text{component}} = \lambda_b \sum_{i=1}^{n} \pi_i \left(\text{failure} \middle/ 10^6 \text{hours} \right) \tag{10}$$

A failure rate of a device is given by λ_b, and n is the number of π_i factors that affect that failure rate. Moreover, it is determined as the failure rate per million hours (failures/10^6 h).

Various power electronic components like switch, diodes, and capacitors are provided in Table 3. In aforementioned table, failure rates across three components such as switch λ_S (failures/10^6 h), diode λ_D (failures/10^6 h), electrolytic capacitor λ_C (failures/10^6 h) and temperature factor of the components are combined.

Component failure that changes with different circumstances is the temperature and effectiveness factors of devices, so they fail differently in space and in the ground. Hence, the component's operating condition on ground is represented by $\pi_E = 1$, π_Q represents the component's quality of 1 and π_A represents the switch's application factor.

As a capacitance factor for a capacitor, π_{Cap} represents the dielectric material and depends on the capacitor's rated capacitance [22]. Equation (11) can be used to calculate the capacitance factor in a dielectric capacitor.

$$\pi_{\text{Cap}} = 0.34 C^{0.18} \tag{11}$$

In the equation, Capacitance is measured in microfarads by 'C'.

In diodes, π_C is the contact construction factor and π_S is the electrical stress factor. A metallurgical diode is considered to have a contact factor of 1, whereas a non-metallurgical diode has a contact factor of 2. Here, T_j stands for junction temperature, and T_C is the ambient temperature of the diode

Table 3 Temperature and effective factor for each component [22]

Components	Effective factors	Temperature factor
Switch	$\lambda_S = \lambda_b \pi_T \pi_A \pi_R \pi_S \pi_Q \pi_E$	$\pi_{T,\text{switch}} = \exp\left[-1925\left(\frac{1}{T_j+273} - \frac{1}{298}\right)\right]$
Diode	$\lambda_D = \lambda_b \pi_T \pi_C \pi_S \pi_Q \pi_E$	$\pi_{T,\text{diode}} = \exp\left[-3091\left(\frac{1}{T_j+273} - \frac{1}{298}\right)\right]$
Capacitor	$\lambda_C = \lambda_b \pi_T \pi_S \pi_{Cap} \pi_Q \pi_E$	$\pi_{T,\text{Cap}} = \exp\left[\frac{0.15}{8.617*10^{-5}}\left(\frac{1}{T_a+273} - \frac{1}{298}\right)\right]$

and switch, which can be calculated using the following equation:

$$T_j = T_C + \theta_{\text{JC}} P_D \tag{12}$$

$$T_C = T_a + \theta_{\text{CA}} P_D \tag{13}$$

θ_{JC} ($^0C/W$) is the maximum junction to case thermal resistance and maximum power dissipation is given by for switch or diode.

The power loss of the switch ($P_{D,\text{Switch}}$) and diode (P_D) is given in the following equations:

$$
\begin{aligned}
P_{D,\text{Switch}} &= P_{\text{CL}} + P_{\text{SL}} \\
&= \frac{1}{T_S} \int_0^{T_S} \left[R_{\text{DS, on}} i_S^2(t) + V_T i_S(t)\right] dt + \left[C_0 f_S V_{\text{DS}}^2\right]
\end{aligned}
\tag{14}
$$

$$P_D = \frac{1}{T_S} \int_0^{T_S} \left[R_d i_S^2(t) + V_F i_D(t)\right] dt \tag{15}$$

In the above equation, $R_{\text{DS, on}}$ is the drain-source on-state resistance of the switch, and R_d is the on-state resistance of the diode. A reliability analysis is dependent upon the temperature factor and the diode and switch power losses [23]. Conduction loss (P_{CL}) and switching loss (P_{SL}) are primarily responsible for estimating power loss (Table 4).

3.4 MTTF calculation and reliability comparison

3.4.1 Proposed FT-MLI topology

The proposed topology is FT for all switches (MOSFET) and therefore enters from post-fault state (P) from Normal State (N) occurs if any one of the four unidirectional and two bidirectional switches is failed. So λ_{12} is defined as

$$\lambda_{12} = 6\lambda_T \tag{16}$$

For any remaining MOSFET, if OSFs occur, the system may transition to a failure state (F) from a post-fault state (P). So λ_{23} is defined as

$$\lambda_{23} = 2\lambda_T + 8\lambda_D \tag{17}$$

where λ_C represents the failure rate of capacitor. When fault occurs simultaneously in two switches from the remaining circuit structure, the system enters the failure state (F) from normal state (N). So λ_{13} is defined as

$$\lambda_{13} = 6\lambda_T^2 + 8\lambda_D \tag{18}$$

3.4.2 CHB-MLI

All of the eight unidirectional switches in [23] have FT, which allows the CHB-MLI to enter the post-fault state (P) from the normal state (N) if any of them fails. Therefore, λ_{12} is defined as follows:

$$\lambda_{12} = 8\lambda_T \tag{19}$$

For any remaining MOSFET, if OSFs occur, the system may transition to a failure state (F) from a post-fault state (P). So λ_{23} is defined as

$$\lambda_{23} = 6\lambda_T \tag{20}$$

In the event of a fault occurring simultaneously in any two MOSFETs from the remaining switches, the system will enter into failure mode (F). So λ_{13} is defined as

$$\lambda_{13} = 24\lambda_T^2 \tag{21}$$

3.4.3 ANPC-MLI

The ANPC-MLI in [24] is FT for four unidirectional switches (MOSFET). The transition from normal state (N) to post-fault state (P) occurs if one of the MOSFETs fails. So λ_{12} is

Table 4 Required parameters of the components, explanation and values taken from their (MOSFET IRF640N) datasheet

Parameters	Explanations	Value	Parameters	Explanations	Value
$R_{DS(on)}$	conductive resistance	0.07 Ω	V_F	Forward voltage of diode	0.5 V
V_T	Threshold voltage	0.5 (V)	R_D or r_d	Diode conductive resistance	0.2 Ω
C_0	Capacitance of power switch out capacitor	330 pF	θ_{CA}	Case to ambient temperature Diode	$63 \left({}^0C/W \right)$
θ_{JC}	Junction to Case temperature of power switch	$1 \left({}^0C/W \right)$	θ_{JC}	Junction to Case temperature Diode	$1.5 \left({}^0C/W \right)$
θ_{CA}	Case to ambient temperature of power switch	$62 \left({}^0C/W \right)$	λ_b	Basic failure rate of Diode	0.0038
λ_b	Basic failure rate of power switch	0.06	λ_b	Basic failure rate of Capacitor	0.00254

defined as

$$\lambda_{12} = 4\lambda_T \tag{22}$$

Let, the OSF is occurred in any one remaining seven MOSFET, the system transition probability to failure state (F) from post-fault (P) state. So λ_{23} is defined as

$$\lambda_{23} = 7\lambda_T \tag{23}$$

When OSF occurs simultaneously inside any two MOSFETs from remaining switches, the system enters the failure state (F) from the normal state (N). So λ_{13} is defined as

$$\lambda_{13} = 4\lambda_T + 28\lambda_T^2 \tag{24}$$

Probabilities of the multilevel inverter being in a certain (i.e. either Normal State (N) or post-fault state (P)) state can be calculated as follows:

$$\overset{\bullet}{P_1}(t) = -(\lambda_{12} + \lambda_{13})P_1(t) \tag{25}$$

$$\overset{\bullet}{P_2}(t) = -(\lambda_{23})P_2(t) + (\lambda_{13})P_1(t) \tag{26}$$

The reliability function $R(t)$ can be obtained as follows:

$$R(t) = P_1(t) + P_2(t) \tag{27}$$

$$R(t) = \frac{\lambda_{12}e^{-\lambda_{23}t} + (\lambda_{13} - \lambda_{23})e^{-(\lambda_{12}+\lambda_{13})t}}{\lambda_{12} + \lambda_{13} - \lambda_{23}} \tag{28}$$

It is noteworthy that the proposed fault-tolerant topology has greater reliability in terms of MTTF. In the preceding equations, the reliability of the proposed FT-MLI topology, conventional CHB-MLI and ANPC-MLI topologies are plotted against time for easy understanding. The reliability curve is plotted for the conventional CHB, ANPC and proposed
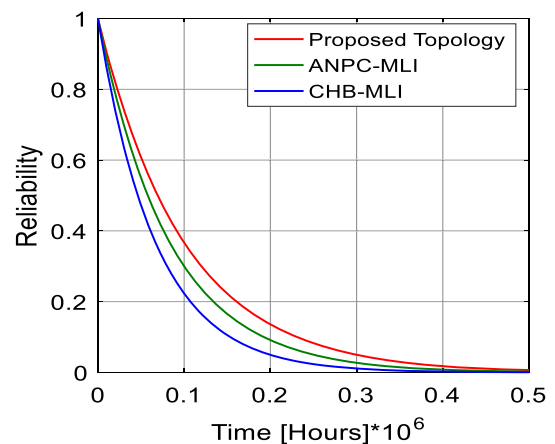

Fig. 6 The reliability curve of the proposed topology compared to MLI conventional topologies

FT-MLI topology using Eq. (28) and is shown in Fig. 6. has higher reliability than the conventional topologies.

4 Simulation results

To authenticate the performance of the proposed FT concept, the newly developed single phase FT-MLI is simulated using MATLAB/SIMULINK along with Sim-Power-Systems toolbox. The arbitrarily considered inverter parameters for the proposed FT topology are mentioned in Table 5. The proposed FT topology is controlled by a multicarrier pulse width modulation strategy. The generation of switching pulses is governed by continuous comparison of carrier signals (3000 Hz) and fundamental signal (50 Hz). The triggering pulses so obtained are employed to each an individual switches to achieve different voltage levels. The number of carrier signals proportionally increases with the increase in levels.

Table 5 Simulation and experimental parameters

DC supply ($V_1 = V_2$)	48 V
Power switch (S_1–S_7)	GW30NC120HD
Gate driver circuit	M57962L
Modulating wave frequency	$f_m = 50$ Hz
Switching frequency	$f_c = 3000$ Hz
Modulation index	$m_a = 0.85$
Load resistance, inductance values	$R = 20\ \Omega, L = 20$ mH

An illustration of the output voltage and current waveform from the proposed FT MVSI is shown in Fig. 7 based on simulations under healthy, faulty and fault cleared conditions. In healthy condition (before $t = 0.94$ s), the proposed FT structure generates 5-level output voltage with identical voltage steps of 20 V each. For simulation study, an OSF is created at $t = 0.94$ s to $t = 1$ s in each of the switch(es), respectively. The state during the period of OSF is known as the faulty state. By the proposed FT control technique, the fault is cleared after $t = 1$ s and the output voltage waveforms change from unacceptable to acceptable for all switch failures except S_4 and S_6. In case of failure in power switches S_4 and S_6, a five-level output voltage waveform are obtained. It is evident from the above discussion that after the clearance of fault, a full fault-tolerant operation can be achieved when particular power switches S_4 and S_6 fail while failure in other switches as mentioned in Table 2 support partial fault tolerant operation.

Losses associated with the FT-MVSI topology can be analysed and assessed with the use of a thermal modelling simulation performed on the PLECS platform. The PLECS provides a domain for modelling thermal structures and accurately computing switching and conduction losses in switches utilzsing multi-dimensional lookup tables based on manufacturer information or real data. Further, IGBT (*GW30NC120HD*) switches have been employed as power switches in the PLECS-based simulation model, and the datasheet was imported in order to analyse power losses. The graph showing the steady state displays the loss patterns in Fig. 8. A remarkable total efficiency of 97.40 per cent characterizes the proposed topology. The experimental efficiency of the proposed inverter is 96.94%, which is somewhat less than the simulated efficiency due to losses in the driver units.
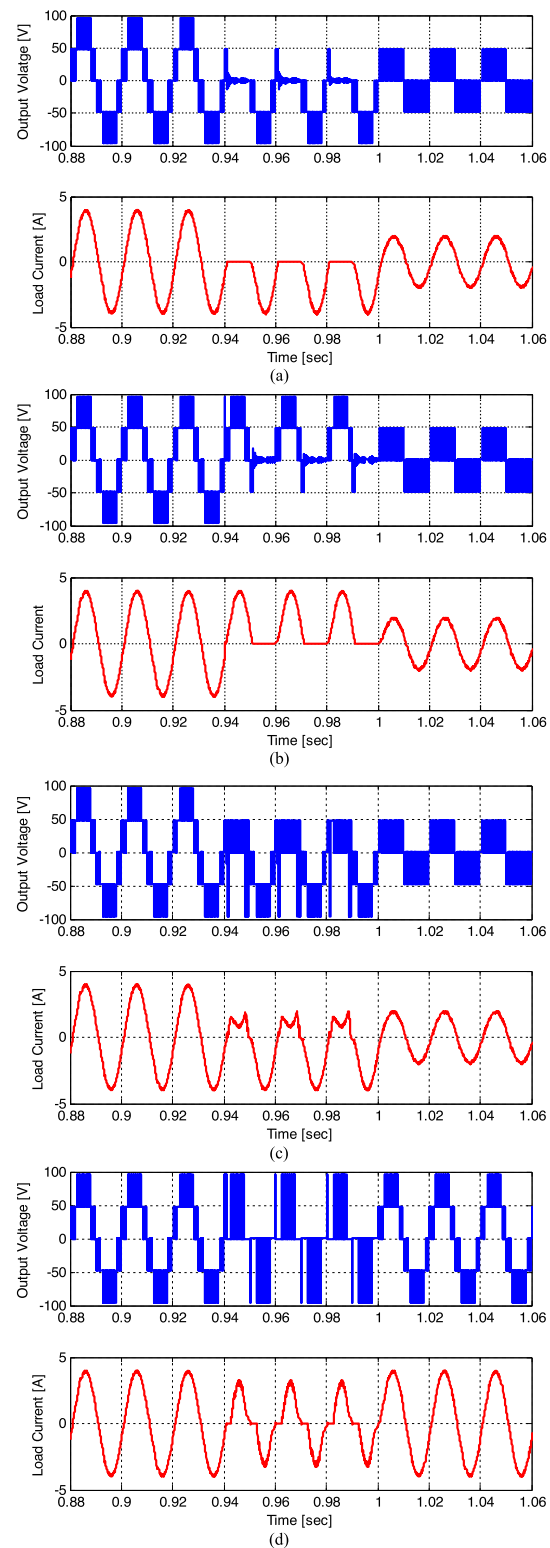

Fig. 7 Simulation results of FT MVSI: Output voltage and load current waveforms under OSF (normal, faulty and fault cleared conditions). **a** S_1 and/or S_2 failure, **b** S_2 and/or S_4 failure, **c** S_3 and/or S_5 failure, **d** S_4 failure, **e** S_5 and/or S_6 failure, **f** S_6 failure
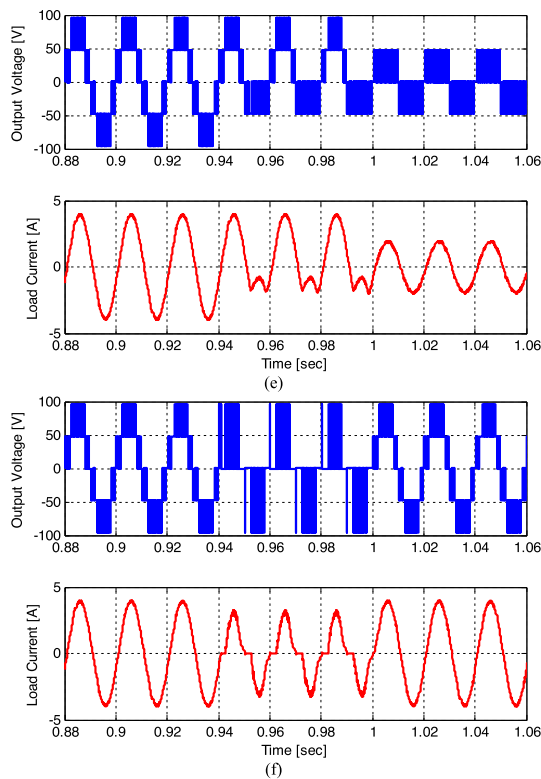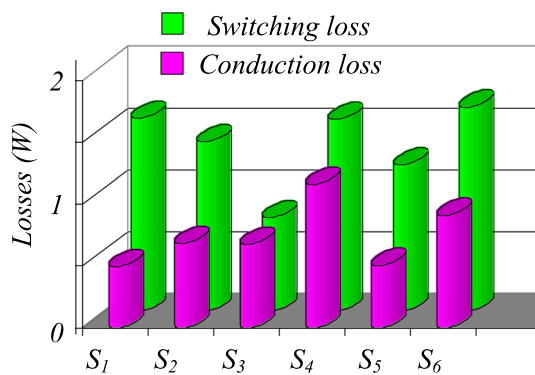
Fig. 7 continued

Fig. 8 Loss distribution graph on steady-state

5 Experimental validation and discussion

To validate the idea of the suggested FT control approach, the proposed FT-MLI is simulated using the MATLAB/SIMULINK software package, and the practical prototype is set up in an experimental setting. The prototype is developed experimentally to ensure that the aforementioned FT structure is feasible. A real-time digital controller, the dSPACE DS1104 is used for the generation of the switching

pulses. A host-PC operating the MATLAB/Simulink software tool, discrete power IGBT modules with built-in drivers and protection units, DC sources, a dSPACE1104 controller, a power quality analyzer (Fluke 43B), and a digital storage oscilloscope are all employed in the experimental setup. YOKOGAWA DL750E scope-coder is used to measure and record all the waveforms. Figure 9 shows the laboratory picture of the experimental setup.

In order to verify the proposed FT MVSI structure experimentally, a pre-programmed open circuit fault is created after $t = 0.94$ s on different switches and cleared at $t = 1$ s. In the duration of $t = 0.94$ s to $t = 1$ s, an unacceptable waveform is observed for individual switches. Figure 10a, b shows the transition of output voltage waveform from five to three level after fault inception. A partial fault-tolerant solution with reduced magnitude of voltage and current is observed for the proposed FT structure. Figure 10c shows the full fault-tolerant solution to the proposed FT structure.

The similar switch failures have been investigated in a simulation study, and the same results are observed. It is worth to note that the simulated and experimented results are identical to each other. Finally, the proposed FT-MLI structure is validated satisfactorily. The proposed FT MVSI is claimed to be reduced components FT-MLI. One of the key outcomes of presented studies is the continuous operation of proposed FT-MLI by adopting the proposed FT switching scheme in spite of the occurrence of OSF.

Also, the proposed topology is tested for THD under RL load which results in a good performance. Under this condition, the recorded output voltage and load current THD are 7.8% and 1.4% under healthy (before open-circuit fault) condition as illustrated in Fig. 11a, b, respectively.

Similarly, the proposed topology is tested for THD under a fault cleared state. Under this condition, the recorded output voltage and load current THD are 19.6% and 13.6% under fault cleared (after OC fault) condition as illustrated in Fig. 12a, b, respectively.

Notably, the value of THD can be increased by 5%, either by increasing the number of levels at the output or by increasing the switching frequency, although with the limitations of increased switching losses and reduced efficiency.

6 Comparision with recent fault-tolerant topologies

To illustrate the merits of proposed FT-MVSI, an appropriate comparison is carried out with classical and recently published MLIs. Table 6 summarizes the stated comparison. The comparison shows that the proposed FT structure requires
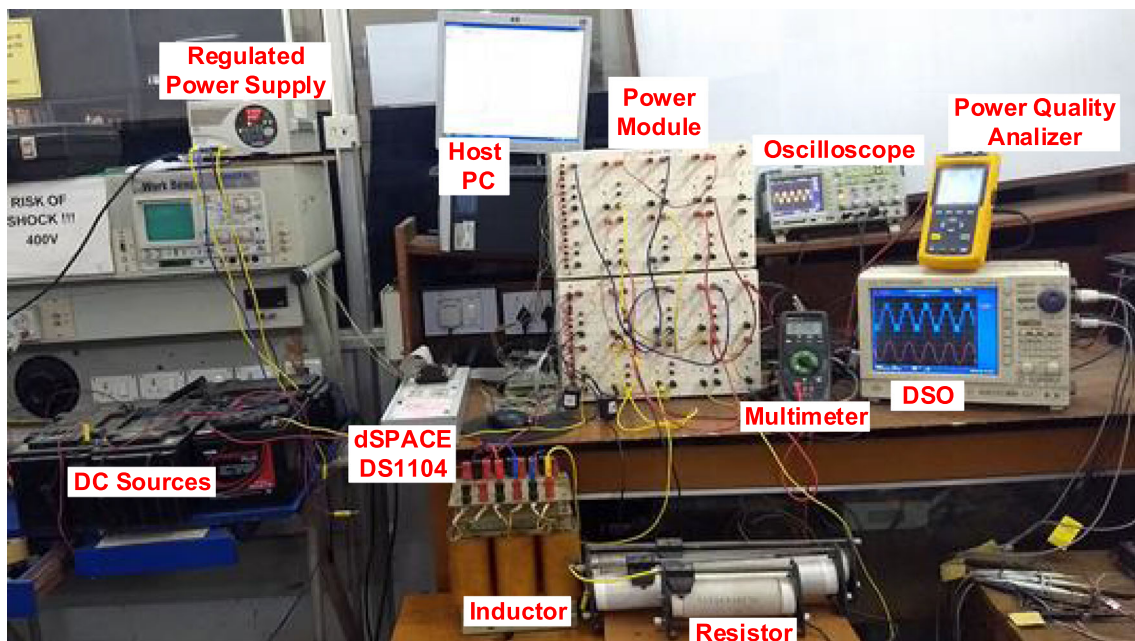
**Fig. 9** Picture of the experimental setup

fewer components for its reliable operation. While the structures in [14, 25, 28] and NPC comprise extra circuitry like clamping diodes which increase component count, whereas NPC does not possess FT operation. The proposed FT-MLI is highly competent to CHB along with minimum switch count. The structures in [22, 26, 27, 29] have higher switch count with FT ability in case of single OSF and unable to produce output voltage in case of multiple swich failure. The FT-MLI [28] requires more switches and highly competent to presented FT-MVSI in the event of multi switch failure scenario. Furthermore, four switches are conducting at an instant to generate a level in CHB, but in the proposed one, the conducting switches simultaneously (two) are less.

7 Conclusion

Reliability, continuity and fault related subjects in industries have been studied for decades and MLIs have become a key part in number of industry applications in which failures can have theatrical effects. An accident or fault in factory and industries can create vast economic and social losses. This research represents an approach to introducing fault-tolerant operation of single-phase MLI by considering either switch-open or multi-switch-open situation. The article has underlined the importance of the operation of the proposed FT structure even after OSF by providing continuous supply to the load with acceptable output voltage waveform. Simulation is used to prove the proposed concept, and experimental tests are used to verify the results. The obtained results prove the reliable operation of FT MVSI which can be achieved through the proposed FT control strategy. The current study has investigated for a MLI structure having symmetrical sources only. In addition to ensure fault tolerant operation in the event of a fault occurence in a single switch, the proposed fault tolerant strategy ensures fault tolerant operation in multiple switches as well. The proposed structure can be maintained at the rated voltage by using the step-up transformers in a faulty scenario.
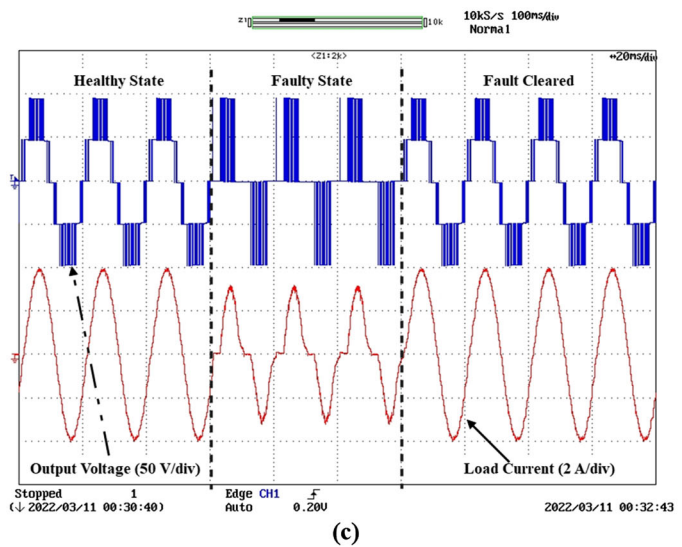
Fig. 10 Experimental results of FT MVSI: Output voltage (50 V/div) and load current (2A/div) waveforms under OSF (normal, faulty and the fault cleared conditions). **a** S_1 and/or S_2 failure, **b** S_2 and/or S_4 failure, **c** S_4 failure
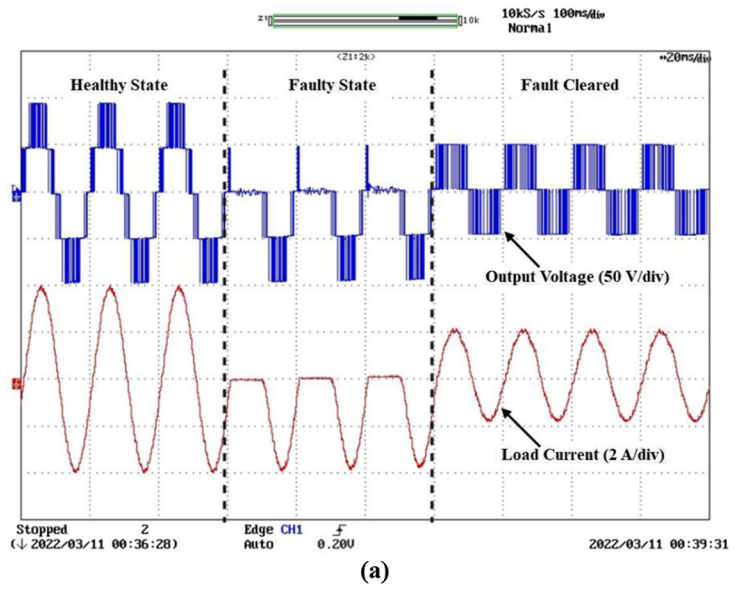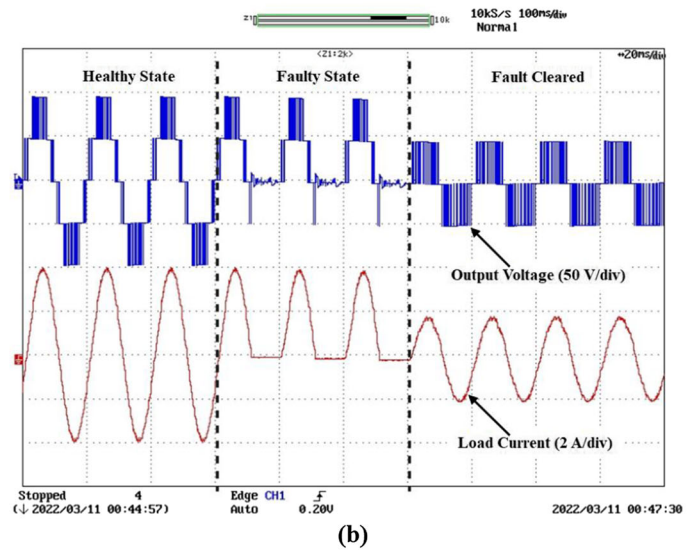
Fig.11 Experimental results of the proposed topology under healthy condition **a** Output voltage THD spectrum **b** current THD spectrum
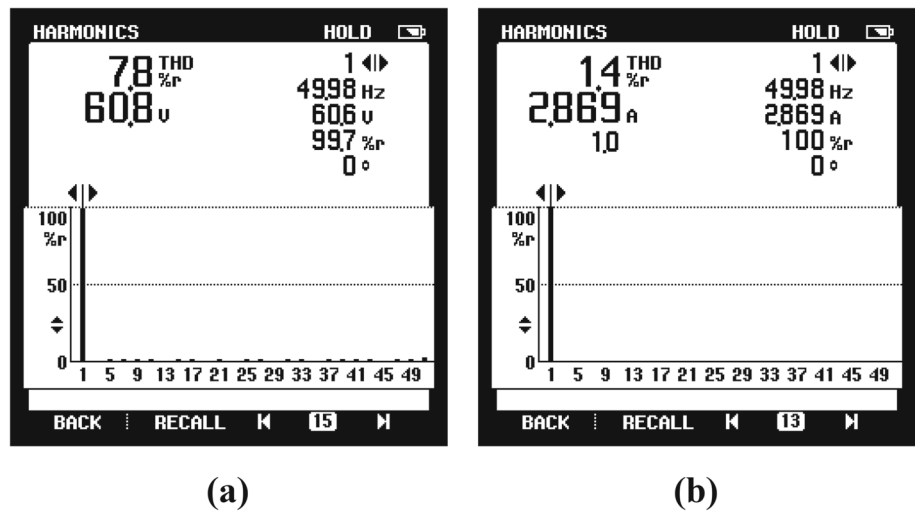
Fig.12 Experimental results of the proposed topology under fault cleared condition: **a** Output voltage THD spectrum, **b** current THD spectrum
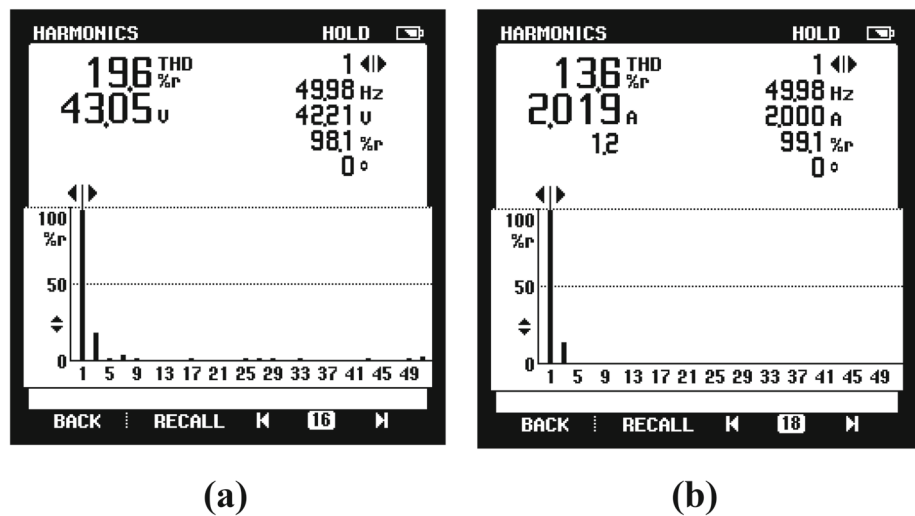
Table 6 Comparative study of the proposed FT-MLI with classical and recent literature

Components	FT-MVSI	Classical MLIs			References						
		NPC	FC	CHB	[14]	[25]	[26]	[27]	[28]	[29]	[22]
Input dc supply	2	1	1	2	2	1	4	1	2	1	2
DC Capacitors	0	4	10	0	0	2	0	8	0	10	0
Unidirectional switches	4	8	8	8	7	6	20	22	14	18	12
Bidirectional switches	2	0	0	0	2	1	0	0	0	0	0
Driver circuits	6	8	8	8	9	7	20	22	14	18	12
Clamping diodes	0	12	0	0	6	2	0	0	4	0	0
Fuses	0	0	0	0	0	0	0	0	4	0	0
Output Voltage (Healthy mode)	5-level	5-level	5-level	5-level	5-level	5-level	5-level	5-level	5-level	5-level	5-level
Fault tolerance	Yes	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
OSF (one of the switches)	Yes	No	No	Yes	No	No	No	Yes	Yes	Yes	Yes
Multi Switch failure	Yes	No	No	No	No	No	No	No	Yes	No	No

Declarations

Conflict of interest The Authors declare that there is no conflict of interest.

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