An improved Z-source inverter with high voltage boost ability

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Abstract

An improved high voltage boost Z-source inverter topology is proposed to improve voltage boost ability. Compared to the conventional Z-source inverter, it can produce very high voltage boost with a short shoot-through duty ratio, the voltage stress on Z-source capacitors and inverter-bridge is greatly reduced, and has inherent limitation to inrush current at startup. The addition of a input capacitor and an active switch allows the current in the Z source network to flow in the reverse direction, which adapts to a wide range of the load change. Theoretical analysis, the operation principle of the proposed topology and comparison with the conventional topology are explicitly described. Simulation and experimental results are presented to demonstrate the new features.

Keywords Z-source · Inverter · High voltage boost · Improve topology

1 Introduction

A Z-source inverter (ZSI) is proposed as the single-stage inverter topology to demonstrate both buck and boost power conversion ability in [1] as shown in Fig. 1. Z-source inverter has found widespread applications, and attracted the interest of researchers in recent years. Some scholars have carried out in ZSI applications such as photovoltaic power generation [2, 3], motor drive [4] and electric vehicle [5, 6]. There are also some scholars who have studied ZSI modeling analysis, modulation methods and topology improvements [7–13].

Despite the above advantages, the conventional ZSI also shows the some drawbacks, such as the voltage and current surge caused by starting, the limited boost capability and intermittent input current. In order to overcome the voltage stress across capacitors and inrush current at starting, a improved ZSI is proposed in [14]. In [15], a quasi-ZSI is recommended to solve the elements voltage stresses. However, as the conventional ZSI, the quasi-ZSI has no high voltage gain. High gain ZSI is introduced in [16, 17]. A high voltage

boost ZSI (HVB ZSI) in [17] is shown in Fig. 2, however the high number of passive elements increases the volume and loss of the inverter.

To reduce the high volume and weight, a switched-inductor ZSI has been presented to obtain high-voltage gains in [18], but it bears higher capacitor voltage stress than the conventional ZSI and quasi-ZSI. In [19–21], new switched-inductor inverters were proposed to enhance characteristics of the presented SBI in [18]. In [22, 23], the topologies for half-bridge SBI have been presented. The inverters use more active elements rather than capacitors and inductors. By using more active elements, switching loss can effectively reduce.

In this paper, an improved ZSI with high voltage boost ability (HVB-ZSI) is proposed. It employs a input capacitor and an active switch to make the current in the Z-source network to flow in the reverse direction, which makes inverter not only has high boost capacity but also has the ability to adapt to a wide range of load changes. In the following sections, different operating states of the improved HVB-ZSI are investigated. It has the advantages of low Z-source capacitor voltage stress and current surge limitation at startup. Theoretical analysis for the proposed topology is investigated and comparison with other topologies is also provided. The improved performance is validated by both simulated and experimental results.

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Fig. 1 Conventional ZSI

Fig. 2 HVB ZSI

2 Structure and working state

2.1 Structure of proposed Z-source inverter

The circuit of the improved HVB-ZSI is shown in Fig. 3. The circuit components are almost the same as the HVB-ZSI shown in Fig. 2. The difference is that the position of the inverter bridge and Z-source network is exchanged and their connection direction is reversed. It can suppress the start-up inrush current [9], and the damage of the inverter caused by the start-up inrush current is avoided. The second difference is that the active switch SW₇ and its control mode are added to the improved HVB-ZSI, the current in the improved Z source network can flow in the reverse direction. The diode D₁₃ ensures the current flowing in one direction of the supply, and input capacitor C_{in} is added to the input side to provide a path for the reverse current, therefore the quality of the output voltage is improved.

In Fig. 3, assuming that $C_1 = C_2$, $L_1 = L_2 = L_3 = L_4 = L_5 = L_6$, the network becomes symmetrical. From the symmetry circuits, the voltages across capacitors and inductors are shown in Eq. 1

Fig. 3 Topology of the proposed ZSI

$$\begin{aligned} V_{C1} &= V_{C2} = V_C \\ V_{L1} &= V_{L2} = V_{L3} = V_{L4} = V_{L5} = V_{L6} = V_L \end{aligned} \quad (1)$$

2.2 Operating state of proposed Z-source inverter

There are 9 switching states of the proposed HVB-ZSI, including a shoot-through zero vector state, two traditional zero-vector states and 6 effective vector states. According to the current direction, there are 8 operating states of the proposed HVB-ZSI, as shown in Fig. 4. In addition, the inverter side can be simplified by an equivalent current source when the inverter is in the effective vector state.

- (1) State 1: The inverter is in the shoot-through zero vector state and the active switch SW₇ is off, as shown in Fig. 4a. Although the inverter is in the shoot-through zero state, the inductor current cannot change suddenly. The freewheeling diodes of the inverter arm are on, the dc-link voltage V_i is clamped to zero by freewheeling diodes, and three inductors of the Z-source network are connected in parallel. The inductor currents flow in reverse and decrease. The voltage across inductors can be expressed as

$$V_L = V_{dc} + V_C \quad (2)$$

where V_{dc} is the input dc voltage.

- (2) State 2: The inverter is still in the shoot-through zero vector state and the active switch SW₇ is also off, as shown in Fig. 4b. At this time, because the switch tube of the inverter bridge arm is turned on, the Z source network capacitors and the input capacitor charge

Fig. 4 Operating states. **a** State 1, **b** State 2, **c** State 3, **d** State 4, **e** State 5, **f** State 6, **g** State 7, and **h** State 8

inductors. The inductor current increases positively, and the dc link voltage V_i is still zero.

- (3) State 3: The inverter is in the traditional zero-vector state and the input current is zero. The dc power source charges to the input capacitor C_{in} , and the inductors of the Z-source network charge to the capacitors, as shown in Fig. 4c. At the moment, three inductors of the Z-source network are connected in series. The voltages of dc link and inductors can be expressed as follows.

$$\begin{aligned} V_i &= V_{dc} + 2V_C \\ 3V_L &= -V_C \end{aligned} \quad (3)$$

- (4) State 4: The inverter runs in a valid vector state, as shown in Fig. 4d. The inductors current i_L and the free-wheeling diode current i_D of the active switch SW7 satisfy the following inequality (4).

$$i_D > 0 \quad i_L > ii \quad (4)$$

In this state, the power supply directly delivers power to the load, and the Z-source network inductors charge to the capacitors.

$$V_i = V_{dc} + 2V_C.$$

- (5) State 5: The inverter is in the valid vector state, as shown in Fig. 4e. In this state, as the inductors current i_L continue to decrease, the capacitors of the Z-source network supply power to the load. In this case, the inductors current i_L satisfies the inequality (5).

$$\frac{1}{2}i_i < i_L < i_i \quad (5)$$

- (6) State 6: The inverter is still in the valid vector state, as shown in Fig. 4f. The inductors' current satisfy the inequality (6).

$$0 < iL < \frac{1}{2}ii \quad (6)$$

At the end of state 5, the active switch SW7 starts to conduct, the input current is less than zero and flows in reverse.

- (7) State 7: The inverter is in the valid vector state and the active switch SW7 is still closed, as shown in Fig. 4g. But at this time the inductors' current drop to zero and then increase in the opposite direction. The capacitors of the Z-source network discharge to inductors and load.

- (8) State 8: The inverter is in the traditional zero-vector state, as shown in Fig. 4h. The dc power supply charges to the input capacitor. The inductors' current continues to flow in the opposite direction, and the Z-source network capacitors discharge to inductors.

According to the analysis of the above 8 states, we can see that the dc link voltage V_i of the proposed ZSI is equal to $(V_{dc} + 2V_C)$ in the valid vector state and the traditional zero-vector state. In this way, the dc link voltage will not be distorted in the all operating states, which eliminates the three special abnormal operating states when the conventional Z-source inverter is under the light load or small inductance.

2.3 Control strategy of switch SW7

According to the 8 operating states of the above circuit, the active switch SW7 can provide a reversely flowing path for the reverse current, and the output current meets the requirement of load current. The switch SW7 is off in state 1 and state 2 of the shoot-through state, the current flows through the freewheeling diode of SW7 in mode 3, 4 and 5 of the non shoot-through state, and the switch SW7 is on in state 6, 7 and 8. So, the driving signal of the switch SW7 is opposite to the shoot-through signal.

3 Analysis of proposed Z-source network

The 8 operating states in Fig. 4 can be simplified. If the voltage relationship of the circuit is only considered, the operating states can be simplified into two operating states, that is, the shoot-through state and the non shoot-through state. Figure 5 shows the equivalent circuit of the proposed topology shown in Fig. 3 when viewed from the inverter side. The inverter bridge is equivalent to a short circuit when the inverter bridge is in the shoot-through zero state, as shown in Fig. 5a. From Fig. 5a, we have

$$\begin{aligned} V_L &= V_{dc} + V_C \\ V_i &= 0 \end{aligned} \quad (7)$$

The inverter bridge becomes an equivalent current source as shown in Fig. 5b when in the non-shoot-through state. The following equations can be derived in this state:

$$\begin{aligned} 3V_L &= -V_C \\ V_i &= V_{dc} + V_C - 3V_L \end{aligned} \quad (8)$$

The average value of the inductor voltage over one switching period should be zero in the steady state, the shoot-through duty cycle is D , from (7) and (8), we can get

Fig. 5 Equivalent circuit. **a** Shoot-through state and **b** non-shoot-through state

$$V_C = \frac{3D}{1-4D} V_{dc} \quad (9)$$

The peak dc-link voltage across the inverter bridge is expressed as

$$V_i = \frac{1+2D}{1-4D} V_{dc} = B V_{dc} \quad (10)$$

$$B = \frac{1+2D}{1-4D} \quad (11)$$

where B is the boost factor. The boost factors of the conventional Z-source inverter [1] and HVB-ZSI [13] are expressed as follows

$$\begin{aligned} B_2 &= \frac{1}{1-2D} \\ B_3 &= \frac{1+2D}{1-4D} \end{aligned} \quad (12)$$

The comparison of B in the three topologies is shown in Fig. 6 obtained from (11) and (12). From Fig. 6, it is obvious that the boost ability of the proposed HVB-ZSI is higher than the conventional ZSI when the shoot-through duty cycle D is same. The proposed HVB-ZSI has the same boost factor as the HVB-ZSI.

4 Analysis of three topologies

4.1 Voltage gain

The voltage gain G of the ZSI is the product of the voltage boost factor B and the modulation index M and it is determined by the modulation index and boost factor. The boost factors as expressed in (11) and (12) can be controlled by duty cycle of the shoot-through zero state over the non-shoot-through

Fig. 6 B versus D of the three topologies

state of the inverter PWM. The simple boost control method is used in this paper. For a given shoot-through duty ratio D , the maximum value of M is $(1 - D)$. The maximum voltage gain G value of the proposed HVB-ZSI is shown in Eq. 13.

$$G_{\max} = MB = (1 - D) \frac{1 + 2D}{1 - 4D} \quad (13)$$

The voltage gains of the conventional ZSI [1] and the HVB-ZSI [14] and can be expressed as follows

$$\begin{aligned} G_{\max 2} &= MB = (1 - D) \frac{1}{1 - 2D} \\ G_{\max 3} &= MB = (1 - D) \frac{1 + 2D}{1 - 4D} \end{aligned} \quad (14)$$

Figure 7 shows the maximum voltage gain G versus D of the proposed HVB-ZSI, HVB-ZSI and the conventional ZSI obtained from Eqs. 13 and 14. According to Fig. 7, we can see that the maximum voltage gain G of the proposed HVB-ZSI is the same as that of HVB-ZSI and is much higher than that of the conventional ZSI under the same shoot-through duty ratio D . It means that a smaller D is used in the proposed HVB-ZSI to output the same ac voltage.

4.2 Capacitor voltage

Based on the above analysis, it can be seen that the Z-source capacitor voltage stress of the proposed HVB-ZSI is shown in Eq. (9). The capacitor voltages of the conventional ZSI and the HVB-ZSI are expressed as

$$\begin{aligned} V_{C2} &= \frac{1D}{1 - 2D} V_{dc} \\ V_{C3} &= \frac{1 - D}{1 - 4D} V_{dc} \end{aligned} \quad (15)$$

Figure 8 shows the comparison of V_c/V_{dc} in the three topologies. As shown in Fig. 8, when D increases, so do the

Fig. 7 G versus D of the three topologies

capacitor voltages V_c of the three topologies. However, it can be seen that the capacitor voltage stress of the proposed HVB-ZSI is significantly lower than HVB-ZSI under the same shoot-through duty ratio D . If the voltage gains of the three inverter topologies are same, the D of the proposed HVB-ZSI can be expressed as

$$D = \frac{(4G + 1) - \sqrt{16G^2 + 9}}{4} \quad (16)$$

Substituting (16) into (9), the Z-source capacitor voltage stress of the proposed HVB-ZSI is expressed as

$$V_C = \frac{3(4G + 1) - 3\sqrt{16G^2 + 9}}{4(\sqrt{16G^2 + 9} - 4G)} V_{dc} \quad (17)$$

The capacitor voltage stress of the conventional ZSI and HVB-ZSI can be expressed as

$$\begin{aligned} V_{C2} &= GV_{dc} \\ V_{C3} &= \frac{\sqrt{16G^2 + 9} - (4G - 3)}{4(\sqrt{16G^2 + 9} - 4G)} V_{dc} \end{aligned} \quad (18)$$

The comparison of V_c/V_{dc} in the three topologies is shown in Fig. 9. From Fig. 9, it is obvious that the Z-source capacitor voltage stress of the proposed HVB-ZSI is much lower than that of the conventional ZSI and the HVB-ZSI under the same voltage gain G .

4.3 Z-source inductor current ripple

The average Z-source inductor current equals the average input current. Therefore, for the proposed topology during the non-shoot-through state, the Z-source inductor current decreases and the current ripple can be expressed as

Fig. 8 V_c/V_{dc} versus D and of the three topologies

Fig. 9 V_c/V_{dc} versus G of the three topologies

$$\Delta i_L = \frac{(1-D)TV_c}{3L} \quad (19)$$

Substituting (9) into (19), the current ripple is expressed as follows

$$\Delta i_L = \frac{(1-D)DT}{L(1-4D)} V_{dc} \quad (20)$$

For the conventional ZSI and HVB-ZSI, however, during the non-shoot-through state, the current ripple can be expressed as

$$\Delta i_{L2} = \frac{(1-D)DTV_{dc}}{L(1-2D)} \quad (21)$$

$$\Delta i_{L3} = \frac{(1-D)DTV_{dc}}{L(1-4D)} \quad (22)$$

From (20) and (22), we can see that the current ripple of the proposed HVB-ZSI is the same that of HVB-ZSI.

If the input voltages are same, at a given voltage gain G , the inductor current ripple of the proposed HVB-ZSI and HVB-ZSI under simple boost control can be expressed as (23), and the inductor current ripple of the conventional ZSI can be expressed as (24).

$$\Delta i_L = \frac{(1-2G)(3-2G)TV_{dc}}{4(4G-3)L} = k_1 \frac{TV_{dc}}{L} \quad (23)$$

$$\Delta i_{L2} = \frac{(G-1)GTV_{dc}}{(2G-1)L} = k_2 \frac{TV_{dc}}{L} \quad (24)$$

where k_1 and k_2 are the inductor current ripple coefficient, Fig. 10 shows the comparison of the inductor current ripple coefficient k of three topologies.

Fig. 10 k versus G of the three topologies

From Fig. 10, we can know that the inductor current ripple coefficient of the proposed HVB-ZSI and HVB-ZSI is significantly lesser than the conventional ZSI under the same voltage gain G .

4.4 Power tube voltage stress

The voltage stress on the power tubes of the proposed HVB-ZSI is the peak dc-link voltage. Under the simple boost control, the power tube voltage stress V_s of the proposed HVB-ZSI can be expressed as

$$V_s = BV_{dc} = \frac{(4G+3) - \sqrt{16G^2+9}}{2(\sqrt{16G^2+9}-4G)} V_{dc} \quad (25)$$

The power tube voltages of the conventional ZSI and HVB-ZSI can be expressed as

$$V_{s2} = (2G-1)V_{dc} \quad (26)$$

$$V_{s3} = BV_{dc} = \frac{(4G+3) - \sqrt{16G^2+9}}{2(\sqrt{16G^2+9}-4G)} V_{dc}$$

The comparison of V_s in the three topologies is shown in Fig. 11. As shown in Fig. 11, the power tube voltage stress on the inverter-bridge of the proposed HVB-ZSI and the HVB-ZSI is much smaller than that of the conventional ZSI under the same voltage gain G .

4.5 Comparison with other topologies

Table 1 compares different features of the proposed HVB ZSI with other topologies. As shown in Table 1, the proposed HVB ZSI and HVB ZSI have the most passive components. Moreover, the proposed HVB ZSI has the moderate switches and totally the most components in Table 1.

Fig. 11 V_s / V_{dc} versus voltage gain G

In the proposed HVB ZSI, when the shoot-through duty cycle is moderate, the voltage stresses of the switches, diodes and capacitors are lower than HVB ZSI. Compared with other topologies, the proposed HVB ZSI and HVB ZSI have the highest boost factor. Among the topologies of Table 1, proposed HVB ZSI and HVB ZSI have highest inductor current stresses. Due to the highest voltage gain, the inverter outputs the largest power.

Voltage stress of the components based on the voltage gain is shown in Table 2. It can be seen from Table 2 that the voltage stress of the components is related to the voltage gain and the input voltage. In order to better compare the voltage stress of different topologies, the corresponding results are shown in Table 3 when $G=2$ and $V_{dc}=100$ V. It can be seen from Table 3 that the proposed HVB ZSI has the lowest diode voltage and capacitor voltage stress.

Table 1 Comparison of different three-phase topologies

	Proposed HVB ZSI	HVB ZSI [17]	Improved ZSI [14]	EB qZSI [15]	SBI [18]	Embedded-Type qSBI [20]	HB-SBI [7]	Conventional ZSI [1]
Switch	7	6	6	7	7	7	8	6
Diode	14	13	1	4	2	2	4	1
Inductor	6	6	2	2	1	1	2	2
Capacitor	2	2	2	2	1	1	2	2
Voltage stress on switches	$\frac{(1+2D)(1-D)}{3D}V_c$	$(1+2D)V_c$	V_c	$V_{c1} = V_{c1}$ $V_{D1,2} = V_{c1}$	V_c	V_c	$2V_c$	V_c
Voltage stress on diodes	$\frac{1+2D}{3}V_c$	$\frac{D(1+2D)}{1-D}V_c$	V_c	$V_{D3} = 2(1-D)V_{c1}$ $V_{D4} = 2DV_{c1}$ $V_{c1} = \frac{1}{1-4D+2D^2}V_{dc}$	$V_{Da} = \frac{D^2}{1-D}V_c$ $V_{Db} = DV_c$	V_c	$2V_c$	V_c
Capacitor voltage	$\frac{3D}{1-4D}V_{dc}$	$\frac{1-D}{1-4D}V_{dc}$	$\frac{D}{1-2D}V_{dc}$	$V_{c2} = \frac{1-2D}{1-4D+2D^2}V_{dc}$	$\frac{1-D}{1-2D}V_{dc}$	$\frac{1}{1-2D}V_{dc}$	$\frac{1-D}{2(1-3D)}V_{dc}$	$\frac{1-D}{1-2D}V_{dc}$
Boost factor	$\frac{1+2D}{1-4D}$	$\frac{1+2D}{1-4D}$	$\frac{1}{1-2D}$	$\frac{1}{1-4D+2D^2}$	$\frac{1-D}{1-2D}V_{dc}$	$\frac{1}{1-2D}$	$\frac{1-D}{2(1-3D)}$	$\frac{1}{1-2D}$
Inductor current	$\frac{1-D}{1-4D}I_i$	$\frac{1-D}{1-4D}I_i$	$\frac{1-D}{1-2D}I_i$	$I_{L1} = \frac{1-D}{1-4D+2D^2}I_i$ $I_{L2} = \frac{(1-D)^2}{1-4D+2D^2}I_i$	$\frac{1-D}{1-2D}I_i$	$\frac{1-D}{1-2D}I_i$	$\frac{1-D}{1-3D}I_i$	$\frac{1-D}{1-2D}I_i$

Table 2 voltage stress of the components based on the voltage gain

	Proposed HVB ZSI	HVB ZSI [17]	Improved ZSI [14]	SBI [18]	Embedded-Type qSBI [20]	HB-SBI [7]	Conventional ZSI [1]
Voltage stress on switches	$\frac{(4G+3)-\sqrt{16G^2+9}}{2(\sqrt{16G^2+9}-4G)}V_{dc}$	$\frac{(4G+3)-\sqrt{16G^2+9}}{2(\sqrt{16G^2+9}-4G)}V_{dc}$	$(G-1)V_{dc}$	GV_{dc}	GV_{dc}	$2GV_{dc}$	GV_{dc}
Voltage stress on diodes	$\frac{8G^2+4G+3-(2G+1)\sqrt{16G^2+9}}{2(\sqrt{16G^2+9}-4G)}V_{dc}$	$\frac{8G^2+4G+3-(2G+1)\sqrt{16G^2+9}}{2(\sqrt{16G^2+9}-4G)}V_{dc}$	$V_{dc}(G-1)$	GV_{dc}	GV_{dc}	$2GV_{dc}$	GV_{dc}
Capacitor voltage	$\frac{3(4G+1)-3\sqrt{16G^2+9}}{4(\sqrt{16G^2+9}-4G)}V_{dc}$	$\frac{\sqrt{16G^2+9}-(4G-3)}{4(\sqrt{16G^2+9}-4G)}V_{dc}$	$(G-1)V_{dc}$	GV_{dc}	GV_{dc}	GV_{dc}	GV_{dc}

Table 3 Voltage stress values when $G=2$ and $V_{dc}=100$ V

	Proposed HVB ZSI (V)	HVB ZSI (V) [17]	Improved ZSI (V) [14]	SBI (V) [18]	Embedded-Type qSBI (V) [20]	HB-SBI (V) [7]	Conven- tional ZSI (V) [1]
Voltage stress on switches	234	234	100	200	200	400	200
Voltage stress on diodes	25.7	25.7	100	200	200	400	200
Capacitor voltage	62.9	138	100	200	200	200	200

Fig. 12 Gate PWM control signal

5 Simulation and experiment results

5.1 Simulation results

The above analysis was confirmed by simulation. The simulation results were given to confirm the above advantages of the proposed HVB-ZSI. Simple boost control is used in simulation. Two straight lines to control the shoot-through states are used, as shown in Fig. 12. When the triangular waveform is greater than the upper envelope, V_p , or lower than the bottom envelope, V_n , the circuit turns into

shoot-through state. Otherwise it operates just as traditional carrier-based PWM.

The simulation parameters are:

- (1) Z-source network: $L_1=L_2=L_3=L_4=L_5=L_6=500\ \mu\text{H}$, $C_1=C_2=1200\ \mu\text{F}$;
- (2) Output filter: $L=1500\ \mu\text{H}$, $C_f=50\ \mu\text{F}$;
- (3) Switching frequency: 10 kHz;
- (4) Three-phase resistance load $R=15\ \Omega/\text{phase}$;

Case 1: $V_{dc}=100$ V, the shoot-through duty ratio $D=0.1925$, the modulation ratio $M=0.8075$. In this case, according to the above analysis, we can get $B=6$, $G=4.863$, $V_C=251$ V, $V_i=600$ V.

The simulation results of the proposed HVB-ZSI are shown in Fig. 13a. From Fig. 13a, we can see that in the proposed HVB-ZSI, V_C is boosted to 250 V in steady state, V_i is boosted to 600 V, and the inrush current is much smaller than the conventional one.

Figure 13b shows the simulation results of the HVB-ZSI. From Fig. 13b, it is obvious that V_C is boosted to 380 V, V_i is boosted to 600 V, and there's a huge inrush current at start. V_C is quickly charged to 540 V. Then, the impulse voltage and impulse current may damage the inverter.

From the Fig. 13, we can see that the voltage boost capability of the two HVB-ZSI topologies is the same under the same D and M , the capacitor voltage of the proposed HVB-ZSI is less than that of the HVB-ZSI and inrush current at start-up is also significantly reduced.

The input diode D_{13} current, capacitor voltage, switch SW7 current and voltage of the proposed HVB-ZSI are shown in Fig. 14. It can be seen from these results, D_{13} current, capacitor voltage V_C , and switch SW7 current and voltage are about 350 A, 252 V, 90 A and 600 V, respectively, in the steady-state condition. The simulation results are consistent with the theoretical analysis.

Figure 15 shows the input diode D_{in} current and capacitor voltage of HVB-ZSI. It can be seen that the current and capacitor voltage are about 140 A and 373 V in the steady state condition, which are larger than the proposed HVB-ZSI.

The DC link voltage and the inductor current simulation waveforms of the proposed HVB-ZSI and the HVB-ZSI at

Fig. 13 Simulation results in case 1. **a** Proposed HVB-ZSI and **b** HVB-ZSI

Fig. 14 Simulation waveforms of I_{D13} , V_C , I_{SW7} and V_{SW7}

the light load ($R = 300\Omega$ $L_f = 10$ mH) are shown in Fig. 16. From Fig. 16, it can be seen that the DC link voltage distortion of HVB-ZSI has happened in the non-through state,

Fig. 15 Simulation waveforms of I_{D13} , V_C , of HVB-ZSI

Fig. 16 DC-link voltage and inductor current at light load. **a** Proposed HVB-ZSI and **b** HVB-ZSI

while the proposed HVB-ZSI can eliminate the light-load DC link voltage distortion. The simulation results verify the correctness of theoretical analysis.

Case 2: The proposed HVB-ZSI is to produce a three-phase peak ac voltage 220 V. By theoretical calculations, $D=0.1461$, $M=0.8539$, $B=3.11$ and $G=2.656$, the capacitor voltage V_C is boosted to 105 V and the DC link voltage V_i is equal to 311 V. The simulation results for the proposed ZSI are shown in the Fig. 17a in this case.

In the case of the HVB-ZSI, in order to output the same ac voltage, the shoot-through duty ratio is 0.1461 and the modulation ratio M is 0.8539. The simulation results for the HVB-ZSI are shown in the Fig. 17b. From Fig. 17b, we can see that V_C is boosted to 205 V and V_i is boosted to 311 V. The capacitor voltage stress is greatly increased and huge inrush current occurs at startup.

To study dynamic response of the proposed HVB ZSI, assuming that the input voltage of the proposed HVB ZSI suddenly drops from 200 to 150 V at 0.5 s, the capacitor voltage begins to drop from the original 160 V, and the DC link voltage drops from 550 V. At the same time, due

to the adjustment of the voltage and current double loops, the shoot-through duty cycle D begins to rise, which make capacitor voltage rapid rise to compensate for the input voltage drop. After 0.2 s adjustment, D was increased from 0.11 to 0.18, and the capacitor voltage and output voltage remain unchanged after a short period of adjustment. The whole process is shown in Fig. 18.

5.2 Study on efficiency and power loss

The efficiency and power loss of proposed HVB ZSI and HVB ZSI are further studied. The power loss calculation method of component in [23] is used. The power loss of the proposed HVB-ZSI and HVB-ZSI are calculated according to the parameters summarized in Table 4 for $V_{dc}=100$ V and $B=6$.

The input power and output power of the proposed HVB ZSI are about 450 W and 370 W and the efficiency is 82.24%, but output power of HVB ZSI are only 344 W and the efficiency is only 76.44%. Figure 19 shows the power losses simulation results. The power loss of both inverters is calculated as [24]. It can be seen from Fig. 19 that the total power loss of the proposed HVB-ZSI is about 80 W and the total power loss of the HVB-ZSI is about 106 W.

The efficiency curve of the proposed HVB ZSI and HVB ZSI under different output power values is shown in Fig. 20 according to parameters shown in Table 4 when $V_{dc}=100$ V and the output voltage is 220 V. The value of output power is changed by changing the output load (R), and the efficiency values of different output powers are obtained. The efficiency calculation is based on the power loss equations in [24]. From Fig. 20, it can be seen that the efficiency of the proposed HVB ZSI is higher than that of HVB ZSI.

Fig. 17 Simulation results in case 2. **a** Proposed HVB-ZSI and **b** HVB-ZS

Fig. 18 Dynamic response results

Table 4 Parameters for the efficiency and power loss

Component	Type	Parameters	Values	Parameters	Values
Switches	IGW40N60H3 (600 V, 40 A, Infineon)	V_{FS}	1.75 V	R_s	0.21Ω
Diodes	RNRG3060 (600 V, 30 A, Semiconductor)	V_{FD}	0.6 V	R_D	0.09Ω
Inductors	CS467090 (202nH/N2)	R_L	0.18Ω	f	10 kHz
				B	6
Capacitors ELH12WM102R70KT	R_C	0.03Ω	V_{dc}	100 V	
(1000 μ F/450 V, Aishi)

Fig. 19 Power loss simulation results **Fig. 20** Efficiency under different output power **Fig. 21** Experimental prototype **Fig. 22** Main component volumes

5.3 Experiment results

A hardware circuit, as shown in Fig. 21, was built. The main component parameters are shown in Table 4.

Figures 22 and 23 show the comparison of main components size and weight between two inverters. The main component parameters are shown in the Table 4. Size and weight of each component can be obtained from the data-sheet. It can be seen from Figs. 22 and 23 that volumes and weights of the proposed HVB ZSI have decreased by 17.2% and 24.8% respectively compared with those of the

HVB ZSI. From the aforementioned power loss, the HVB ZSI has higher power loss than the proposed HVB ZSI. So for heat dissipation, volume and weight of the heat sink of HVB ZSI is larger than those of the proposed HVB ZSI.

Figures 24 and 25 show experimental results. Figure 24 shows the experimental results in case 1. V_C is about

Fig. 23 Main component weights

Fig. 24 Experimental results in case 1

Fig. 25 Experimental results in case 2

250 V, V_i is boosted to 600 V, and the peak output line voltage is 420 V. Figure 25 shows the experimental results in case 2. V_c is 105 V, V_i is boosted to 415 V, and the output line voltage is 220 V.

5.4 Conclusion

This paper has presented a new Z-source inverter topology with high voltage boost ability. Compared to the previous Z-source inverter with high voltage boost ability, the new topology has following unique features and advantages: (1) The Z-source capacitor voltage stress is reduced greatly under the same boost ability; (2) The ability to adapt to a wide range of load increases the quality of the output voltage; (3) The inrush current can be suppressed with a proper start control strategy. The improved performance of the proposed ZSI is confirmed by simulation and experimental results.

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References

- Peng F (2003) Z-source inverter. *IEEE Trans Ind Appl* 39(2):504–510
- Sun D, Ge B, Liang W, Abu-Rub H, Peng FZ (2015) An energy stored quasi-Z-source cascade multilevel inverter-based photovoltaic power generation system. *IEEE Trans Ind Electron* 62(9):5458–5467
- Kim K, Cha H, Kim H-G (2017) A new single-phase switched-coupled-inductor DC–AC inverter for photovoltaic systems. *IEEE Trans Power Electron* 32(7):5016–5022
- Neve VS, Zope PH, Suralkar SR (2013) Analysis and simulation of Z-source inverter fed to single phase induction motor drive. *Int J Sci Eng Technol* 2(1):08–12
- Ellabban O, Van Mierlo J, Lataire P (2013) Control of a bidirectional Z-source inverter for electric vehicle applications in different operation modes. *J Power Electron* 11(2):120–131
- Sideng Hu, Liang Z, He X (2016) Ultra capacitor-battery hybrid energy storage system based on the asymmetric bi-directional Z-source topology for EV. *IEEE Trans Power Electron* 31(11):7489–7498
- Babaei E, Asl ES, Babayi MH (2016) Steady-state and small-signal analysis of high-voltage gain half-bridge switched boost inverter. *IEEE Trans Ind Electron* 63(6):3546–3553

8. Babaei E, Shokati Asl E (2016) A new topology for Z-source half-bridge inverter with low voltage stress on capacitors. *Elect Power Syst Res* 140:722–734
9. Ahmad A, Bussa VK, Singh RK, Mahanty R (2018) Switched-boost-modified Z-source inverter topologies with improved voltage gain capability. *IEEE J Emerg Sel Top Power Electron* 6(4):2227–2244
10. Abbasi M, Eslahchi AH, Mardaneh M (2018) Two symmetric extended-boost embedded switched-inductor quasi-Z-source inverter with reduced ripple continuous input current. *IEEE Trans Ind Electron* 65(6):5096–5104
11. Rostami H, Azizian MR, Alireza Davari S, Rad SM (2021) Single-phase three-level neutral-point-clamped inverter based on modified Z-source network with reduced voltage stress on capacitors. *IEEE J Emerg Sel Top Power Electron* 9(1):980–993
12. Pan X, Pang Z, Liu Y, Yin S (2020) Enhanced-boost bidirectional quasi-Z-source inverter with novel active switched inductor cells. *IEEE J Emerg Sel Top Power Electron* 8(3):3041–3055
13. Mohammadi M, Moghani JS, Milimonfared J (2018) A novel dual switching frequency modulation for Z-source and quasi-Z-source inverters. *IEEE Trans Ind Electron* 65(6):5167–5176
14. Tang Y, Xie S, Zhang C (2011) An improved Z-source inverter. *IEEE Trans Power Electron* 26(12):3865–3868
15. Yuanwei Gu, Chen Y, Zhang Bo (2018) Enhanced-boost quasi-Z-source inverter with an active switched Z-network. *IEEE Trans Ind Electron* 65(10):8372–8381
16. Lei P (2014) L-Z-source inverters. *IEEE Trans Power Electron* 29(12):6534–6543
17. Trinh Q-N, Lee H-H (2012) A new Z-source inverter topology with high voltage boost ability. *J Electr Eng Technol* 7(5):714–723
18. Ravindranath A, Mishra SK, Joshi A (2013) Analysis and PWM control of switched boost inverter. *IEEE Trans Ind Electron* 60(12):5593–5602
19. Meinagh FAA, Babaei E, Tarzamni H (2017) Modified high voltage gain switched boost inverter. *IET Power Electron* 10(13):1655–1664
20. Nguyen M-K, Le T-V, Park S-J, Lim Y-C (2015) A class of quasi-switched boost inverters. *IEEE Trans Ind Electron* 62(3):1526–1536
21. Zhu X, Zhang Bo, Qiu D (2019) A high boost active switched quasi-Z-source inverter with low input current ripple. *IEEE Trans Ind Inf* 15(9):2341–2354
22. Asl ES, Babaei E, Sabahi M (2017) High voltage gain half-bridge quasi-switched boost inverter with reduced voltage stress on capacitors. *IET Power Electron* 10(9):1095–1108
23. Babaei E, Asl ES (2017) High-voltage gain half-bridge Z-source inverter with low-voltage stress on capacitors. *IEEE Trans Ind Electron* 64(1):191–197
24. Shen M, Joseph A, Wang J, Peng FZ, Adams DJ (2007) Comparison of traditional inverters and Z-source inverter for fuel cell vehicles. *IEEE Trans Power Electron* 22(4):1453–1463

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