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# Low-Power Energy Harvesting Voltage Doubler Using CTLs Based on Inverse Class-F Configuration Compatible with Fifth Generation

**Marwa Mansour**[1]

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## Abstract

This paper introduces a highly efficient and low-power inverse class-F voltage doubler (VD) designed for radio frequency (RF) energy harvesting systems. Specifically tailored for mid-band 5G technology, the VD is designed for operation within the 1240–1300 MHz satellite band. The innovative design employs an inverse class-F architecture, incorporating a $\lambda/8$ short-ended transmission line (TL) connected to the diode anode and a ($\lambda/12$) open-ended transmission line linked to the input of the voltage doubler. This configuration aims to reshape voltage and current waveforms, effectively reducing losses and series resistance in the diode. Dual-coupled transmission lines (CTLs) are utilized to provide passive voltage boosting at low-input power levels. The suggested voltage doubler is implemented using RO4003C substrate material with a dielectric relative permittivity ($\varepsilon_r$) of 3.38 and a thickness of 0.81 mm. Measured results demonstrate a minimum input return loss of − 29.3 dB at 1.25 GHz, operating seamlessly within a frequency band from 1.18 to 1.32 GHz. The measured conversion efficiency is 45.2% at an input power ($P_{\text{in}}$) of − 4dBm. Furthermore, the peak RF–DC efficiency reaches 50% at an input power of 0dBm. Simulated results predict a remarkable conversion efficiency of 60% and 68.7% at − 4dBm and 0 dBm, respectively. In addition to its exceptional performance, the suggested voltage doubler exhibits an experimental DC output voltage of 0.53 V at $P_{\text{in}} = -10$dBm and a saturated DC voltage of 3.4 V at an input power of 10dBm under a load terminal resistance of 8 KΩ. Finally, the dimensions of the proposed voltage doubler are $25.3 \times 10.5\text{mm}^2$.

**Keywords** Ambient power · Class-$F^{-1}$ · Energy harvesting (EH) · Harmonic termination · Voltage doubler (VD) · Wireless power transfer (WPT)

✉ Marwa Mansour
marwa_mansour@eri.sci.eg

[1] Microelectronics Department, Electronics Research Institute (ERI), Cairo 11843, Egypt

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## 1 Introduction

Wireless power transfer (WPT) and radio frequency energy harvesting (RF-EH) have emerged as prominent focuses in microwave research. WPT is commonly utilized for long-distance and high-power transmission, while RF-EH concentrates on capturing low-power energy from diverse sources like Wi-Fi, GSM 900, and GSM 1800. The potential of RF-EH lies in its ability to power the Internet of Things (IoT), wireless sensor networks (WSNs), and medically implanted devices by converting otherwise wasted RF energy into usable DC output power. These energy harvesting circuits find applications in devices relying on limited power sources, such as batteries [2]. While the research on high-efficiency RF rectifiers has been extensive, there has been limited exploration of low-power rectifiers [6–8], 21.

Due to the complicated design of matching networks for larger bandwidths, only a limited number of broad-band rectifiers with high conversion efficiency have been reported [9]–11. On the other hand, multiband rectifiers are essential for sustaining device operation in the absence of energy sources [4, 10], 13. The nonlinear nature of diodes leads to variations in input impedance concerning frequency, DC load, and input power. To mitigate the variation in load impedance and rectifier nonlinearity, researchers have investigated resistance compression networks (RCNs), as discussed in [1]. Furthermore, multistage transmission line matching networks [19] and ladder LC networks [3] demonstrated effective matching over a wide range of frequencies.

In reference [13], a dual-band voltage doubler operating at frequencies of 0.85 and 1.4 GHz was developed utilizing double resonance circuits and a high Q-factor sine-shaped microstrip coil. This innovative design demonstrated an impressive maximum RF-to-DC efficiency of 50% at 0 dBm. Another noteworthy advancement is a wideband rectifier detailed in [14], showcasing an outstanding efficiency of 70% and yielding a DC voltage of 3.4 V at an input power of $P_{\text{in}} = 3\text{dBm}$. The investigation of wideband RF rectifiers has been a central focus of extensive research, with notable studies, such as those cited in [11], 12. For instance, the radio rectifier discussed in [11] employs microstrip transmission lines and ($\lambda/4$) short-circuit stubs designed for high-power systems, achieving peak RF-to-DC efficiency at a high-input power value ($P_{\text{in}} = 15\text{dBm}$). In [12], a wideband rectifier utilized dual L-sections for high-power applications. At an input power of $P_{\text{in}} = 0\text{dBm}$, it obtained a maximum RF-to-DC efficiency of 30%, and the paper did not provide information on the DC output voltage.

Additionally, a balanced RF rectifier utilizing inverse class-F over a large PCB area of 35 mm $\times$ 36 mm achieved an exceptional efficiency of 74.9% at a high-input power of 19 dBm, making it unsuitable for low-power systems [17]. In [15], a class-F RF voltage doubler (VD) was presented, achieving an efficiency of 60.5% at an input power of 2 dBm using discrete lumped elements. However, a class-F with discrete lumped components is considered a high-level circuit due to its complicated network. Another approach in [23] designed a 2.38 GHz RF microwave rectifier based on a microstrip coupled transmission line, with a maximum efficiency of 62% at an input power of 0 dBm but with a relatively large board size of 35 mm $\times$ 35 mm. Dual-coupled transmission lines in [22] were employed as a passive voltage boost, achieving a maximum RF-to-DC efficiency of 75.3% at an input power of 5.5 dBm and an efficiency of 58.5% at $P_{\text{in}} = -5\text{dBm}$, albeit with a large printed circuit board

dimension of 35 mm × 34 mm. In [24], a circuit configuration implementing an inverse class-F rectifier was realized under certain conditions, featuring a large PCB area of 30 mm × 19 mm.

This paper introduces a novel approach a low-power and compact-size voltage doubler designed for energy harvesting applications. The proposed design employs an inverse class-F topology with dual microstrip coupled transmission lines (CTLs). This configuration minimizes diode losses by strategically manipulating current and voltage waveforms. The inverse class-F configuration employs a ($\lambda/8$) short-ended transmission line (TL) and a ($\lambda/12$) open-ended TL to minimize diode losses by reducing the overlap between current and voltage waveforms. In this configuration, the ($\lambda/8$) short-ended TL and ($\lambda/12$) open-ended TL actively shape the voltage and current waveforms, yielding a distinctive square wave for the current and a characteristic half-sinusoidal wave for the voltage. The achievement of inverse class-F operation relies on maintaining an out-of-phase relationship between the current and voltage, leading to a deliberate phase difference that significantly mitigates overlap. This intentional phase difference serves to reduce losses and enhance overall efficiency. To compact the printed circuit board (PCB) size, the ($\lambda/12$) transmission line is intelligently divided into two parts, and the layout of the ($\lambda/8$) short-ended TL takes the form of a U-shape. The design introduces a voltage boost at low-power levels through the incorporation of dual-coupled transmission lines (CTLs). The integration of the inverse class-F configuration with dual CTLs enables the voltage doubler to perform optimally, particularly in cases involving lower energy signals.

The voltage doubler achieves impressive measured and simulated conversion efficiencies of 50% and 68.7%, respectively, at 0 dBm. The design attains a measured RF–DC efficiency of 45.2% with a DC voltage of 1.24 V at $P_{\text{in}} = -4\text{dBm}$. Furthermore, it maintains a constant measured DC voltage of 3.4 V at an input power of 10 dBm. The efficiency bandwidth spans 140 MHz, and the printed circuit board (PCB) size is compact at $0.19\lambda_g \times 0.08\lambda_g\text{mm}^2$.

The structure of the paper is organized as follows: Sect. 2 delves into the fundamentals of RF-to-DC rectifiers and introduces the basic concepts of inverse class-F. Section 3 provides an in-depth discussion on the design, analysis, fabrication, and experimental results of the proposed inverse class-F voltage doubler. Finally, Sect. 4 summarizes the work.

## 2 Fundamentals of RF-to-DC Rectifier

Diode-based voltage doubler circuits are more commonly used than CMOS circuits due to their low turn-on voltage [5]. Schottky barrier diodes with a low forward voltage drop are widely employed in RF energy harvesting applications, enhancing the conversion efficiency ($\eta_{\text{RF-DC}}$) at low-input power levels.

The conversion efficiency of the rectifier is primarily influenced by diode losses, impedance mismatch losses, printed circuit board (PCB) conductor losses, substrate losses, and radiation losses. Diode parameters such as series resistance ($R_S$), junction capacitance ($C_J$), built-in potential ($V_{\text{bi}}$), breakdown voltage ($V_{\text{br}}$), and higher-order

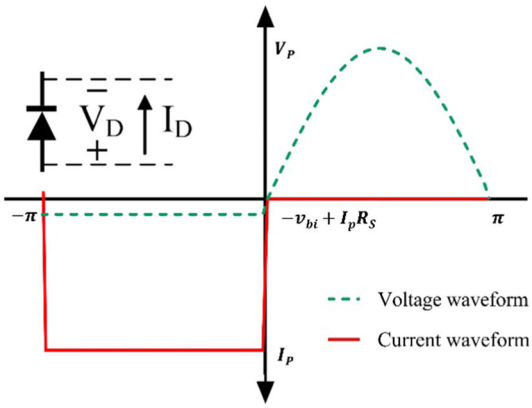



**Fig. 1** Current and voltage waveforms of the ideal inverse class-F architecture (where $V_p$ and $I_p$ are the peak voltage and current values, respectively, while $v_{\text{bi}}$ and $R_s$ are the built-in potential and the series resistance of the diode, respectively)

harmonics generated by the diode contribute to diode losses. The loss in the low-input power region is attributed to the forward diode built-in potential ($V_{\text{bi}}$).

The loss in the high-input power region is attributed to the diode breakdown voltage ($V_{\text{br}}$), arising from the leakage current after the output voltage exceeds the breakdown voltage of the diode [16]. Losses resulting from power dissipation in the diode depend on the integral of the voltage waveform multiplied by the current waveform [6]. Reducing the integral outcome can be achieved by eliminating the overlap between the two waveforms, utilizing techniques such as class-F and inverse class-F.

The inverse class-F circuit is a harmonic elimination circuit consisting of ($\lambda/8$) short-ended and ($\lambda/12$) open-ended transmission lines (TLs). The inverse class-F configuration is employed to create a high impedance at even harmonics and a low impedance at odd harmonics.

As a result, the voltage waveform is shaped to be a half-sinusoidal wave, while the current is formed as a square wave across the rectifying device, as illustrated in Fig. 1, according to Fourier series analysis [18]. This design reduces the overlap between the voltage and current waveforms, consequently minimizing power losses from the diode and enhancing efficiency.

## 3 Proposed Inverse Class-F Voltage Doubler

### 3.1 Design and Analysis

The schematic diagram of the suggested voltage doubler (VD), shown in Fig. 2, consists of a DC block capacitor ($C_b$), dual-coupled transmission lines (CTLs), an HSMS2852 zero-bias Schottky diode, a harmonic elimination circuit including a $\lambda/8$ short-ended transmission line (TL), a $\lambda/12$ open-ended TL, a DC filter ($L_1$ and $C_1$), and load resistance ($R_L$).

The ($\lambda/8$) short-ended transmission line compensates for the capacitive input impedance of diode $D_1$ by introducing an inductive reactance ($jZ_{01}$) at the operating frequency ($f_0$). Additionally, it functions as an open circuit at the second harmonic,

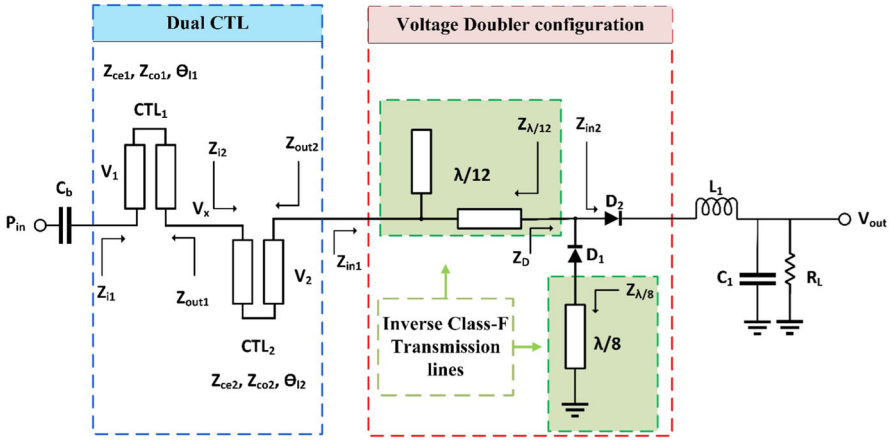



**Fig. 2** Schematic circuit of the suggested voltage doubler

thereby canceling the second current harmonic, as expressed in Eq. (1) [24].

$$Z_{\lambda/8} = +jZ_{01}\ \tan\left(\frac{\pi}{4}\frac{f}{f_0}\right) = \begin{cases} 0, & f = 0 \\ jZ_{01}, & f = f_0 \\ \infty, & f = 2f_0 \\ -jZ_{01}, & f = 3f_0 \end{cases} \tag{1}$$

where $Z_{01}$ is the characteristic impedance for the ($\lambda/8$) transmission line, and $f_0$ is the fundamental frequency at which the rectifier operates. The inductor $L_1$ eliminates the imaginary part of diode $D_2$ and the output DC filter by setting the imaginary part, as specified in Eq. (2), equal to zero.

$$Z_{\text{in}\,2} = Z_{D\,2} + j\omega L_1 + \left(R_L \| \frac{1}{j\omega C_1}\right) \tag{2}$$

where $Z_{D2}$ represents the input impedance of diode ($D_2$). The ($\lambda/12$) open-ended transmission line is divided into two parts to compact the PCB size. It functions as a short circuit at the third harmonic, canceling the third voltage harmonic. Moreover, it acts as a parallel open stub, matching the input impedance of the diodes ($Z_D$) to the output impedance of the dual-coupled transmission lines (CTLs), denoted as ($Z_{\text{out2}}$), as expressed in Eq. (3) [24].

$$Z_{\lambda/12} = -jZ_{02}\cot\left(\frac{\pi}{6}\frac{f}{f_0}\right) = \begin{cases} \infty, & f = 0 \\ -1.73j\ Z_{02}, & f = f_0 \\ -0.58j\ Z_{02}, & f = 2f_0 \\ 0, & f = 3f_0 \end{cases} \tag{3}$$

where $Z_{02}$ is the characteristic impedance of the ($\lambda/12$) transmission line. The dual-coupled transmission lines (CTLs) are utilized to provide passive voltage gain at

low-input power and to match the voltage doubler circuit to 50 Ω [22]. The voltage boost offered by the CTLs generates a sufficient input voltage higher than the forward built-in potential of the diode $V_{\mathrm{bi}}$, enabling the diodes to operate at lower input power levels than conventional configurations. The ABCD matrix for symmetric dual-coupled transmission lines can be expressed as follows [20].

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix}$$

where

$$\begin{aligned} A_x &= D_x = \frac{Z_{\mathrm{ce}_x} - Z_{\mathrm{co}_x} \tan^2 \theta_{l_X}}{Z_{\mathrm{ce}_x} + Z_{\mathrm{co}_x} \tan^2 \theta_{l_X}} \\ B_x &= \frac{2jZ_{\mathrm{ce}_x} Z_{\mathrm{co}X} \tan\theta_{l_X}}{Z_{\mathrm{ce}_x} + Z_{\mathrm{co}_x} \tan^2 \theta_{l_x}} \\ C_x &= \frac{2j \tan\theta_{l_x}}{Z_{\mathrm{ce}_x} + Z_{\mathrm{co}_x} \tan^2 \theta_{l_X}} \end{aligned} \tag{4}$$

where $\theta_{l_x}$ represents the electrical length of the xth CTL, while $Z_{\mathrm{ce}\,x}$ and $Z_{\mathrm{co}\,x}$ are the even-mode and odd-mode characteristic impedances of the xth CTL, respectively. The total passive boosting gain ($G_t$) obtained by the dual CTLs can be derived as follows:

$$\begin{aligned} \mathrm{G}_1 &= \frac{\mathrm{V}_x}{\mathrm{V}_1} = \frac{1}{\mathrm{A}_1 + \frac{\mathrm{B}_1}{\mathrm{Z}_{\mathrm{out}\,1}}} \\ \mathrm{G}_2 &= \frac{\mathrm{V}_2}{\mathrm{V}_x} = \frac{1}{\mathrm{A}_2 + \frac{\mathrm{B}_2}{\mathrm{Z}_{\mathrm{out}\,2}}} \\ \mathrm{G}_t &= \frac{\mathrm{V}_2}{\mathrm{V}_1} = \mathrm{G}_1\mathrm{G}_2 = \left(\frac{1}{\mathrm{A}_1 + \frac{\mathrm{B}_1}{\mathrm{Z}_{\mathrm{out}\,1}}}\right)\left(\frac{1}{\mathrm{A}_2 + \frac{\mathrm{B}_2}{\mathrm{Z}_{\mathrm{out}\,2}}}\right) \end{aligned} \tag{5}$$

where $\mathrm{V}_1$ and $\mathrm{V}_2$ represent the input and output voltages of the dual-coupled transmission lines, respectively. $\mathrm{V}_x$ is the voltage between the two coupled lines, and $\mathrm{Z}_{\mathrm{out}\,x}$ is the output impedance of the xth CTL. Additionally, the relationship between the input impedance ($Z_i$) and the output impedance($Z_{\mathrm{out}}$) of each CTL can be expressed as follows:

$$Z_i = \frac{A \times \mathrm{Z}_{\mathrm{out}} + B}{C \times \mathrm{Z}_{\mathrm{out}} + D} \tag{6}$$

To determine the values of the six parameters ($\mathrm{Z}_{\mathrm{ce}\,1}$, $\mathrm{Z}_{\mathrm{co}\,1}$, $\mathrm{Z}_{\mathrm{ce}\,2}$, $\mathrm{Z}_{\mathrm{co}\,2}$, $\theta_{\mathrm{l}\,1}$, and $\theta_{\mathrm{l}\,2}$) that define the characteristics of the two CTLs, the following conditions should be satisfied:

(i) The input impedance of the first CTL ($Z_{\mathrm{i}1}$) should be matched to the port's input impedance, which is 50 Ω.

$$\mathrm{Z}_{\mathrm{i}1} = 50\Omega \tag{7}$$

(ii) The output impedance of the second CTL ($Z_{out2}$) should match the input impedance of the voltage doubler ($Z_{in1}$), as shown in Eq. (8).

$$Z_{out2} = Z_{in1} \tag{8}$$

The relationship between ($Z_{i1}$) and ($Z_{out2}$) of the dual CTLs can be expressed as follows:

$$\begin{aligned} V_1 &= (A_1A_2 + B_1C_2)V_2 + (A_1B_2 + B_1D_2)I_2 \\ I_1 &= (C_1A_2 + D_1C_2)V_2 + (C_1B_2 + D_1D_2)I_2 \\ Z_{i1} &= \frac{V_1}{I_1} = \frac{(A_1A_2+B_1C_2)\times Z_{out2}+(A_1B_2+B_1D_2)}{(C_1A_2+D_1C_2)\times Z_{out2}+(C_1B_2+D_1D_2)} \end{aligned} \tag{9}$$

(iii) The total gain ($G_t$) of the dual CTLs should be greater than one, as derived from Eq. (4), as follows:

$$\begin{aligned} V_1 &= (A_1A_2 + B_1C_2)V_2 + (A_1B_2 + B_1D_2)\frac{V_2}{Z_{out2}} \\ G_t &= \frac{V_2}{V_1} = \frac{Z_{out2}}{(A_1A_2+B_1C_2)\times Z_{out2}+(A_1B_2+B_1D_2)} > 1 \end{aligned} \tag{10}$$

(iv) The gain of each CTL must exceed one.

$$\begin{aligned} \left(\frac{1}{A_1+\frac{B_1}{Z_{out\,1}}}\right) &> 1 \\ \left(\frac{1}{A_2+\frac{B_2}{Z_{out\,2}}}\right) &> 1 \end{aligned} \tag{11}$$

where the output impedance of the first CTL can be related to its input impedance using Eq. (6) as follows:

$$Z_{out1} = -\frac{50D_1-B_1}{50C_1-A_1} \tag{12}$$

The use of dual CTLs adds a significant degree of freedom to the system. With many parameters and few equations, there are infinitely many solutions to obtain the parameters ($Z_{ce\,1}, Z_{co1}, Z_{ce\,2}, Z_{co\,2}, \theta_{l\,1}$, and$\theta_{l\,2}$) of dual CTLs. The constraints on selecting one of the solutions include values that yield the highest efficiency at low-input power, low conductor and radiation loss, and a compact size. The system equations from (4) to (12) are optimized using advanced design system (ADS).

### 3.2 Fabrication of RF Voltage Doubler

The layout for the suggested inverse class-F VD, depicted in Fig. 3(a), is implemented using RO4003C substrate material with a thickness of 0.81 mm and a dielectric relative permittivity ($\varepsilon_r$) of 3.38. The dimensions are 25.3 mm × 10.5 mm. The manufacturing

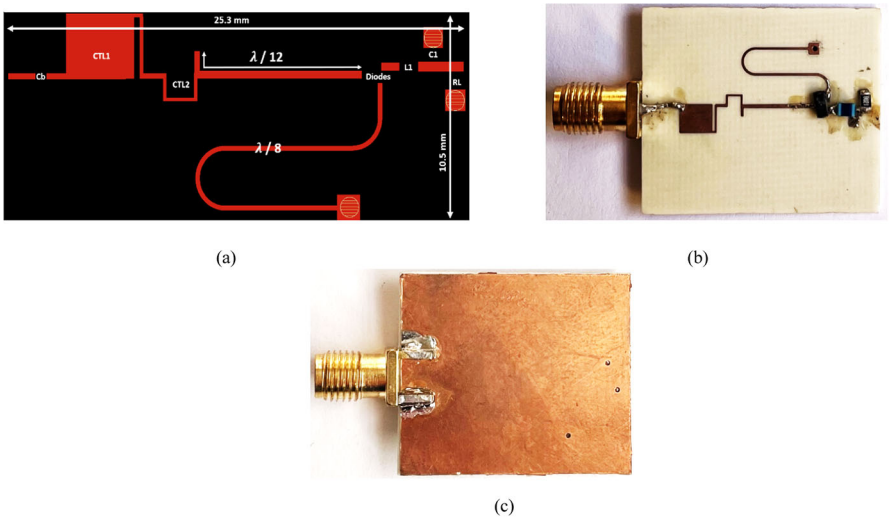



**Fig. 3** Proposed inverse class-F VD: **a** layout, **b** top view, and **c** bottom view of prototype

process employs photolithography with a mask resolution of approximately 4064 dpi (dots per inch). In the manufactured design, the minimum track width is 0.15 mm, and the minimum space between two tracks is also set to 0.15 mm. The design underwent simulation using the Advanced Design System program (ADS) and electromagnetic (EM) simulation for layout and physical verifications. Measurement tools include a signal generator with part number MG3697C, a vector network analyzer (VNA) identified as Rohde & Schwarz ZNA67, and a digital multimeter. Figure 3(b) and (c) displays the top and bottom views of the manufactured prototype photography. The bottom layer of the manufactured PCB serves as the ground layer, comprising a solid layer without any etching or DGS, as illustrated in Fig. 3(c).

For the Schottky diode, the model number HSMS2852 is selected, which has a low forward built-in potential voltage ($V_{\text{bi}}$) of 0.25 V, making it suitable for low-input power energy harvesting systems. However, it comes with a large series resistance ($R_s$) of 25 Ω. The issue of the series resistance is addressed by introducing the inverse class-F harmonic termination network, preventing the overlap of current and voltage across the diode with the series resistance. The values of discrete components used in the proposed design are given in Table 1, which includes the quality factor (Q), self-resonance frequency (SRF), and the manufacturer part number corresponding to each component.

The inductor $\text{L}_1$ is carefully selected to eliminate the imaginary part of Eq. (2) at the operating frequency ($f_0$), assuming a large value for the smoothing capacitor ($\text{C}_1$). The smoothing capacitor ($\text{C}_1$) serves the purpose of providing a smooth and ripple-free DC voltage at the circuit's output. While, the blocking capacitor ($C_b$) is employed to block the DC voltage generated by the rectifier. Its value is chosen to be sufficiently large to avoid affecting the input impedance. To ensure the inverse class-F operation, the voltage waveform is designed as a half-sinusoidal wave, while the current waveform

**Table 1** Utilized components specification in the suggested voltage doubler

| Element | Value | Manufacturer model number | Quality factor | Tolerance (%) | SRF (GHz) |
|---|---|---|---|---|---|
| Cb and C1 | 0.082 uF | GRM155R71C823KA88D | – | ± 10 | – |
| L1 | 27 nH | LQW2BAN27NJ00 | 85@500 MHz | ± 5 | 2.75 |
| RL | 8 kΩ | RC0805FR-078K06L | – | ± 1 | – |

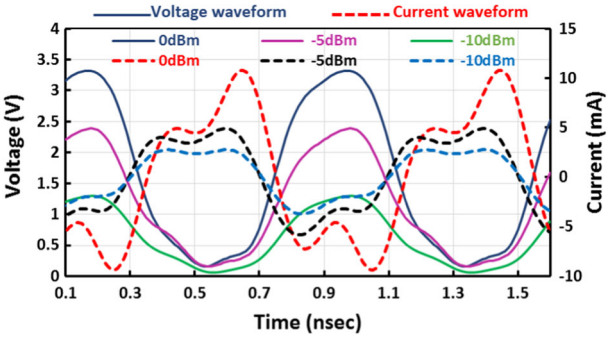



**Fig. 4** Current and voltage waveforms of the suggested inverse class-F VD at various input power levels

adopts a square wave. Figure 4 provides a graphical representation of the voltage and current waveforms for the proposed inverse class-F voltage doubler, showcasing different input power levels (0 dBm, − 5 dBm, and − 10 dBm). In this illustration, the solid curves represent voltage waveforms, and the dashed curves elucidate current waveforms. The distinctive 180-degree phase shift between the current and voltage is evident, effectively minimizing their overlap and enhancing overall efficiency. Moving forward, Fig. 5 details the impedance contour of the proposed class-$F^{-1}$ VD at an input power of -10 dBm. The configuration distinctly displays an open circuit at the second harmonic frequency of 2.47 GHz and a short circuit at the third harmonic frequency of 3.66 GHz.

The selection of the resistive load ($R_L$) is crucial, as it influences the DC voltage, the RF-to-DC efficiency (η), and the input power at which the peak efficiency (η) occurs. The output voltage is directly proportional to the load resistance, expressed as $V_{\text{out}} = I_{\text{out}} \times R_L$, and the rectifier's conversion efficiency (η) decreases as the load $R_L$ increases, following the formula $\eta = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{V_{\text{out}}^2}{P_{\text{in}} \times R_L}$. The peak efficiency occurs at an input power of $P_{\text{in}} = \frac{V_{\text{br}}^2}{4R_L}$, where $V_{\text{br}}$ is the breakdown voltage of the diode [16]. Thus, increasing the value of $R_L$ shifts the maximum efficiency to lower input power levels. The impact of the load resistance ($R_L$) on the output DC voltage and efficiency is examined to determine the optimal value. Criteria for selecting $R_L$ include finding the value that yields the highest output voltage and efficiency at low-input power levels. The optimal resistance value, $R_L$, is determined through a careful trade-off

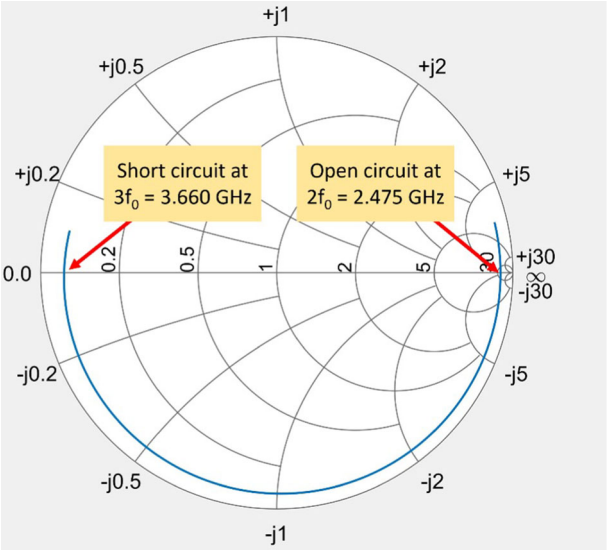



**Fig. 5** Impedance contour for the suggested inverse class-F VD at an input power of − 10 dBm

between DC voltage ($V_{\mathrm{DC}}$) and RF–DC efficiency. The output voltage experiences an increase with the load resistance until it saturates at a high $P_{\mathrm{in}}$. The behavior of efficiency in terms of $R_L$ is complex, rising with the load resistor until it reaches a peak and then decreasing again as the load resistor increases. The influence of the load resistor ($R_L$) on efficiency (η) is illustrated in Fig. 6. As observed, efficiency exhibits an inverse relationship with the value of $\mathrm{R_L}$ and can be determined using the formula $\eta = \frac{V\mathrm{out}^2}{R_L \times P_{\mathrm{in}}}$. Consequently, the selected $\mathrm{R_L} = 8\ \mathrm{k\Omega}$ results in the highest efficiency at an input power of − 10 dBm, whereas a 4 kΩ load resistor achieves a peak efficiency of 70% but shifts the peak efficiency to $P_{\mathrm{in}} = 3.5\mathrm{dBm}$. The variation of DC output voltage with different load values is presented in Fig. 7. As cleared, any increase in

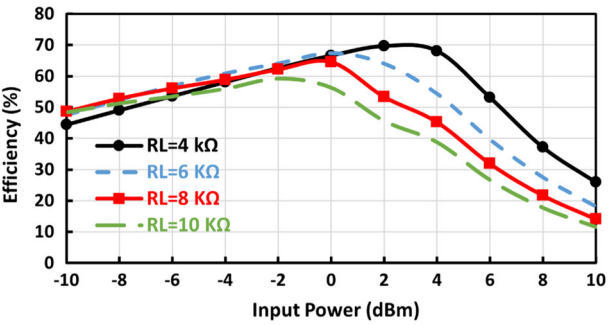



**Fig. 6** Simulated efficiency versus input power at different load resistance values, operating at 1.25 GHz

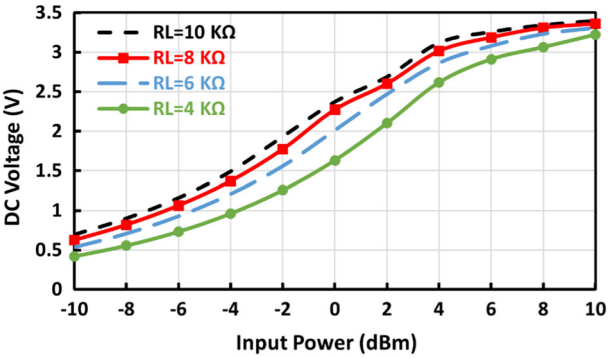



**Fig. 7** Simulated DC output voltage against input power at various $R_L$ values for the proposed inverse class-F voltage doubler at a frequency of 1.25 GHz

the load resistor leads to a corresponding rise in the output DC voltage, as expressed by $V_{\text{out}} = I_{\text{out}} \times R_L$.

### 3.3 Simulated and Measured Results

Figure 8 displays the simulated and measured DC output voltage against RF input power at a frequency of 1.25 GHz and a load of 8 kΩ. At an input power of -10 dBm, the measured DC output voltage equals 0.53 V and a saturated DC voltage of 3.4 V at $P_{\text{in}} = 10$dBm. Additionally, the DC voltage is directly proportional to the RF input power, efficiency, and load resistance ($R_L$), as indicated by the efficiency equation ($\eta = \frac{V\text{out}^2}{R_L \times P_{\text{in}}}$), and the DC voltage saturates when the efficiency reaches its peak value.

The RF–DC conversion efficiency against input power for the suggested inverse class-F voltage doubler is shown in Fig. 9 at $f_0 = 1.25$ GHz with a load resistance

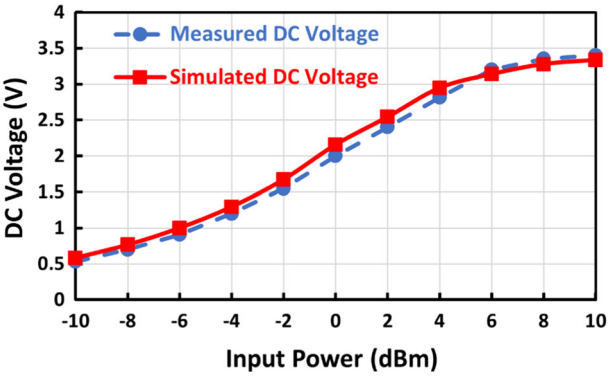



**Fig. 8** Measured and simulated DC voltage versus input power of the suggested radio frequency VD ($f_0 = 1.25$ GHz and $R_L = 8$ kΩ)

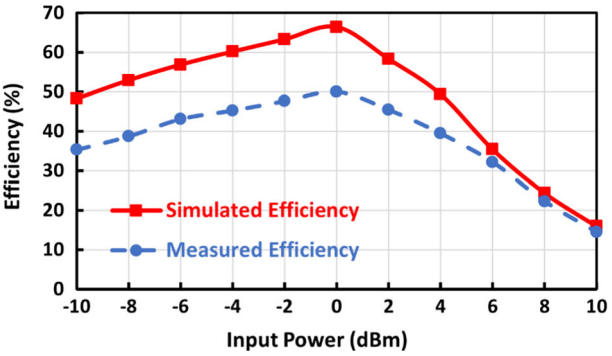



**Fig. 9** Measured and simulated efficiency versus input power of the suggested radio frequency VD at an operating frequency of 1.25 GHz and a load resistor of 8 kΩ

of 8 kΩ. As observed, the suggested voltage doubler achieves an extremely measured efficiency of 50% at $P_{\text{in}} = 0\text{dBm}$ and a conversion efficiency of 45.2% at $P_{\text{in}} = -4\text{dBm}$. Furthermore, an efficiency of 35.3% at $P_{\text{in}} = -10\text{dBm}$ is achieved due to the use of dual CTLs, which increase the input voltage and reduce the built-in potential loss of the diode at low-input power. Figure 10 illustrates the simulated RF-to-DC efficiency versus the frequency for the suggested RF voltage doubler. Notably, a frequency bandwidth of 1 GHz to 1.52 GHz is achieved with an efficiency exceeding 40% at $P_{\text{in}} = -4\text{dBm}$. It is important to highlight that increasing the input power leads to higher RF–DC conversion efficiency, as the input impedance varies at different power levels, impacting the matching. Additionally, low-input power levels contribute to increased diode losses due to the required turn-on voltage of the diode. On the other hand, Fig. 11 depicts the measured and simulated efficiency ($\eta$) against frequency at $P_{\text{in}} = -4\text{dBm}$. The inverse class-F voltage doubler achieves a measured efficiency ($\eta$) of 45.2% at a frequency of 1.25 GHz. The difference between the measured and simulated results comes from the tolerance in discrete components, soldering effects, the influence of SMA connectors, PCB losses, parasitic impacts, and manufacturing

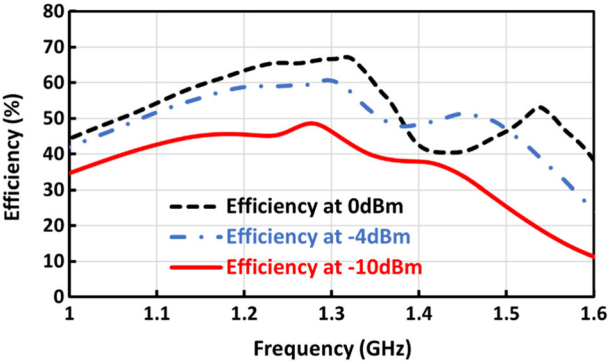



**Fig. 10** Simulated efficiency versus frequency at different input power levels for the suggested RF VD tested with $R_L = 8$ kΩ

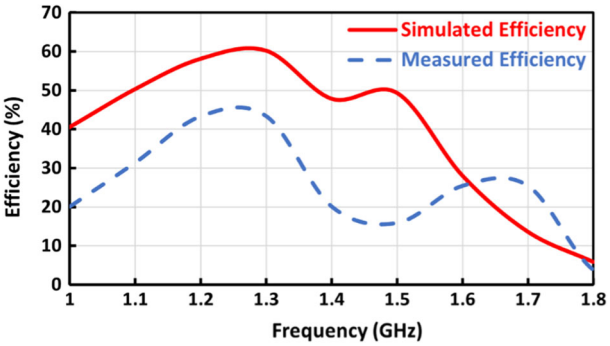



**Fig. 11** Simulated and measured efficiency versus the frequency for the proposed RF voltage doubler at $P_{\text{in}} = -4\,\text{dBm}$ and $R_L = 8\ \text{k}\Omega$

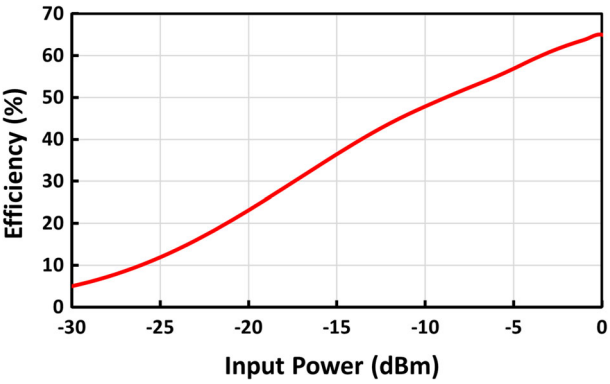



**Fig. 12** Simulated efficiency versus input power at an operating frequency of 1.25 GHz and dc load of 8 kΩ

errors. Figure 12 illustrates RF–DC conversion efficiency at $f_0 = 1.25$ GHz for a lower input power range from − 30 to 0 dBm at $R_L = 8\ \text{k}\Omega$. The suggested voltage doubler achieves 25% efficiency at an input power of − 20 dBm and 37% at − 15 dBm.

Figure 13 shows large signal input return loss ($|S_{11}|$) at different input power levels. A satisfactory match with $|S_{11}|$ below -10 dB is observed across the frequency band from 1200 to 1340 MHz. The diode's nonlinear nature causes its input impedance to vary with input power, requiring the matching circuit to be configured at a specific power level, in this case, − 10 dBm.

Figure 14(a) shows the measured input reflection coefficient $|S_{11}|$ for the suggested inverse class-F VD, achieving an input return loss of − 29 dB at 1.25 GHz with a 100 MHz impedance bandwidth. While Fig. 14(b) displays a photograph of the voltage doubler's measurement system. Figure 14(c) illustrates the measured input reflection coefficient $|S_{11}|$ at various input power levels of − 5 dBm, 0 dBm, 5 dBm, and 10 dBm. At an input power of 10 dBm, the proposed design exhibits a dual-band match at (1.1–1.35 GHz) and (1.5–1.72 GHz). However, at an input power of 5 dBm, the operating bandwidth narrows to (1.18–1.34 GHz) and (1.57–1.7 GHz), and so forth.

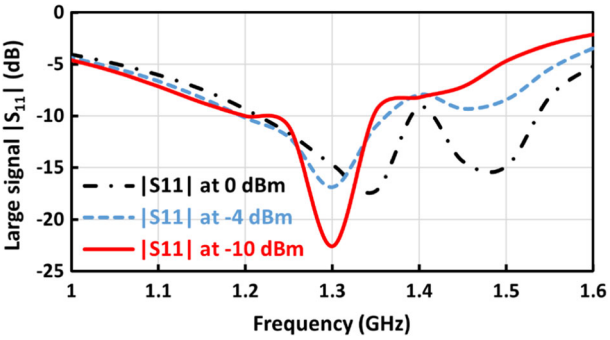


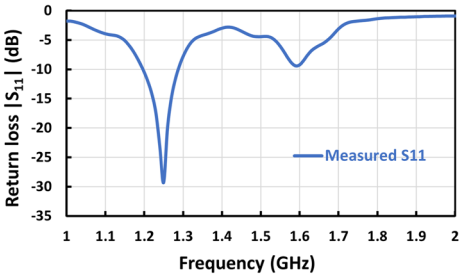

**Fig. 13** Simulated $|S_{11}|$ at different RF input power levels for the proposed VD with $R_L = 8$ kΩ

The proposed inverse class-F design utilizes coupled transmission lines (CTLs) to boost the input voltage and enhance the conversion efficiency at low-power levels. Moreover, the CTLs affect the input reflection coefficient. The impact of CTLs on RF–DC conversion efficiency is illustrated in Fig. 15. Evidently, employing dual CTLs increases RF–DC conversion efficiency by over 5% at -10 dBm.

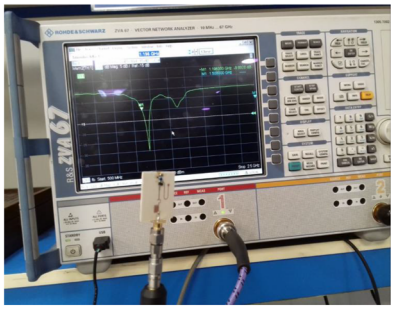
The impact of coupled transmission lines (CTLs) on the input return loss $|S_{11}|$ versus frequency at a load resistance of 8 kΩ is illustrated in Fig. 16. It is evident that the use of dual CTLs improves input impedance matching, reducing the return loss at 1.3 GHz by introducing inductive reactance to the proposed voltage doubler. In Fig. 17, the DC output voltage exhibits a slight change with the incorporation of dual CTLs. While the impact of dual CTLs on DC voltage is marginal compared to using a single CTL, their use increases RF-to-DC efficiency by approximately 1.5% at − 10 dBm input power, as opposed to a single CTL. Notably, the dual CTL configuration significantly influences the input reflection coefficient $|S_{11}|$, exhibiting an improvement of approximately − 3 dB compared to a single CTL, as shown in Fig. 16.

### 3.4 Comparison with the State of the Art

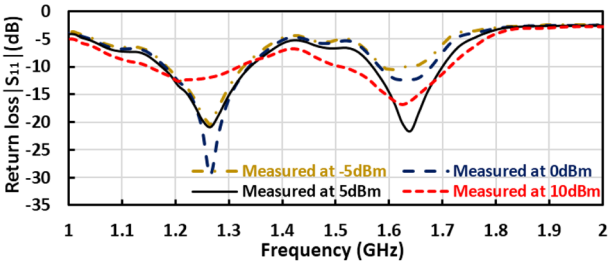
The suggested inverse class-F voltage doubler, which integrates dual microstrip coupled transmission lines, has been compared with recently reported RF rectifiers. The comparison encompasses working frequency, diode model, substrate material, conversion efficiency, load resistance, DC voltage, input reflection coefficient $|S_{11}|$, and fabricated board size, as detailed in Table 2. The inverse class-F voltage doubler displays outstanding input matching, achieving − 29 dB, surpassing values in [11, 13, 14], and [24]. The proposed class-$F^{-1}$ voltage doubler demonstrates an impressive conversion efficiency of approximately 35% at a low-input power of − 10 dBm, in contrast to the 58.5% reported at a higher input power of − 5 dBm in [22]. It is noteworthy that peak efficiency is attained at low-input power levels. Furthermore, the design accomplishes a high DC voltage of 0.53 V with a low-input power of − 10 dBm,




(a)



(b)




(c)

**Fig. 14** **a** Measured input reflection coefficient $|S_{11}|$ for the suggested inverse class-F voltage doubler (VD), **b** photograph of the measurement system (VNA part number: Rohde & Schwarz ZNA67), and **c** measured input reflection coefficient $|S_{11}|$ at several input power levels of − 5 dBm, 0 dBm, 5 dBm, and 10 dBm

surpassing the performance of references [14], 24. Finally, the design boasts a compact PCB area of $(0.19\lambda_g \times 0.08\lambda_g)$, distinguishing it from state-of-the-art published works.

## 4 Conclusion

A low-power inverse class-F voltage doubler for energy harvesting (EH) systems has been comprehensively analyzed, designed, fabricated, and measured. The suggested voltage doubler (VD) configuration operates at a frequency of 1.25 GHz, aligning

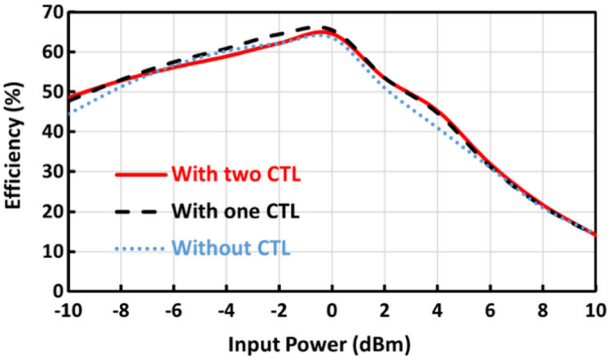



**Fig. 15** Effect of the coupled transmission lines on the simulated efficiency for the proposed design ( $f_0 = 1.25$ GHz and $R_L = 8$ kΩ)

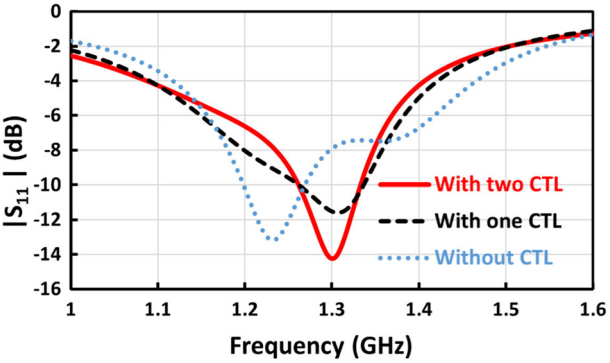



**Fig. 16** Influence of the coupled transmission lines on the simulated input reflection coefficient $|S_{11}|$ for the suggested voltage doubler (VD) design (small-signal $|S_{11}|$ and a load resistance of 8 kΩ)

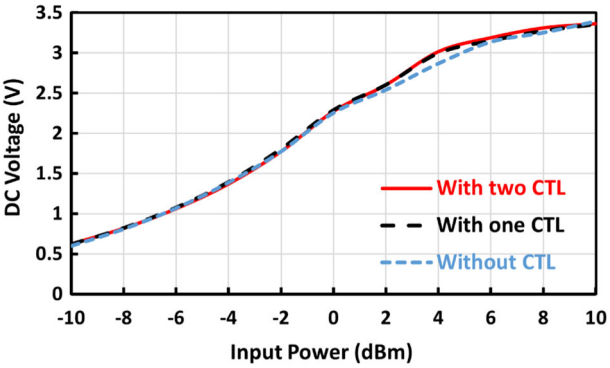



**Fig. 17** Impact of the coupled transmission lines on simulated DC voltage versus input power for the suggested inverse class-F voltage doubler (VD) ($f_0 = 1.25$GHz and$R_L = 8$kΩ)

**Table 2** Performance comparison of the proposed RF voltage doubler with other microwave rectifiers utilizing microstrip substrate

| Index | This work | 2023 [13] | 2023 [14] | 2020 [11] | 2018 [12] | 2022 [15] | 2020 [23] | 2021 [22] | 2017 [17] | 2019 [24] |
|---|---|---|---|---|---|---|---|---|---|---|
| Topology | Class-$F^{-1}$ and two CTLs | Dual-band | Wideband | Wideband | Wideband | Class-F | CTL | Two CTLs | Class- $F^{-1}$ | Class- $F^{-1}$ |
| Frequency band (GHz) | 1.18–1.32* | 0.85, 1.4 | 0.72–1.05 | 1–2.4 | 0.87–2 | 0.9 | 2.38 | 2.39 | 2.34 | 2.35 |
| Diode model number | HSMS2852 | HSMS2852 | HSMS2852 | SMS7630-005LF | SMS7630-005LF | HSMS2852 | HSMS285C | HSMS2860 | HSMS2860 | HSMS2860 |
| Substrate | RO4003C | RO4003C | RO4003C | NA | FR-4 | RO4003C | RO4003C | RO4003C | RO4350 | F4BM220 |
| Efficiency (%) @ dBm | 35.3@-10<br>45.2@-4 | 50@0 | 70@3 | 50@4 | 40@0 | 60.5@2 | 62@0 | 58.5@-5 | 74.9@19 | 52@0 |
| Load resistance ($R_L$) | 8 KΩ | 2.7 KΩ | (2–10) KΩ | 1.6 KΩ | 22 KΩ | 10 KΩ | 2 KΩ | 1.76 KΩ | 330 Ω | NA |
| DC voltage (V) @ dBm | 0.53@-10 | 1.2@0 | 3.4@3 | 1 V@0 | NA | 1@-10 | NA | NA | NA | 0.5@1 |
| Input return loss \|S11\| (dB) | $< -29$ | $< -15.5$ | $< -10$ | $-10$ | $< -5$ | $< -12$ | NA | NA | $< -20$ | NA |
| PCB size ($\lambda_g$) | $0.19\lambda_g \times 0.08\lambda_g$ | NA | $0.13\lambda_g \times 0.03\lambda_g$ | NA | NA | $0.1\lambda_g \times 0.1\lambda_g$ | $0.5\lambda_g \times 0.5\lambda_g$ | $0.5\lambda_g \times 0.65\lambda_g$ | $0.5\lambda_g \times 0.5\lambda_g$ | $0.34\lambda_g \times 0.2\lambda_g$ |
| PCB area ($cm^2$) | 2.7 | 4.7 | 1.26 | 10 | 11.4 | 2.8 | 12.25 | 14.62 | 12.6 | 5.7 |
| Results | Measured | Measured | Measured | Measured | Measured | Measured | Measured | Measured | Measured | Measured |

*CTL* Coupled Transmission Line

*Bandwidth measured at efficiency > 40%.

with the mid-band frequency range of 5G technology. The compact size of 2.66 cm2 is achieved using RO4003C substrate material with a dielectric relative permittivity ($\varepsilon_r$) of 3.38 and a microstrip thickness of 0.81 mm. The inverse class-F configuration employs $\lambda/8$ short-ended and $\lambda/12$ open-ended transmission lines to minimize diode losses. Dual-coupled transmission lines are incorporated to enhance voltage at low-power levels. In prototype testing, the measured efficiency demonstrates an RF–DC conversion efficiency of 45.2% at $P_{\text{in}} = -4\text{dBm}$, rendering it highly suitable for energy harvesting applications. The design achieves a peak efficiency of 50% at 0 dBm with an operating frequency of 1.25 GHz. This results in a DC output voltage of 0.53 V at -10 dBm and a saturated DC voltage of 3.4 V at an input power of 10 dBm. The proposed inverse class-F voltage doubler has been intricately designed to cater specifically to the needs of battery-powered implantable and wearable medical devices. This versatile design lends itself to a range of applications across various fields, including implantable wearable electronics, physiological operation monitoring, neural recording, and medical imaging. Its adaptability makes it a valuable asset in the realm of advanced medical technology.

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**Data Availability** The data that support the findings of this study are available from the corresponding author, [Marwa Mansour], upon reasonable request.

## Declarations

**Conflict of Interest** The author declares that she has no conflict of interest.

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