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EDITORIAL

Guest Editorial: Low Power Architectures for Digital Video and Image Compression

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It's my great pleasure to introduce this Special Section on Low power architectures for digital video and image compression to the Circuits, Systems, and Signal Processing readership. It is dedicated to research problems and innovative solutions in all aspects of design and architecture realization issues of state-of-the-art algorithm and analysis for image and video compression techniques. Large bandwidth requirement is one of the key issues in video coding and event triggered transmission of visual information. Prominent examples of such applications include highly efficient video encoding and compression for digital television broadcasting, activity recognition for human behavior characterization and surveillance systems. Artificial intelligence-based compression and analytics algorithms have gained significant academic, research, and industrial interest as compared to traditional transform or entropy coding techniques. Although these compression techniques reduce the transmission bandwidth, but they exhibit high design complexity and memory requirements primarily due to the constraints of high frame rate and image resolution. Moreover, several applications, including portable and wireless image/video analytics and communications pose severe constraints on the power consumption. The power issue has become an imperative design criterion in the era of submicron/nano fabrication technology nodes.

This Special Section has been organized to bring together researchers and experts to address the technological challenges of designing innovative architectures for image/video compression and analytics optimized for low power consumption, small chip area, and high operating frequency. Eleven articles have been accepted after rigorous reviewing process that address one or more challenges with novel solutions that are organized as follows.

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1 Image/Video Compression Architectures

There are two articles under this category. In the first article, Raj et al. have proposed deep neural network-based compressor and decompressor architectures capable of encoding relevant information for bio-medical applications. These architectures have been implemented after rigorous design space exploration to achieve high compression rate and lower computational cost as compared to JPEG and J2K while maintaining superior quality factor.

In the second article, Turcza et al. present an image compressor architecture that exploits the correlation between color components from raw data of Bayer color filter array for resource constraint devices. ASIC implementation has resulted in significant improvements in power consumption and area as compared to other architectures in the literature.

2 Architectures for Image/Video Analytics

Under this category, in the first article, Kumar et al. have developed a deep neural network architecture for activity recognition application that integrates 2D-CNN architecture with temporal shift module to learn spatial and temporal spaces from compressed video input. Since only a small amount of the compressed video stream is used, power and speed on any system are considerably improved while ensuring accurate activity recognition.

In the second article, Tabassum et al. have implemented hardware architecture for Sobel edge detection on brain MRI images followed by thresholding operation to detect brain tumors. The designed IP core consumes very low power and memory.

The third article by Golzar et al. presents an accelerator-architecture of Dynamic Graph Convolutional Neural Network for classification of irregular 3D datasets. Various high-level synthesis techniques along with the custom data–layout are used to maximize the throughput and minimize the complexity of the kernels. Significant speedup has been reported in the FPGA-based architecture as compared to Double Data Rate-4 memory-based CPU design.

In the last article of this category, K. Kumar has optimized 2D FIR filter architecture for image processing applications by considering symmetric filter coefficients using the modified Park-McClellan transformation. Multipliers have been replaced by minimal adders and shifters in the architecture for reducing the power consumption, delay and area overhead.

3 Architectures for Optimizing Computational Operations

In the first article under this category, Purkayastha et al. have designed a complete heuristic-based placement algorithm for the physical design of FPGAs to reduce the length of interconnects. The proposed algorithm introduces a novel segregation table-based cell spreading approach for improving the effectiveness of global placement and

area congestion. The delayed packing of LUTs and FFs reduces the computational overload during legalization.

In the second article, Rosa et al. have developed a squarer unit with emphasis on optimizing the design to achieve energy-saving and scalability in executing the algorithms. The adder tree has been optimized by using efficient adder schemes, omitting identical partial products, and optimization at logical level of all encoders. This has resulted in more energy and area efficient squarer units as compared to Booth folding, Folding and Merging, and radix-4 Booth designs.

The third article presented by Radovic et al. explores the opportunity to approximate the frequency window function for implementing adaptive S-transform. To limit the number of intermediate results that must be saved after each iteration, a multiple-clock-cycle architecture has been proposed resulting in reduced hardware complexity and clock cycle time as compared to the alternative approaches.

In the fourth article, Fan et al. have presented an area-efficient split capacitive array architecture for high-resolution successive approximation register (SAR) analog-to-digital converters (ADCs). The proposed design fabricated in 180 nm CMOS technology has 1 MS/s sampling rate and 15.78 effective number of bits while consuming 32 mW and occupying an active area of 4200 μm by 2200 μm.

In the last article, Huang et al. have proposed fault prediction model by applying particle swarm optimization and support vector machine algorithm for relay protection equipment. The combined model establishes correlation between the variables more accurately and improves the fault prediction accuracy. The model not only provides strong technical support for the maintenance strategy of relay protection equipment but also improves the maintenance efficiency and reduces the failure rate of protection equipment.

Collectively, the above articles have addressed diverse range of challenges and presented innovative solutions for developing optimized algorithms and architectures for image/video compression and analytics. We sincerely thank all the authors for their significant contribution to this issue. We also thank all the reviewers and appreciate their efforts for timely reviews. We hope this special section on Low power architectures for digital video and image compression would offer readers deeper insights into the recent architectural advancements in image/video compression and analytics.

Dr. Brajesh Kumar Kaushik (SM'13) received Doctor of Philosophy (Ph.D.) in 2007 from Indian Institute of Technology, Roorkee, India. He joined Department of Electronics and Communication Engineering, Indian Institute of Technology, Roorkee, as Assistant Professor in December 2009; promoted to Associate Professor in April 2014; and since Aug 2020 he has been serving as full Professor. He has been a Visiting Professor at TU-Dortmund, Germany in 2017; McGill University, Canada in 2018 and Liaocheng University, China in 2018. He served as Visiting Lecturer of SPIE society to deliver lectures in the area of Spintronics and Optics at SPIE chapters located across the world. He regularly serves as General Chair, Technical Chair, and Keynote Speaker of reputed international and national conferences. He also served as Chairman and Vice Chairman of IEEE Roorkee sub-section. Dr. Kaushik is a Senior Member of IEEE and member of many expert committees constituted by government and non-government organizations. He is currently serving as Distinguished Lecturer (DL) of IEEE Electron Devices Society (EDS) to offer EDS Chapters with quality lectures in his research domain. He is Editor-in-Chief of Elsevier Journal, Memories-Materials, Devices, Circuits and Systems; an Editor of IEEE Transactions on Electron Devices; Associate Editor of IEEE Sensors Journal; Associate Editor of IET Circuits, Devices & Systems; Editor of Microelectronics Journal, Elsevier; and Editorial Board member of Circuit World, Emerald. He is among top 2% scientists in world as per Stanford University report of 2019 and 2021. He is currently serving as member of two technical committees namely, Spintronics (TC-5), and Quantum Computing, Neuromorphic Computing and Unconventional Computing (TC-16) of IEEE Nanotechnology Council. He is also Regional coordinator (R10) of IEEE Nanotechnology Council Chapters. He has 12 books to his credit published by reputed publishers such as CRC Press, Springer, Artech and Elsevier. One his books, titled "Nanoscale Devices: Physics, Modeling, and Their Application", CRC Press won 2018 Outstanding Book and Digital Product Awards in the Reference/Monograph Category from Taylor and Francis Group. He has been offered with fellowships and awards from DAAD, Shastri Indo Canadian Institute (SICI), ASEM Duo, United States-India Educational Foundation (Fulbright-Nehru Academic and Professional Excellence). His research interests are in the areas of high-speed interconnects, optics & photonics-based devices, image processing, spintronics-based devices, circuits and computing.