Circuits, Systems, and Signal Processing (2022) 41:3623
https://doi.org/10.1007/s00034-022-02010-w

CORRECTION

Correction to: FPGA Design of a Variable Step-Size Variable Tap Length Denlms Filter with Hybrid Systolic-Folding Structure and Compressor-Based Booth Multiplier for Noise Reduction in Ecg Signal

Miloni M. Ganatra[1,2] · **Chandresh H. Vithalani**[3]

Published online: 4 April 2022

Correction to: Circuits, Systems, and Signal Processin

https://doi.org/10.1007/s00034-021-01933-0

In this article the affiliation for Author Miloni M. Ganatra should have been Electronics and Communication Engineering Department, Indus University, Ahmedabad, Gujarat, India and Gujarat Technological University, Gujarat, India.

The original article has been corrected.

The original article can be found online at https://doi.org/10.1007/s00034-021-01933-0.

✉ Miloni M. Ganatra
miloniganatra87@gmail.com

Chandresh H. Vithalani
chvgec@gmail.com

1 Electronics and Communication Engineering Department, Indus University, Ahmedabad, Gujarat, India

2 Gujarat Technological University, Ahmedabad, Gujarat, India

3 Electronics and Communication Engineering Department, Government Engineering College, Rajkot, Gujarat, India