Time-Domain Digital-to-Analog Converter for Spiking Neural Network Hardware

Seiji Uenohara¹ · Kazuyuki Aihara^{1,2}

Received: 23 August 2019 / Revised: 1 November 2020 / Accepted: 5 November 2020 /

Published online: 11 December 2020

© The Author(s) 2020

Abstract

We propose a new digital-to-analog converter (DAC) for realizing a synapse circuit in mixed-signal spiking neural networks. We refer to this circuit as a “time-domain DAC (TDAC)”. It produces weights for converting a digital input code into voltage using one current waveform. Therefore, the TDAC is more compact than a conventional DAC consisting of many current sources and resistors. Moreover, a TDAC with leak resistance reproduces biologically plausible synaptic responses expressed as alpha functions or dual exponential equations. We also present numerical analysis results for a TDAC and circuit simulation results for a circuit designed using the TSMC 40 nm CMOS process.

Keywords DA converter · Spiking neural network · Mixed signal · Near-memory computing

1 Introduction

Application-specific integrated circuits (ASICs) for neuromorphic hardware have been studied intensively with the aim of achieving highly efficient computation [2,5,11,18,20,25]. Although most neuromorphic hardware is designed with digital circuits [2,4,8–10,12,22], some studies have sought higher efficiency by using analog circuits [11,18] owing to the advantage that highly efficient multiply-accumulate (MAC) operations can be achieved.

✉ Seiji Uenohara
s.uenohara@gmail.com; uenohara@sat.t.u-tokyo.ac.jp

Kazuyuki Aihara
aihara@sat.t.u-tokyo.ac.jp

¹ Institute of Industrial Science, The University of Tokyo, 4-6-1 Komaba, Meguro-ku, Tokyo 153-8505, Japan

² International Research Center for Neurointelligence, University of Tokyo, 7-3-1 Hongo, Bunkyo-ku, Tokyo 113-8654, Japan

Neuromorphic computation requires many MAC operations for the input signals and synaptic weights, and therefore, implementation of highly efficient MAC operations is important for realizing highly efficient neuromorphic hardware. To improve the energy efficiency of MAC operations, attempts have been made to (i) binarize the synaptic weights, (ii) realize weighted summation using current (wired-sum), (iii) realize weighted summation using capacitors, and (iv) develop a method that combines (i) and (ii) or (i) and (iii).

Bankman et al. [5] realized a highly energy-efficient binary convolution neural network chip as a recognition processor. In the circuit, the synaptic weights express binary information and are stored in digital memory. The weighted summation is then calculated by converting the binary information into analog voltages. The capacitors on this chip for weighted summation work also as a digital-to-analog converter (DAC), and this circuit is categorized as a mixed-signal circuit. A mixed-signal circuit that has multi-bit synaptic weights requires a large footprint area and a large amount of energy for the DAC, but the chip developed by Bankman et al. has low power consumption because the synaptic weights are restricted to be binary and the weighted summation is realized by capacitance coupling.

Weighted summation by current is often used in analog neuromorphic hardware [11,15,21,25,28]. In such circuits, the current is produced by synapse circuits. Current-based summation is implemented very simply by connecting each of the metal lines of the synaptic output. In analog neuromorphic hardware, synaptic weights are often expressed by analog voltages that are maintained by capacitors. A circuit with this architecture is highly efficient, but it is difficult to reuse the capacitors that hold the synaptic weights because they cannot hold the weights for a long time due to charge leakage. To solve this problem, there have been many studies of synapse circuits that use analog memory [1,6,13,23,26]. However, many problems need to be solved in order to establish analog memory as a reliable technology. For example, ferroelectric random access memory (FeRAM) suffers from a parasitic charge trapping effect that degrades endurance [29]. Resistive random access memory (ReRAM) is expected as high-integration and high-speed memory, but it may exhibit stochastic switching behavior depending on the composition of the filaments, and this mechanism is still not well understood [7].

To realize highly efficient neuromorphic hardware with reusable synaptic weights that is fabricated using conventional complementary metal–oxide–semiconductor (CMOS) technology, synaptic weights of the circuit architecture can be stored in digital memory and MAC operations can be achieved by an analog circuit; in other words, a mixed-signal architecture is suitable. Realizing a mixed-signal circuit that has multi-bit synaptic weights is important for achieving on-chip learning, but it is difficult to realize high-integration and highly efficient neuromorphic hardware because conventional multi-bit DACs comprise many current-source circuits or resistor arrays, thereby necessitating a large footprint and high power consumption [14,17]. It is especially difficult to implement a highly energy-efficient asynchronous spiking neural network (SNN) chip that has multi-bit synaptic weights because using one DAC per time division is difficult in an asynchronous system.

Figure 1 shows the principal circuits of conventional 4-bit DACs where S_0 – S_3 are the individual values of a bit code, V_{ref} is the reference voltage, I_{ref} is the reference

Fig. 1 Principal circuits of conventional digital-to-analog converters (DACs): (a) resistor string type; (b) current array type; (c) capacitor array type; (d) R2R ladder type; (e) MOS ladder type

current, V_{out} is the output voltage, and I_{out} is the output current. Most conventional DACs consist of circuit elements (CEs) for realizing the weight of the bit code (e.g., resistors, capacitors, and current sources) and switches. It is difficult to implement the resistor string type (Fig. 1(a)), the current array type (Fig. 1(b)), and the capacitor array type [3] (Fig. 1(c)) in highly integrated forms because in those cases the number of CEs increases exponentially as the DAC bit length n increases. However, the R2R ladder type [24] (Fig. 1(d)) and the MOS ladder type (Fig. 1(e)) are highly advantageous because the number of CEs increases only linearly with n . Based on Fig. 1, the CE components and their numbers are summarized in Table 1. Our work will be described later.

In general, resistors and capacitors necessitate a larger footprint than do transistors in CMOS technology, and the CEs are designed to have larger dimensions than transistors that consist of logic gates in order to reduce the influence of fabrication mismatch. Therefore, to implement high-integration and highly efficient mixed-signal SNN hardware with on-chip learning having multi-bit synaptic weights, a suitable DAC architecture is one with neither resistors nor capacitors, or one but with few CEs, the number of which does not increase with the number of bits.

Toward SNN hardware, we propose a new DAC circuit that weights each bit of digital memory by using a current (or voltage) waveform. This makes our DAC more compact than conventional ones, and we refer to this DAC as a “time-domain” DAC (TDAC). A TDAC has the advantages that (i) it can reproduce a postsynaptic potential (PSP) and (ii) its number of CEs is independent of the bit width. Herein, we present the results of numerical analysis of TDAC and circuit simulation.

This paper is organized as follows. In Sect. 2, we explain the principle of TDAC, and in Sect. 3, we present a numerical analysis. Circuit design of TDAC and circuit simulation results are shown in Sect. 4. Finally, we conclude the paper in Sect. 6.

2 Circuit Principle of Time-Domain Digital-to-Analog Converter

Figure 2a shows the TDAC principle in circuit form, and we explain the operation of a 4-bit TDAC as an example. The TDAC consists of an analog block and a digital block that comprise AND gates, an OR gate, switches, a switched current source (SCS), resistors, and capacitors. The digital memory values are B_1 – B_4 , and in this example, B_1 and B_4 are the least significant bit (LSB) and the most significant bit (MSB), respectively. $S_{in}(t)$ is the trigger signal for activating the DAC and corresponds to spike pulses when the TDAC is used as the output stage of a synapse circuit. Signals $S_{B,1}(t)$ – $S_{B,4}(t)$ are non-overlapping digital signals with pulse width t_w for the DAC, and these values are either zero or unity. The SCS outputs a current $I_{out}(t) (\propto V_{non}(t))$, and the leak resistance R_{out} is an option for realizing the waveform of synaptic potential.

The DAC process using the TDAC without the leak resistance R_{out} is as follows (Fig. 2b):

- (1) When $S_{in}(t)$ is high, $V_{non}(t)$ is set to V_{set} .

Table 1 Comparison of proposed and other DACs

	CEs realizing weight	No. of CEs	No. of TRs for SW and logic	Postsynaptic potential reproducibility
Resistor string	Resistors	2^n	4^n	
Current array	Current sources	2^n	$4n$	
Capacitor array	Capacitors	2^n	$10n + 4$	
R2R ladder	Resistors	$3n$	$10n$	
MOS ladder	MOS TRs	$4n$	0	
Time domain (this work)	Two CR circuits and SCS	5	$25n + 8$	✓

CEs: circuit elements; TRs: transistors; SW: switch; SCS: switched current source

Fig. 2 Principle of the time-domain DAC (TDAC) in circuit form: **a** circuit; **b** voltage waveform of each node of the circuit in **a**

- (2) When $S_{in}(t)$ turns off, $S_{B,4}(t)$ is generated at the trailing edge of $S_{in}(t)$. At the same time, $V_{non}(t)$ increases exponentially with time constant $C_{lk}R_{lk}$. If B_4 is high, then capacitor C_{out} is charged during t_w by a current proportional to $V_{non}(t)$.
- (3) $S_{B,3}(t)$ is generated at the trailing edge of $S_{B,4}$. If B_3 is high, capacitor C_{out} is charged during t_w by a current that is proportional to $V_{non}(t)$.
- (4) Operation 3) is repeated until $S_{B,1}(t)$ is generated.

For example, $V_{out,1110}$ represents the voltage-converted digital input code $(1110)_2$ (Fig. 2b) that is obtained by charging, charging, charging, and not charging.

Conventional DACs use many resistors or current sources to weight each bit of digital memory. Implementing these circuit components causes the footprint area to be squared for every unit increase in the length of the memory. By contrast, a TDAC uses a current waveform to weight each memory bit. In the TDAC, the numbers of AND gates, OR gates, and signal generators of $S_{B,k}$ needed to sample the current waveform increases as the length of the memory increases. Therefore, the number of transistors increases linearly, but the disadvantage is that the time taken by the DAC increases. A TDAC is suitable for hardware that must be compact and operate at low speed, such as SNN hardware. In this example, the output current is positive but the TDAC can output negative current.

3 Numerical Analysis of Time-Domain Digital-to-Analog Converter

3.1 Time-Domain Digital-to-Analog Conversion Without Leak Resistance

We define the time of the trailing edge of $S_{in}(t)$ to be zero, and we express the voltage $V_{out}(t)$ as

$$V_{out}(t) = \sum_{k=0}^{q-1} \int_{kt_w}^{(k+1)t_w} B_{q-k} \frac{f_{scs}(V_{non}(t))}{C_{out}} dt, \quad (1)$$

where q is the memory length, t is continuous time ($t \geq 0$), and $f_{scs}(\cdot)$ characterizes the SCS. In this section, we analyze the TDAC when $V_{non}(t)$ is described by $V_{set} \exp(-\frac{t}{C_{lk} R_{lk}})$ and $f_{scs}(V_{non}(t)) = V_{non}(t)$. Under these conditions, Eq. (1) is expressed as

$$V_{out}(t) = \frac{V_{set}}{C_{out}} \sum_{k=0}^{q-1} \int_{kt_w}^{(k+1)t_w} B_{q-k} \exp\left(-\frac{t}{C_{lk} R_{lk}}\right) dt. \quad (2)$$

We integrate Eq. (2) to obtain

$$V_{out}(t) = \frac{V_{set}}{C_{out}} \sum_{k=0}^{q-1} -B_{q-k} C_{lk} R_{lk} \left(\exp\left(-\frac{(k+1)t_w}{C_{lk} R_{lk}}\right) - \exp\left(-\frac{kt_w}{C_{lk} R_{lk}}\right) \right). \quad (3)$$

To ensure that the DAC characteristics remain linear, the weight of the upper bit of the adjacent must be twice that of the lower bit, namely

$$\frac{\left(\exp\left(-\frac{(k+1)t_w}{C_{lk} R_{lk}}\right) - \exp\left(-\frac{kt_w}{C_{lk} R_{lk}}\right) \right)}{\left(\exp\left(-\frac{(k+2)t_w}{C_{lk} R_{lk}}\right) - \exp\left(-\frac{(k+1)t_w}{C_{lk} R_{lk}}\right) \right)} = 2. \quad (4)$$

We solve Eq. (4) to obtain

$$\frac{t_w}{C_{lk} R_{lk}} = \ln 2. \quad (5)$$

Figure 3 shows the input–output characteristics of the TDAC obtained from numerical simulation for varying $\frac{t_w}{C_{lk} R_{lk}}$. As shown therein, the characteristics are linear when $\frac{t_w}{C_{lk} R_{lk}} = \ln 2$ but nonlinear otherwise. In particular, monotonicity is also lost when $\frac{t_w}{C_{lk} R_{lk}} < \ln 2$.

3.2 Time-Domain Digital-to-Analog Conversion With Leak Resistance

When a TDAC is used as the output stage of a synaptic circuit, we can view C_{out} as the membrane capacitance of an analog neuron circuit, where the leak resistance R_{out} is connected in parallel with C_{out} . In this situation, the temporal variation of $V_{out}(t)$ with R_{out} is expressed by

$$\frac{dV_{out}(t)}{dt} = -\frac{V_{out}(t)}{C_{out} R_{out}} + V_{set} \exp\left(-\frac{t}{C_{lk} R_{lk}}\right) \sum_{k=0}^{q-1} S_{B,q-k}(t) B_{q-k}. \quad (6)$$

Fig. 3 Input–output characteristics of TDAC obtained from numerical simulation for varying $\frac{t_w}{C_{lk}R_{lk}}$

We will show that Eq. (6) fits well with biological data on synaptic potentials when all the memory bits are unity and qt_w is sufficient large, in which case $\sum_{k=0}^{q-1} S_{B,q-k}(t)B_{q-k}$ is nearly unity regardless of t . We assume that $V_{out}(0)$ is zero, and in this case Eq. (6) is expressed as

$$\frac{dV_{out}(t)}{dt} = -\frac{V_{out}(t)}{C_{out}R_{out}} + V_{set} \exp\left(-\frac{t}{C_{lk}R_{lk}}\right). \quad (7)$$

We solve Eq. (7) by using the method of variation of constants, setting $C_{out}R_{out} = \tau_1$ and $C_{lk}R_{lk} = \tau_2$. The solution of Eq. (7) is given by

$$V_{out}(t) = g(t) \exp\left(\frac{-t}{\tau_1}\right), \quad (8)$$

where $g(\cdot)$ is a function of time. By using Eqs. (7) and (8), $\frac{dV_{out}(t)}{dt}$ is expressed as

$$\begin{aligned} \frac{dV_{out}(t)}{dt} &= g'(t) \exp\left(-\frac{t}{\tau_1}\right) - \frac{1}{\tau_1} g(t) \exp\left(-\frac{t}{\tau_1}\right), \\ g'(t) &= V_{set} \exp\left(-\frac{\tau_1 - \tau_2}{\tau_1 \tau_2} t\right). \end{aligned} \quad (9)$$

If $\tau_1 = \tau_2$, then the integral of Eq. (9) with respect to t is tV_{set} because $g'(t)$ is a constant. In this case, $V_{out}(t)$ is given by

$$V_{out}(t) = tV_{set} \exp\left(\frac{-t}{\tau_1}\right), \quad (10)$$

which is an alpha function.

If $\tau_1 \neq \tau_2$, then the integral of Eq. (9) with respect to t is

$$g(t) = -\frac{\tau_1 \tau_2}{\tau_1 - \tau_2} V_{set} \exp\left(-\frac{\tau_1 - \tau_2}{\tau_1 \tau_2} t\right) + g_c, \quad (11)$$

where g_c is a constant of integration. By using $V_{out}(0) = 0$, we obtain $g_c = \frac{\tau_1 \tau_2}{\tau_1 - \tau_2} V_{set}$. Substituting g_c for $g(t)$, we obtain

$$g(t) = -\frac{\tau_1 \tau_2}{\tau_1 - \tau_2} V_{set} \left(1 - \exp\left(-\frac{\tau_1 - \tau_2}{\tau_1 \tau_2} t\right)\right). \quad (12)$$

Substituting Eq. (12) for Eq. (8), we obtain

$$V_{out}(t) = \frac{\tau_1 \tau_2}{\tau_1 - \tau_2} V_{set} \left(\exp\left(-\frac{t}{\tau_1}\right) - \exp\left(-\frac{t}{\tau_2}\right)\right), \quad (13)$$

which is a dual exponential function. It is known that alpha and dual exponential functions fit well to biological data on synaptic potentials [16,19,27].

Figure 4 shows synaptic potential waveforms obtained from numerical simulation. Panels (a) and (b) show the waveforms with the alpha function ($\tau_1 = \tau_2$), and (c) and (d) show those with the dual exponential function ($\tau_1 \neq \tau_2$). To obtain panels (a) and (c) and panels (b) and (d), we changed $\frac{t_w}{\tau_2}$ and the digital input code, respectively. In panels (a) and (c), the waveforms are so similar that they cannot be distinguished visually, and the peak of the potential does not change when $\frac{t_w}{\tau_2}$ is varied. By contrast, as shown in panels (b) and (d), when the input code is $(10101010)_2$ or $(01010101)_2$, the peak changes. In the TDAC, C_{out} is not charged during $S_{B,k}$ when memory bit k is zero, and this is caused by alternating charging and leaking. Moreover, the upper bit is converted into analog current faster than the lower one. However, we can ignore the influence of these when qt_w is sufficiently smaller than the time constant of the membrane potential of a neuron circuit.

4 Proposed Circuit

A block diagram of our proposed circuit is shown in Fig. 5, where an 8-bit (sign+7) DAC can output negative and positive current. The circuit consists of a digital block and an analog block, the details of which are shown in Fig. 6.

The digital block consists of logic gates and delay circuits (DLs). Each DL consists of 11 transistors that output $S_{B,k}$ with pulse width t_w . The pulse width is the adjusted bias voltage V_{dl} . If the bit-length of the TDAC increases, then an additional DL, two NAND gates, a NOT gate, two NMOS transistors, and two PMOS transistors are required, thereby increasing the total number of transistors by 25. The output signal of the digital block is the input for the analog block.

The analog block consists of voltage-controlled current sources, switches, MOS resistors, and MOS capacitors. Negative and positive current outputs are realized by transistors M_n and M_p , respectively. The number of transistors in the analog block does

Fig. 4 Synaptic potential waveforms obtained from numerical simulation: **a** $\tau_1 = 1$ and $\tau_2 = 1$ when $\frac{t_w}{\tau_2}$ is varied; **b** $\tau_1 = 1$ and $\tau_2 = 1$ when the DAC digital input code is varied; **c** $\tau_1 = 1$ and $\tau_2 = 0.5$ when $\frac{t_w}{\tau_2}$ is varied; **d** $\tau_1 = 1$ and $\tau_2 = 0.5$ when the DAC digital input code is varied

not increase when the bit-length of the TDAC increases. We explain the operation of positive and negative current output in Sections 4.2 and 4.3, respectively.

4.1 Positive Current Output

The proposed circuit outputs positive current when B_8 is unity. As an example, Fig. 7a shows the timing diagram of the input signal and node voltages when the input digital bit code is $(11101000)_2$. The process for outputting positive current is as follows.

- (1) When $S_{in}(t)$ turns high, $S_{rsp}(t)$ and $S_{sip}(t)$ turn high and low, respectively. At the same time, $V_{gp}(t)$ is set to V_{rsp} , where V_{rsp} is a small voltage.
- (2) When $S_{in}(t)$ turns off, $S_{B,7}(t)$ is generated at the trailing edge of $S_{in}(t)$. At the same time, $V_{gp}(t)$ increases exponentially.

Fig. 5 Block diagram of proposed 8-bit TDAC

- (3) $S_{B,6}(t)$ is generated at the trailing edge of $S_{B,7}$. If B_6 is high, then capacitor C_{out} is charged during t_w by M_p .
- (4) Operation 3 is repeated until $S_{B,1}(t)$ is generated.

We prevent wasteful power consumption by setting $S_{stp}(t)$ to low while $S_{in}(t)$ is high. This is because wasteful current flows from M_5 to M_4 if $S_{stp}(t)$ is high while $S_{in}(t)$ is high.

4.2 Negative Current Output

The proposed circuit outputs negative current when B_8 is zero. Figure 7b shows the timing diagrams of the input signal and node voltages when the input digital bit code is $(01101000)_2$. The process for outputting positive current is as follows.

- (1) When $S_{in}(t)$ turns high, $S_{rsn}(t)$ and $S_{stn}(t)$ turn low and high, respectively. At the same time, $V_{gn}(t)$ is set to V_{rsn} , where V_{rsn} is a high voltage.
- (2) When $S_{in}(t)$ turns off, $S_{B,7}(t)$ is generated at the trailing edge of $S_{in}(t)$. At the same time, $V_{gn}(t)$ decreases exponentially.
- (3) $S_{B,6}(t)$ is generated at the trailing edge of $S_{B,7}$. If B_6 is high, then capacitor C_{out} is charged during t_w by M_n .
- (4) Operation 3 is repeated until $S_{B,1}(t)$ is generated.

We prevent wasteful power consumption by setting $S_{stn}(t)$ to high while $S_{in}(t)$ is high. This is because wasteful current flows from M_9 to M_{10} if $S_{stn}(t)$ is low while $S_{in}(t)$ is high.

Symbol **Schematic**

(a)

Symbol **Schematic**

(b)

Symbol **Schematic** M_p, M_n : voltage controlled current source M_4, M_9 : switch M_5, M_{10} : MOS resistor for leak M_3, M_8 : MOS capacitor

(c)

Fig. 6 Details of the **a** digital block, **b** delay circuit, and **c** analog block of the proposed circuit

Fig. 7 Timing diagrams of input signal and node voltages for **a** positive and **b** negative current output operations

5 Circuit Simulation

5.1 Time-Domain Digital-to-Analog Conversion Without Leak Resistance

We designed an 8-bit TDAC as shown in Fig. 5 with the TSMC 40 nm CMOS process (1 poly, 8 metal), and we evaluated the circuit by means of the Spectre simulation. We set the bias voltages and the capacitance as $V_{DD} = 700$ mV, $V_{dl} = 180$ mV, $V_{lkp} = 140$ mV, $V_{lkn} = 420$ mV, and $C_{out} = 0.5$ pF, and the output voltage $V_{out}(t)$ was reset to 350 mV on every input.

Figure 8 shows the input–output characteristics of the TDAC when V_{rsn} and V_{rsp} are varied separately. In the designed 8-bit TDAC, the output current is negative when

Fig. 8 Input–output characteristics of TDAC

the digital input code is between zero and 128, and it is positive when the digital input code is between 129 and 255. The slopes of the characteristics in the two regions can be adjusted separately by varying V_{rsn} and V_{rsp} as shown in Fig. 8. The energy per one digital-to-analog conversion is 27 fJ when the digital input code is (1111111)₂ and $V_{rsp} = 0$ mV.

5.2 Time-Domain Digital-to-Analog Conversion With Leak Resistance

The circuit simulation for synaptic-potential generation was conducted by adding a MOS resistance between the output node and the ground. We set the bias voltages and the capacitance as $V_{DD} = 700$ mV, $V_{dl} = 340$ mV, $V_{lkp} = 300$ mV, $V_{lkn} = 300$ mV, $V_{rsn} = 570$ mV, $V_{rsp} = 70$ mV, and $C_{out} = 0.5$ pF.

Figure 9 shows the synaptic-potential waveforms for various digital input codes $S_{in}(t)$ and DL outputs. As shown in Fig. 4, which was obtained by numerical simulation, the waveforms are smooth when the lined bit is unity or zero, but in other cases the waveform has multiple peaks. We obtained waveforms that are similar to those from the numerical simulation.

5.3 Application of Time-Domain Digital-to-Analog Converter to a Leaky Integrate-and-Fire Neuron Circuit

To demonstrate that the TDAC works as a synapse circuit of an SNN circuit, we applied the TDAC to a leaky integrate-and-fire (LIF) neuron circuit. Figure 10 shows an LIF neuron circuit and a block diagram of the LIF circuit with synapse circuits. The TDAC in this figure is the same circuit as shown in Fig. 5. In this situation, the digital input code to the m th TDAC represents a synaptic weight W_m .

Fig. 9 Synaptic-potential waveforms obtained from circuit simulation for various DAC digital input codes

The neuron circuit in Fig. 10a integrates the currents from the TDACs by capacitor C_x , and membrane potential $V_x(t)$ is generated. The MOS transistor M_k works as a leak resistor. Voltages V_{lk} and V_{rst} are the resting membrane potential and the reset potential, respectively (Fig. 10b). When $V_x(t)$ reaches V_{th} , output spike $S_{out}(t)$ is generated and $V_x(t)$ is reset to V_{rst} . The bias voltages V_{bp1} and V_{bp2} adjust the firing threshold voltage V_{th} and the spike pulse width of $S_{out}(t)$ by varying the rising time of V_a and V_b . Voltage V_x is reset to V_{rst} when $V_x(t)$ reaches V_{th} . The current output nodes of the TDACs connect to $V_x(t)$ as shown in Fig. 10c to achieve current-based summation asynchronously. Each TDAC has no resistor or capacitor for generating a PSP because the LIF circuit includes those components as M_k and C_x .

A circuit simulation with the LIF circuit was conducted. We used four TDACs as synapse circuits and set the bias voltages and the capacitance as $V_{DD} = 700$ mV, $V_{dl} = 340$ mV, $V_{lkp} = 300$ mV, $V_{lkn} = 300$ mV, $V_{rstn} = 570$ mV, $V_{rstp} = 200$ mV, $V_{rst} = 200$ mV, $V_{xlk} = 200$ mV, $V_{lk} = 550$ mV, $V_{bp1} = 100$ mV, $V_{bp2} = 100$ mV,

Fig. 10 Details of the **a** leaky integrate-and-fire (LIF) neuron circuit, **b** timing diagram of the input/output signal and node voltages of the LIF circuit, and **c** block diagram of the LIF circuit with synapse circuits

and $C_x = 0.5$ pF. The values of the synaptic weights are $W_1 = (11000000)_2$, $W_2 = (10100000)_2$, $W_3 = (01111000)_2$, and $W_4 = (11101011)_2$. Here, W_3 is negative because the MSB is zero. The periods of input spikes $S_{in,1}$, $S_{in,2}$, $S_{in,3}$, and $S_{in,4}$ are 210 ns, 230 ns, 250 ns, and 270 ns, respectively.

The results of the circuit simulation are shown in Fig. 11. As shown in Fig. 11, a PSP is generated when the spike pulse arrives, and the neuron circuit generates spike pulse

Fig. 11 Membrane-potential waveform and input/output spikes during a LIF neuron operation with the time-domain digital-to-analog converter obtained from circuit simulation

$S_{out}(t)$ when $V_x(t)$ reaches V_{th} . The LIF circuit and the TDAC have no clock signal, and their operations start with the input spikes as their trigger; thus, the SNN circuit is an asynchronous system like biological neural networks. The circuit simulation results show that the TDAC can be used to implement neuromorphic hardware.

6 Conclusion

We proposed a new DAC, called a TDAC, in which the weight of each bit that codes for the DAC is realized by a current waveform sampled using non-overlapping digital signals. The number of transistors needed to implement a TDAC increases linearly with the bit-length, but the transistors can be made small because they work as a digital circuit. A TDAC is therefore more compact than a conventional DAC in which the number of transistors increases exponentially with increasing bit-length. Moreover, a TDAC with leak resistance realizes biologically plausible synaptic responses without the need for other circuit components. TDACs are therefore suitable for implementing

mixed-signal SNN hardware that requires high integration. Moreover, a circuit simulation showed that a TDAC works as a synapse circuit of SNNs by applying a TDAC to an LIF neuron circuit.

We showed the condition under which a TDAC remains linear, namely, that the ratio of the pulse width for sampling the current waveform to the time constant should be $\ln 2$. To realize a TDAC that has good linearity and is robust against fabrication mismatches, the pulse width (resp. the time constant) should be set according to the time constant (resp. the pulse width), and we intend to develop such a circuit in our future work.

Acknowledgements This work was supported by the VLSI Design and Education Center (VDEC) of the University of Tokyo in collaboration with Cadence Design Systems, Inc. This work was also supported by the BMAI Project at IIS of the University of Tokyo.

Open Access This article is licensed under a Creative Commons Attribution 4.0 International License, which permits use, sharing, adaptation, distribution and reproduction in any medium or format, as long as you give appropriate credit to the original author(s) and the source, provide a link to the Creative Commons licence, and indicate if changes were made. The images or other third party material in this article are included in the article's Creative Commons licence, unless indicated otherwise in a credit line to the material. If material is not included in the article's Creative Commons licence and your intended use is not permitted by statutory regulation or exceeds the permitted use, you will need to obtain permission directly from the copyright holder. To view a copy of this licence, visit <http://creativecommons.org/licenses/by/4.0/>.

References

1. S.P. Adhikari, C. Yang, H. Kim, L.O. Chua, Memristor bridge synapse-based neural network and its learning. *IEEE Trans. Neural Netw. Learn. Syst.* **23**(9), 1426–1435 (2012)
2. F. Akopyan, J. Sawada, A. Cassidy, R. Alvarez-Icaza, J. Arthur, P. Merolla, N. Imam, Y. Nakamura, P. Datta, G.J. Nam et al., Truenorth: Design and tool flow of a 65 mW 1 million neuron programmable neurosynaptic chip. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **34**(10), 1537–1557 (2015)
3. J.F. Albarran, D.A. Hodges, A charge-transfer multiplying digital-to-analog converter. *IEEE J. Solid-State Circuits* **11**(6), 772–779 (1976)
4. K. Ando, K. Ueyoshi, K. Orimo, H. Yonekawa, S. Sato, H. Nakahara, S. Takamaeda-Yamazaki, M. Ikebe, T. Asai, T. Kuroda et al., Brein memory: A single-chip binary/ternary reconfigurable in-memory deep neural network accelerator achieving 1.4 TOPS at 0.6 W. *IEEE J. Solid-State Circuits* **53**(4), 983–994 (2017)
5. D. Bankman, L. Yang, B. Moons, M. Verhelst, Murmann, B. An always-on 3.8 $\mu\text{J}/86\%$ CIFAR-10 mixed-signal binary CNN processor with all memory on chip in 28nm CMOS. In: *Int. Solid State Circuits Conf.*, pp. 222–224. IEEE (2018)
6. G.W. Burr, R.M. Shelby, A. Sebastian, S. Kim, S. Kim, S. Sidler, K. Virwani, M. Ishii, P. Narayanan, A. Fumarola et al., Neuromorphic computing using non-volatile memory. *Adv. Phys. X* **2**(1), 89–124 (2017)
7. A. Chen, A review of emerging non-volatile memory (NVM) technologies and applications. *Solid-State Electron.* **125**, 25–38 (2016)
8. G.K. Chen, R. Kumar, H.E. Sumbul, P.C. Knag, R.K. Krishnamurthy, A 4096-neuron 1M-synapse 3.8-pJ/SOP spiking neural network with on-chip STDP learning and sparse weights in 10-nm FinFET CMOS. *IEEE J. Solid-State Circuits* **54**(4), 992–1002 (2018)
9. S.G. Cho, E. Beigné, Z. Zhang, A 2048-neuron spiking neural network accelerator with neuro-inspired pruning and asynchronous network on chip in 40nm CMOS. In: *Proc. Cust. Integr. Circuits Conf.*, pp. 1–4. IEEE (2019)
10. M. Davies, N. Srinivasa, T.H. Lin, G. Chinya, Y. Cao, S.H. Choday, G. Dimou, P. Joshi, N. Imam, S. Jain et al., Loihi: A neuromorphic manycore processor with on-chip learning. *IEEE Micro* **38**(1), 82–99 (2018)

11. G. Indiveri, F. Corradi, N. Qiao, Neuromorphic architectures for spiking deep neural networks. In: *Int. Electron. Devices Meet.*, pp. 4–2. IEEE (2015)
12. H. Kim, H. Tang, W. Choi, J. Park, An energy-quality scalable STDP based sparse coding processor with on-chip learning capability. *IEEE Trans. Biomed. Circuits Syst.* **14**(1), 125–137 (2020)
13. D. Kuzum, S. Yu, H.P. Wong, Synaptic electronics: materials, devices and applications. *Nanotechnology* **24**(38), 382001–1–22 (2013)
14. T. Miki, Y. Nakamura, M. Nakaya, S. Asai, Y. Akasaka, Y. Horiba, An 80-Mhz 8-bit CMOS D/A converter. *IEEE J. Solid-State Circuits* **21**(6), 983–988 (1986)
15. R. Mochida, K. Kouno, Y. Hayata, M. Nakayama, T. Ono, H. Suwa, R. Yasuhara, K. Katayama, T. Mikawa, Y. Gohou, A 4M synapses integrated analog ReRAM based 66.5 TOPS/W neural-network processor with cell current controlled writing and flexible network architecture. In: *Symp. VLSI Tech.*, pp. 175–176. IEEE (2018)
16. T.S. Otis, Y. De Koninck, I. Mody, Characterization of synaptically elicited GABAB responses using patch-clamp recordings in rat hippocampal slices. *J. Physiol.* **463**(1), 391–407 (1993)
17. H.U. Post, K. Schoppe, A 14-bit monotonic NMOS D/A converter. *IEEE J. Solid-State Circuits* **18**(3), 297–301 (1983)
18. N. Qiao, H. Mostafa, F. Corradi, M. Osswald, F. Stefanini, D. Sumislawska, G. Indiveri, A reconfigurable on-line learning spiking neuromorphic processor comprising 256 neurons and 128K synapses. *Front. Neurosci.* **9**, 141–1–17 (2015)
19. W. Rall, R. Burke, T. Smith, P.G. Nelson, K. Frank, Dendritic location of synapses and possible mechanisms for the monosynaptic EPSP in motoneurons. *J. Neurophysiol.* **30**(5), 1169–1193 (1967)
20. J. Schemmel, J. Fieries, K. Meier, Wafer-scale integration of analog neural networks. In: *Proc. Int. Jt. Conf. Neural Netw.*, pp. 431–438. IEEE (2008)
21. J. Schemmel, L. Kriener, P. Müller, K. Meier, An accelerated analog neuromorphic hardware system emulating nmda-and calcium-based non-linear dendrites. In: *Proc. Int. Jt. Conf. Neural Netw.*, pp. 2217–2226. IEEE (2017)
22. T. Schoenauer, S. Atasoy, N. Mehrtash, H. Klar, NeuroPipe-Chip: A digital neuro-processor for spiking neural networks. *IEEE Trans. Neural Netw.* **13**(1), 205–213 (2002)
23. K. Seo, I. Kim, S. Jung, M. Jo, S. Park, J. Park, J. Shin, K.P. Biju, J. Kong, K. Lee et al., Analog memory and spike-timing-dependent plasticity characteristics of a nanoscale titanium oxide bilayer resistive switching device. *Nanotechnology* **22**(25), 254023–1–5 (2011)
24. B. Smith, Coding by feedback methods. In: *Inst. Electr. Electron. Eng.*, vol. 41, pp. 1053–1058. IEEE (1953)
25. H. Tanaka, T. Morie, K. Aihara, A CMOS spiking neural network circuit with symmetric/asymmetric STDP function. *IEICE Trans. Fundamentals* **92**(7), 1690–1698 (2009)
26. Y.F. Wang, Y.C. Lin, I.T. Wang, T.P. Lin, T.H. Hou, Characterization and modeling of nonfilamentary Ta/TaO x/TiO 2/Ti analog synaptic device. *Sci. Rep.* **5**, 10150–1–9 (2015)
27. M. Wilson, J.M. Bower, Cortical oscillations and temporal interactions in a computer simulation of piriform cortex. *J. Neurophysiol.* **67**(4), 981–995 (1992)
28. C.X. Xue, W.H. Chen, J.S. Liu, J.F. Li, W.Y. Lin, W.E. Lin, J.H. Wang, W.C. Wei, T.Y. Huang, T.W. Chang et al., Embedded 1-Mb ReRAM-based computing-in-memory macro with multibit input and weight for CNN-based AI edge processors. *IEEE J. Solid-State Circuits* **55**(1), 203–215 (2019)
29. E. Yurchuk, S. Mueller, D. Martin, S. Slesazek, U. Schroeder, T. Mikolajick, J. Müller, J. Paul, R. Hoffmann, J. Sundqvist, et al. Origin of the endurance degradation in the novel HfO 2-based 1t ferroelectric non-volatile memories. In: *Proc. Int. Reliab. Phys. Symp.*, pp. 2E–5. IEEE (2014)