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An Ultra-Low-Energy Analog Comparator for A/D Converters in CMOS Image Sensors

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Abstract This paper proposes a new solution of an ultra-low-energy analog comparator, dedicated to slope analog-to-digital converters (ADC), particularly suited for CMOS image sensors (CISs) featuring a large number of ADCs. For massively parallel imaging arrays, this number may be as high as tens-hundreds of thousands ADCs. As each ADC includes an analog comparator, the number of these comparators in CIS is always high. Detailed analysis shows that power dissipation of a comparator contributes significantly to a total power consumption of an ADC. Thus, minimization of the comparator energy consumption during the analog-to-digital (A/D) conversion of an image frame is crucial for design of CMOS image sensors. Compared to classical dynamic or continuous-time comparators operating in the slope ADC, under the same bias conditions, the proposed comparator shows a 2–3 orders of magnitude reduction of the power consumption. In addition, the proposed topology shows a simple and compact layout and does not require a power-down mechanism. The circuit has been simulated in detail for a 0.18-μm CMOS technology under two different power supply voltages of 1.8 and 1 V. While implemented in a 12-bit slope ADC of a massively parallel CIS, operating at a speed 1000 fps, the energy required for A/D conversion is 0.5 pJ.

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1 Introduction

Analog comparator is an intermediate element between the analog and digital domain of an analog-to-digital converter (ADC). The main comparator parameters such as resolution, speed, and noise directly affect the quality of analog-to-digital (A/D) conversion. Two other parameters, namely power consumption and area, become particularly important for circuits with high number of ADCs. The representative examples of such systems are CMOS image sensors (CISs) [10,16,19,20,22], especially massively parallel CISs [5,11–13,15,21]. For the latter, A/D conversion is implemented at the pixel level, as illustrated in Fig. 1a. Here, the power consumption and the area of a single pixel should be sufficiently small to minimize the total chip size and power consumption which are both proportional to the number of pixels and become nonnegligible even for a low-resolution sensors containing up to tens of thousands of pixels. For those reasons, a single-slope ADC is preferred for in-pixel implementation because it is simple and can be fitted within several hundred square micrometers of silicon surface. A complete N-bit single-slope ADC consists of an analog comparator and an N-bit time-to-digital converter (TDC) as illustrated in Fig. 1b. The TDC can be implemented as a fully digital circuit (e.g., as an N-bit counter), and, therefore, minimizing its layout area and power consumption is relatively easy, as opposed to a comparator, which is an analog circuit with very limited potential for area reduction.

Let us investigate the power consumption for two different types of CMOS comparators shown in Fig. 2: continuous time and discrete time (dynamic). The classic continuous-time comparator (Fig. 2a) consists of a MOS differential pair, biased by a current source, and of an additional gain stage [1]. In the ADC from Fig. 1b, such comparator draws a mean current of I_{bias} during the entire interval time T_{ramp}. One can say that until V_{ramp} becomes equal to V_{sense}, as well as after that time event, the
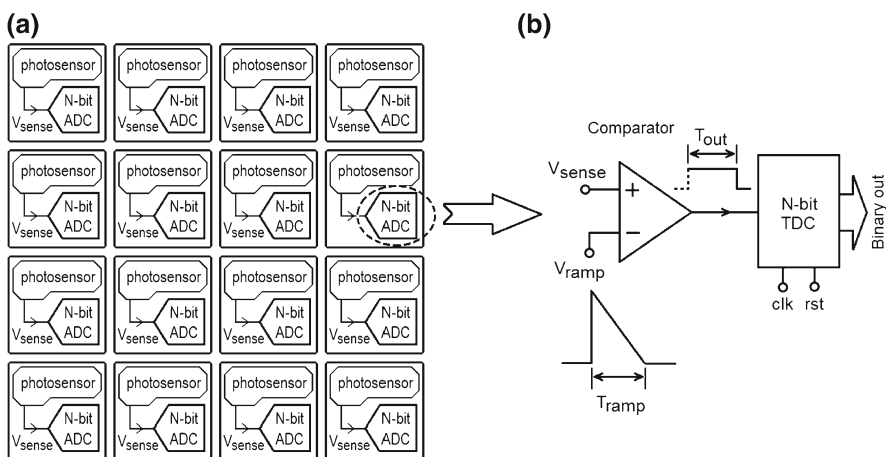

Fig. 1 Analog comparator in a massively parallel CIS: **a** 4x4 pixel sub-array of a large count array, **b** in-pixel ADC
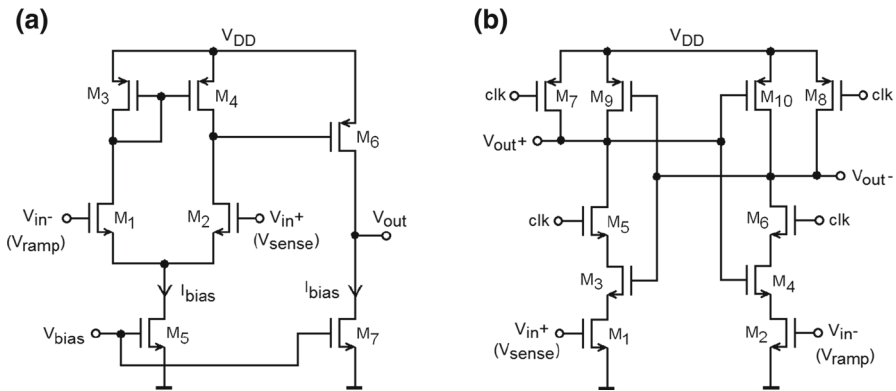
Fig. 2 Examples of the classic CMOS comparators: **a** continuous-time comparator with a differential pair [1], **b** discrete-time (dynamic) comparator with a latch [1,3,4]

comparator dissipates electric power in vain. The power dissipation can be reduced, e.g., by reducing the bias current. However, the current can be decreased only to a value that still provides the required slew rate (SR) at the comparator output and is related to the desired A/D conversion rate. In addition, an appropriate SR is necessary to properly control the digital circuits without excessive short-circuit currents in their operation. Because of these limitations, the power consumption of a continuous-time comparator can dominate a total power consumption of an ADC (up to 90% of a total consumption [13]).

The conventional discrete-time (dynamic) comparator from Fig. 2b is a regenerative latch, which is periodically regenerated and latched by a clock signal [1,3,4]. This comparator draws current from the power source only when the state changes, similarly to a digital circuit. The energy required to change the state can be as small as in a digital gate. However, the application range of this comparator in a slope ADC from Fig. 1b is sub-optimal in terms of energy consumption per single A/D conversion. The main reason for this is that throughout the time interval, T_{ramp}, a discrete-time comparator needs to check a voltage difference, $V_{\mathrm{sense}} - V_{\mathrm{ramp}}$, at regular intervals determined by the clock. It can be easily shown that the number of comparisons performed by the comparator during a single A/D conversion cycle is on the order of 2^N. For example, for a 10-bit converter the comparator performs 1024 comparisons. Each comparison (regeneration + latch) is related to the consumption of energy. As a result, the total energy consumption of this comparator may be comparable to that of a continuous-time comparator. Furthermore, multiple state transitions cause kickback noise which may become too high for a photosensor signal.

The energy consumption of both comparators can be reduced by power-down mechanism, which disables them after V_{ramp} and V_{sense} become equal. With this method, however, the energy required per A/D conversion of an image can only be reduced by half. This can be explained as follows. The comparators assigned to the pixels with low illumination power (higher V_{sense}) are active during a short time and consume little energy. Whereas the comparators with pixels with higher illumination power (lower V_{sense}) are active for a longer time and, therefore, consume more energy. In a long

sequence of image frames, the count of light and dark pixels is similar, and, therefore, the power consumption of the entire array of pixels is reduced only by 50%.

This paper proposes a new solution for a dynamic CMOS analog comparator, which changes its state only once during a single A/D conversion in a slope ADC. As a result, power consumption of the comparator is about 2–3 orders smaller than in the conventional continuous and dynamic comparators. Furthermore, the proposed comparator meets the remaining requirements imposed on the in-pixel implementation, namely simplicity, small surface area, and no need for power-down mechanism. The paper presents different versions of the comparator, differing in terms of resolution and power consumption. For all circuit implementations in 0.18-μm CMOS technology from AMS, detailed simulations have been carried out under a power supply voltage of 1.8 and 1V, respectively. A detailed comparison of the proposed comparator with two other conventional comparators is also given.

2 Proposed Ultra-Low-Energy Analog Comparator

In the following Sects. 2.1–2.8, the operation principle of the proposed comparator is explained and its main electrical parameters are analyzed in detail.

2.1 Principle of Operation

Schematics of the proposed dynamic comparator in two-, three-, and four-stage versions are shown in Fig. 3a–c. The consecutive versions differ in resolution and energy consumption per state transition. The first stage of the comparator consists of an n-channel transistor (M_{comp}) and a p-channel transistor (M_2). The transistor M_{comp} is the main device which compares V_{sense} with V_{ramp}. The M_2 is to precharge the parasitic capacitance C_1 to the voltage V_{DD}. The consecutive gain stages are composed of dynamic inverters with parasitic capacitances C_1, C_2, and C_3 at their outputs. The capacitance loading the comparator output is denoted as C_{load}.

The comparator operating principle is as follows. Let us assume that the voltage V_{sense} is in between 0 V and V_{DD}. The initial value of V_{ramp} is V_{DD}, and, therefore, M_{comp} is switched off. The capacitances C_1 and C_3 are initially precharged to V_{DD} by the pulse of $\overline{RST}$, and the capacitances C_2 and C_{load} are discharged to 0 V by RST. The A/D conversion is initialized and V_{ramp} starts falling from V_{DD} to 0 V in a period T_{ramp}. When the falling ramp descends below

$$V_{ramp}(t) \approx V_{sense} - V_{TH} \tag{1}$$

where V_{TH} is the threshold voltage of M_{comp}, M_{comp} starts conducting the current which discharges C_1. The voltage change on C_1 is amplified by the consecutive inverters. As a result, the comparator output voltage V_{out} changes at high speed.

Energy consumption of the comparator during its state transition is associated only with recharging the parasitic capacitances and can be given by:

$$E_{comp} = (C_1 + C_2 + \ldots + C_{load}) \cdot V_{DD}^2 \tag{2}$$
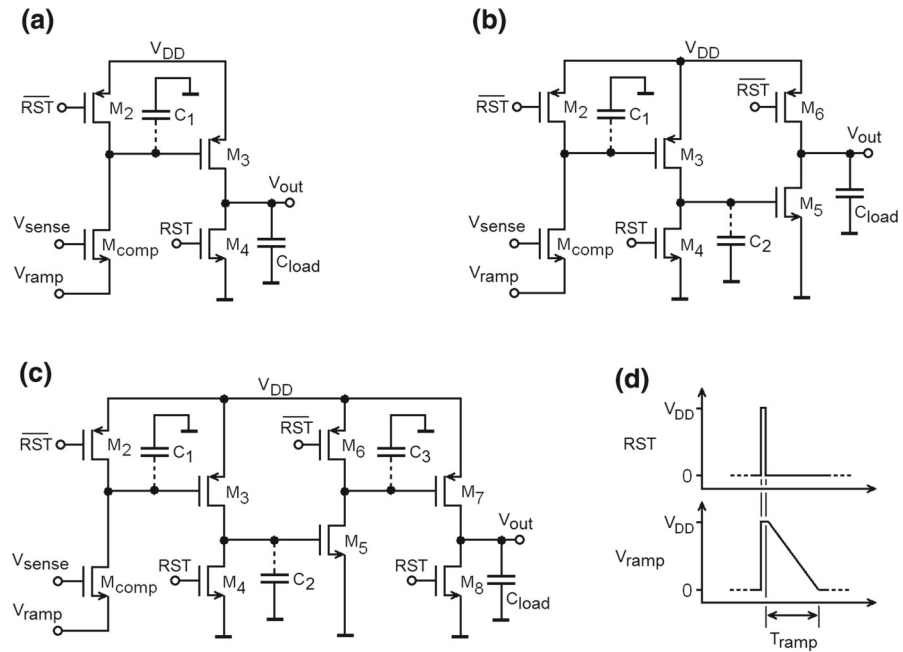
Fig. 3 Proposed ultra-low-energy analog comparator for slope ADC: **a** two-stage, **b** three-stage, **c** four-stage, **d** timing diagrams

As explained above, the proposed comparator changes its state only once for the entire period T_{ramp}. Consequently, the total energy consumed by the comparator in a single A/D conversion is equal to that given by (2).

It should also be noted that the ramp generator, even though it is connected to a source node of the transistor M_{comp}, is always loaded by a high impedance (Z_{ramp}) approximately equal to a series connection of the channel resistance (r_{ds}) of M_{comp} and the parasite capacitance C_1, i.e., $Z_{ramp} \approx r_{ds} + 1/j\omega C_1$. The r_{ds} varies widely within the ramp duration time (M_{comp} is off and on), but Z_{ramp} is always not lower than $1/j\omega C_1$. The ramp generator requires a buffer to drive only a capacitive load. The classical realization of such buffer, for example operational transconductance amplifier (OTA) with closed feedback loop, can be applied.

As explained before (Fig. 1b), the analog comparator in a slope ADC acts as a voltage-to-time converter, which translates V_{sense} to a pulse duration time (T_{out}). With the origin of the time axis aligned with the start of the ramp signal, the comparator voltage-to-time conversion can be determined, taking (1) into account, as:

$$T_{out}(V_{sense}) = \frac{T_{ramp}}{V_{DD}} \cdot (V_{sense} - V_{TH})$$
$$\text{for } V_{TH} < V_{sense} < V_{DD} \text{ and } 0 < V_{ramp} < V_{DD} \tag{3}$$

where V_{ramp} ranges from 0 to the supply voltage V_{DD}, and V_{sense} ranges from V_{TH} to V_{DD}. In modern CMOS technologies, the voltage V_{TH} can be reduced even to 0 V, but

"zero V_{TH}" devices may have too large leakage for this application. In practice, this means that the lowest value of V_{sense} is about 0.2–0.5 V, which is adequate for the use in image sensors, because the voltages below that value are not used in most types of the pixel photosensors [7,9,13].

2.2 Slew Rate and Resolution

The verification of a voltage resolution of dynamic comparators is more difficult compared to continuous-time comparators because the input–output DC characteristic cannot be plotted, and, thus, the voltage gain cannot be easily determined. If we restrict our considerations to the application of this comparator in a slope ADC, where it acts as a voltage-to-time converter, the required resolution of the comparator can be easily determined in the time domain. The comparator controls an N-bit TDC, and, therefore, it must make a decision (make a comparison) during the time interval $T_{ramp}/2^N$. Assuming the comparator output is changing from 0 V to V_{DD}, the required SR should be at least

$$SR > 2^N \cdot V_{DD}/T_{ramp} \qquad (4)$$

For example, for values of $V_{DD} = 1.8$ V, $T_{ramp} = 1$ ms, and 10-bit resolution, the required SR is 1.8 V/µs. This is not challenging because the comparator in the pixel ADC is loaded by a simple digital circuit (latch or gate) with low capacitance of up to tens of the femtofarads (fF). However, the SR depends not only on the load capacitance but also on the amplitude and the slope of an input signal. For a sufficiently large amplitude (e.g., 0-V_{DD}) and a slope (e.g., 100 V/µs) of V_{ramp}, the comparators in Fig. 3 reach a SR of hundreds of volts per microsecond. However, in a real-pixel ADC [13], the comparator is stimulated by V_{ramp} of large amplitude (0-V_{DD}) but with a relatively small slope (e.g., 1.8 V/ms). Under such conditions, the actual SR of the comparator may be multiple times lower as compared to its maximum possible because of insufficient voltage gain of this comparator. Moreover, some further reduction of SR and resolution of the comparators from Fig. 3 can be caused by the transistor leakage and subthreshold currents. This effect will be discussed in the following Sect. 2.3.

2.3 Optimization of Leakage, Slew Rate, and Resolution

The A/D processing time for a single pixel as long as 1 ms is sufficient for parallel architecture of the pixels array as in Fig. 1a operating at a rate of up to 1000 frames per second. Given the long processing time, the leakage currents (I_{off}) of transistors will result in an undesirable change in initial voltages at the comparator nodes. Since transistors in the subthreshold region show a voltage gain greater than one, even a small change in the initial node voltage, for example at C_1, will be magnified and propagated through all consecutive stages to the output V_{out}. As a result, the signal edges become smooth, as shown in Fig. 4, and SR as well as the comparator resolution becomes reduced which follows from (4).

Fig. 4 Influence of leakage and subthreshold currents on the signal slope at the comparator output
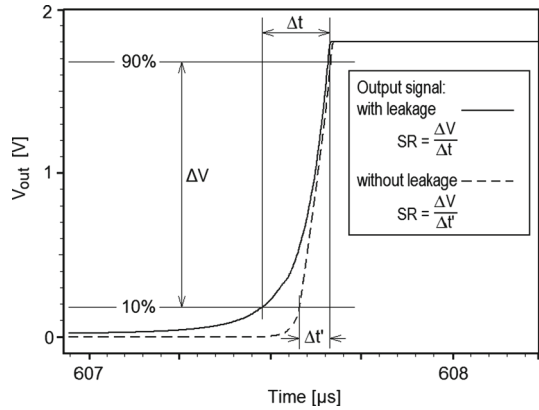
The negative impact of leakage (I_{off}) and subthreshold currents (I_{subth}) can be effectively minimized by properly sizing the transistors and increasing the nodal capacitances C_1, C_2, and C_3.

For the precharge (M_2, M_6) and predischarge (M_4, M_8) transistors, short-channel devices are preferable because nonzero I_{off} of these transistors help to hold initial voltages on the nodal capacitances. Contrary to that, the transistor M_{comp} and the other amplifying transistors (M_3, M_5, M_7) should have longer channels.

Increasing the nodal capacitances simultaneously minimizes the negative impact of I_{off} and I_{subth}. As a result, SR and comparator resolution improve. The propagation time of a comparator may become longer, but no more than a single nanosecond, and therefore, this effect can be omitted for further considerations.

To demonstrate the performance of the new comparator topology, a standard 0.18-µm AMS CMOS technology was chosen and optimization of leakage currents, slew rate, and resolution was carried out. The following working conditions were assumed: processing time $T_{ramp} = 1$ ms, $C_{load} = 50–500$ fF, supply voltage $V_{DD} = 1.0–1.8$ V. In the optimization process, a key priority was to achieve the smallest surface area.

Dimensions of the transistors and the nodal capacitances resulting from the optimization are summarized in Table 1. For all transistors but M_{comp}, a minimum channel width was selected. For M_{comp}, a wider channel was used to limit the device mismatch. The channel lengths were chosen according to indications from above to minimize the impact of leakage. The parasitic nodal capacitances, resulting from p-n source/drain junctions and the gates of transistors, are increased by additional capacitors $C_1 = 20$ fF, $C_2 = 20$ fF and $C_3 = 40$ fF. These capacitors do not cause a significant increase in topology area because for their implementation small-size transistors are sufficient. For example, a capacitance of 20 fF can be implemented using the transistor of about 1.5 by 1.5 µm.

2.4 Simulation Results of Slew Rate and Resolution

The maximum SR value for all comparators from Fig. 3 is independent of the number of amplifying stages because it is determined by the current efficiency of the last stage.

Table 1 Transistor dimensions (in μm/μm) and capacitor values in the comparators from Fig. 3

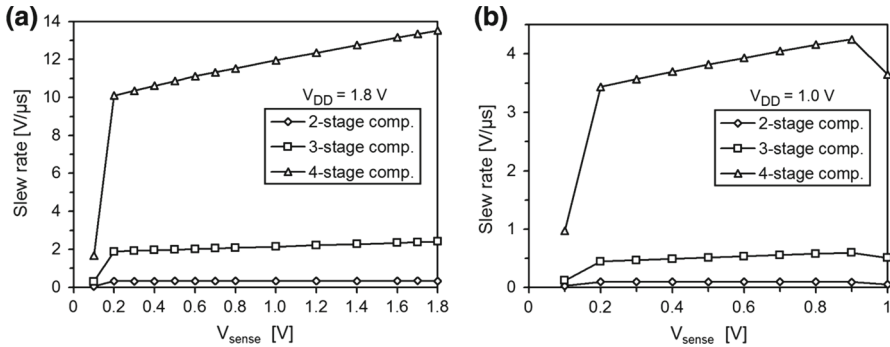| Main transistor	Precharge/predischarge transistors		Amplifying transistors		Additional capacitors			Load capacitance
M_{comp}	p-channel M_2, M_6	n-channel M_4, M_8	n-channel M_5	p-channel M_3, M_7	C_1	C_2	C_3	C_{load}
0.36/0.36	0.22/0.18	0.22/0.18	0.22/0.36	0.22/0.36	20 fF	20 fF	40 fF	50–500 fF

Fig. 5 Slew rate of the comparators from Fig. 3 versus V_{sense} for a supply voltage of 1.8 V (**a**) and 1 V (**b**). Operating conditions: C_{load} = 50 fF, T_{ramp} = 1 ms
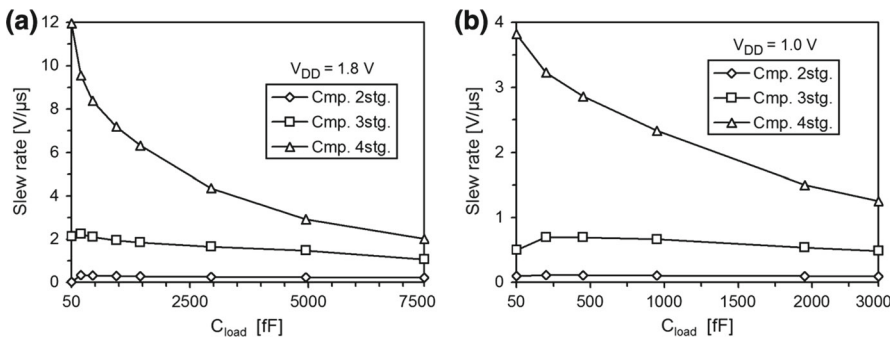

Fig. 6 Slew rate of the comparators from Fig. 3 versus C_{load} for a supply voltage of 1.8 V (**a**) and 1 V (**b**). Operating conditions: T_{ramp} = 1 ms and V_{sense} = 1 V for (**a**), T_{ramp} = 1 ms and V_{sense} = 0.5 V for (**b**)

The maximum value of SR obtained from simulations, while driven by a ramp with a short fall time T_{ramp} = 10 ns, was 300 V/μs for two- and four-stage comparators, and over 800 V/μs for the three-stage comparator. The highest value of SR for three-stage comparator results from the fact that n-channel transistor is in the output stage.

When the ramp fall time is considerably longer, for example T_{ramp} = 1 ms, the SR of the comparators decreases because it is limited by their voltage gain. Under these conditions, the best results are obtained for the four-stage comparator (12 V/μs) followed by the three-stage (2 V/μs) and the two-stage versions (0.3 V/μs). Taking into account the achieved SR values, the expected resolution of the comparators is 7, 10, and 12.5 bits for two-, three-, and four-stage implementations, respectively. These values, in turn, correspond to the input voltage resolution of 11 mV, 1.5 mV, and 0.3 mV for the full-scale operation range of 0–1.8 V. For a supply voltage reduced to 1 V, the resolution decreases to 6, 8.5, and 11 bits, respectively. The detailed plots of the simulated SR as a function of V_{sense} for the selected supply voltages are shown in Fig. 5.

The proposed comparator can be used not only in a pixel ADC, but also for C_{load} larger than typical 50 fF. Simulations indicate that the SR decreases for the larger C_{load}. The corresponding SR plots are presented in Fig. 6. This effect is stronger for
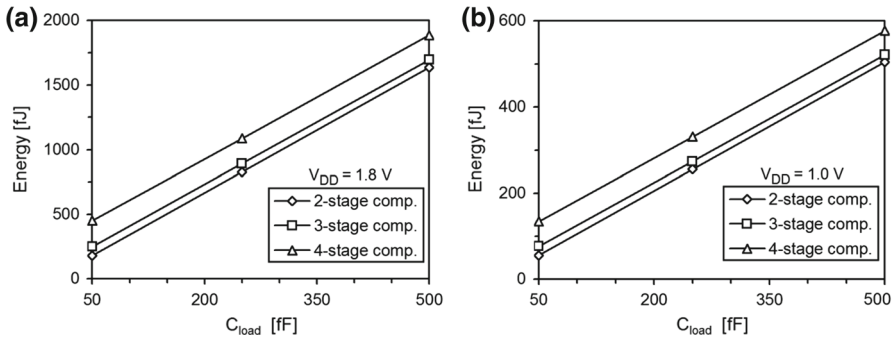
Fig. 7 Energy consumption for the comparators from Fig. 3 during a state transition versus C_{load} for a supply voltage of 1.8 V (**a**) and 1 V (**b**). Operating conditions: $V_{sense} = 1$ and 0.5 V for $V_{DD} = 1.8$ and 1 V, respectively

the four-stage comparator because its SR is not limited by the voltage gain but by its current efficiency. To drive the larger capacitance, the transistor in the output stage (M_7) should be widened. For example, to drive C_{load} of up to 3 pF, the width of M_7 should be increased from 0.22 to 1 μm.

2.5 Simulation Results of Energy Consumption

The energy required to change the comparator state in all three versions with C_{load} of 50 fF is below 0.5 pJ. This energy corresponds to a power dissipation of 0.5 nW for $T_{ramp} = 1$ ms. The exact values of energy obtained from simulations are 180, 250, and 450 fJ for the two-, three-, and four-stage comparator, respectively. In Fig. 7, the detailed plots of the energy consumption as a function of C_{load} for two selected supply voltages are presented. It is worth mentioning that the energy values obtained from the simulations and those calculated with (2) are practically the same.

2.6 The Influence of Body Effect at M_{comp} on the ADC Linearity

Due to the body effect, the threshold voltage of M_{comp} changes during the falling V_{ramp}. The fluctuation of V_{TH} differs for different V_{sense} and results in the nonlinear voltage-to-time characteristic (3). This nonlinearity translates directly to the ADC nonlinearity. Fortunately, this effect is relatively weak. Figure 8a, b shows the voltage-to-time characteristic and its derivative for the three-stage comparator. Its integral nonlinearity (INL) does not exceed 0.7% for an input voltage range of 0.2 V to V_{DD}.

The human eye is not sensitive to nonlinearity of an image sensor in terms of gradient of gray, and, therefore, it is not an issue for most applications. For vision chips, for example, the most important is a high processing efficiency, while image quality is less critical [2,8,15,17,18].

If high linearity is required, then a comparator without the body effect should be used. In such a circuit, the main n-channel transistor, M_{comp}, should be replaced by a
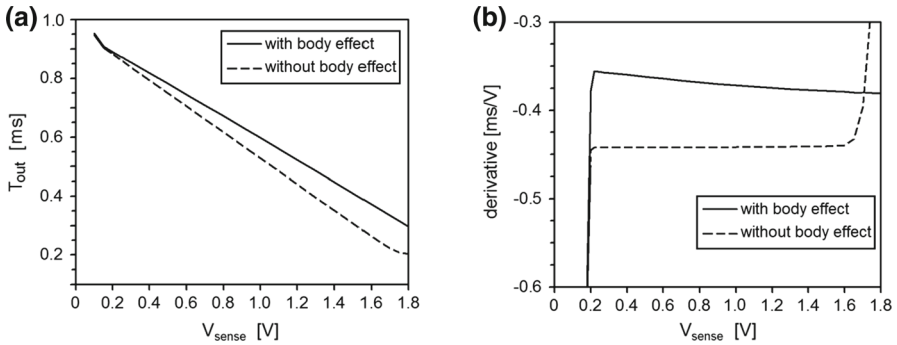
Fig. 8 Voltage-to-time conversion characteristic of the comparator from Fig. 3b (**a**), and its derivative (**b**). The characteristic is plotted with the body effect at M_{comp} (*solid line*) and without the body effect (*dashed line*). Operating conditions: $V_{DD} = 1.8$ V, $T_{ramp} = 1$ ms
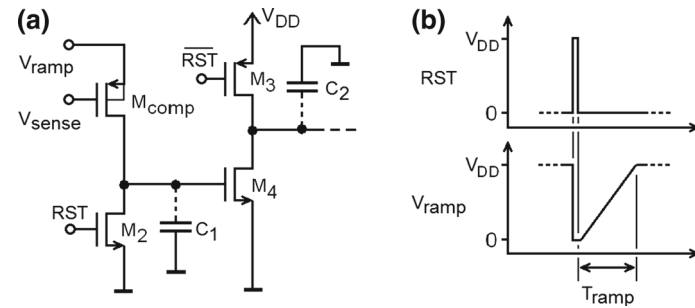

Fig. 9 Input stages of the comparator without the body effect at M_{comp}: **a** circuit diagram, **b** timing diagrams

p-channel device with the substrate connected to the source, and the ramp slope has to be changed from falling to rising, as shown in Fig. 9. In this paper, a *n*-channel version of the comparator with the falling ramp is presented which is more preferred in the image sensor applications. With the falling ramp, the time needed for A/D conversion of a dark signal can be shortened because this signal corresponds to a high voltage V_{sense}. This is important for correlated double sampling (CDS) because it reduces the time interval between signal samples [13].

2.7 Random Input Offset Voltage (V_{os}) and Temporal Noise

A random input offset voltage (V_{os}) of the comparator in a slope ADC from Fig. 1b is one of the factors leading to the lower image quality. Due to a random V_{os}, the ADC conversion characteristic differs from pixel to pixel resulting in an imaging array nonuniformity and fixed pattern noise (FPN).

The largest impact on V_{os} has the mismatch of M_{comp}. In a first-order approximation, V_{os} is equal to a random deviation of the threshold voltage of M_{comp}. Accurate analysis of the mismatch will not be carried out here. Examples of

Table 2 Simulated parameters of the comparators from Fig. 3

	2-stage Fig. 3a	3-stage Fig. 3b	4-stage Fig. 3c
CMOS technology	0.18 µm AMS (austriamicrosystems), standard leakage option		
V_{sense} input range	$0.25V - V_{DD}$		
Input offset voltage:			
non-random built-in offset	≈ 350 mV		
random offset (V_{os})	$\approx \pm 10$ mV (1 sigma)		
Output slew rate (SR) during comparison	0.3 V/µs	2.1 V/µs	12 V/µs
Input resolution[a]	7 bits	10 bits	12.5 bits
	(11 mV)	(1.5 mV)	(0.3 mV)
Energy per comparison	0.18 pJ	0.25 pJ	0.45 pJ
Propagation time	<7 ns	<7 ns	<9 ns
Max. SR, at $T_{ramp} < 10$ ns			
$C_{load} = 50$ fF	300 V/µs	800 V/µs	300 V/µs
$C_{load} = 500$ fF	30 V/µs	120 V/µs	30 V/µs

Operating conditions: $V_{DD} = 1.8$ V, $C_{load} = 50$ fF, $T_{ramp} = 1$ ms
[a] Assuming a full-scale operation range of 0-V_{DD}

such analysis for analog comparators can be found in [6,14]. The estimated value of V_{os} based on the simulations is below ± 10 mV (1 sigma) for all comparators from Fig. 3. The simulations were based on statistical models developed by the technology provider. The temporal noise in a low-frequency range ($1/f$ noise) also results in FPN of an image. Fortunately, FPN related to the V_{os} and $1/f$ noise can be effectively reduced by 1 to 2 orders of magnitude by CDS [12,13].

Temporal noise in a higher-frequency range causes the jitter at a comparator output, which cannot be removed by CDS. For the comparators from Fig. 3, this noise-induced jitter is below ± 0.08 µs (1 sigma) assuming the noise bandwidth of 100 Hz to 10 MHz. Thus, an input-referred noise of the comparators is about 200 µV$_{rms}$. The results are obtained from the time-domain noise analysis (transient noise analysis) in Cadence Spectre simulator.

2.8 Summary of Simulation Results

The major parameters of the comparators from Fig. 3 are summarized in Table 2. They are determined for typical operating conditions: a supply voltage of 1.8 V, a capacitance load of 50 fF, and a ramp time of 1 ms. The corresponding parameters for the lower supply voltage and larger C_{load}, together with the comparison to other solutions, are summarized in Table 3.

3 Comparison

The proposed comparator was compared to the classic topologies from Fig. 2a, b. To facilitate this comparison, a specific application was selected. It was assumed that the

Table 3 Comparison of the comparators from Figs. 2 and 3

	Classic continuous-time Fig. 2a	Classic dynamic Fig. 2b	Proposed dynamic		
			2-stage Fig. 3a	3-stage Fig. 3b	4-stage Fig. 3c
Layout area	$\approx$30 μm^2	$\approx$30 μm^2	$\approx$25 μm^2	$\approx$35 μm^2	$\approx$45 μm^2
Transistor dimensions (in $\mu m/\mu m$)	M_1–M_7 0.44/0.36 $I_{bias} = 50$ nA	M_1–M_2 0.44/0.36 M_3–M_8 0.22/0.18 M_9–M_{10} 0.44/0.18	M_{comp} 0.36/0.36 M_2, M_4, M_6, M_8 0.22/0.18 M_3, M_5, M_7 0.22/0.36		
Clock-induced kickback noise[a]	n.a.	6 mV (max. amplitude)	n.a.		
Random input offset voltage V_{os} (1 sigma)	13 mV		10 mV		
Supply $V_{DD} = 1.8$ V					
V_{sense} input range	0.35–1.75 V	0.45–1.79 V	0.25–1.8 V	0.25–1.8 V	0.25–1.8 V
Output slew rate (SR)					
With $C_{load} = 50$ fF	2.05 V/μs	500 V/μs	0.3 V/μs	2.1 V/μs	12 V/μs
With $C_{load} = 500$ fF	1.25 V/μs	85 V/μs	0.3 V/μs	2.1 V/μs	8.4 V/μs
Energy per A/D conversion					
With $C_{load} = 50$ fF	140 pJ	190 pJ	0.18 pJ	0.25 pJ	0.45 pJ
with $C_{load} = 500$ fF	140 pJ	1900 pJ	1.6 pJ	1.7 pJ	2 pJ
Supply $V_{DD} = 1.0$ V					
V_{sense} input range	0.35–0.9 V	0.45–0.99 V	0.25–0.95 V	0.25–1.0 V	0.25–1.0 V
Output slew rate (SR)					
With $C_{load} = 50$ fF	0.9 V/μs	170 V/μs	0.1 V/μs	0.7 V/μs	3.8 V/μs
With $C_{load} = 500$ fF	0.5 V/μs	Overloaded	0.1 V/μs	0.5 V/μs	2.8 V/μs
Energy per A/D conversion					
With $C_{load} = 50$ fF	60 pJ	50 pJ	0.05 pJ	0.08 pJ	0.14 pJ
With $C_{load} = 500$ fF	60 pJ	–	0.5 pJ	0.52 pJ	0.58 pJ

[a] Measured on a node V_{sense} on the assumption that the capacitance of a photosensor is 10 fF

comparators are to be applied in an ADC with a resolution N of 10 bits, performing one thousand A/D conversions per second (i.e., $T_{ramp} = 1$ ms). For the chosen set of specifications, the required SR for the comparators from Figs. 3a–c to 2a can be determined using (4). From (4), it follows that SR $> 1 \cdot V_{DD}$ [V/μs]. The requirements for the comparator from Fig. 2b are slightly different because this topology must sample the ramp signal at a speed of at least 1 Msample/s (i.e., the frequency on the node "clk" should be at least 1 MHz). This comparator changes its state twice (latch and regeneration) in 1 μs. As a result, the output SR must be doubled, i.e., SR $> 2 \cdot V_{DD}$ [V/μs].

For both classic comparators from Fig. 2, optimization of the slew rate and energy consumption was carried out, analogously to that previously done for the proposed comparators. Dimensions of the transistors were chosen such to result in a similar chip surface for all topologies. For the continuous-time comparator, the bias current I_{bias} was set to 50 nA. The most important simulated parameters of all comparators are summarized in Table 3.

The highest SR value was obtained for the dynamic comparator from Fig. 2b. Its SR is 1–2 orders of magnitude higher compared to other comparators due to the built-in positive feedback. However, with the supply reduced to 1 V and for C_{load} increased to 500 fF, its SR drops drastically and the comparator is not able to operate with the required clock frequency of 1 MHz. The continuous-time comparator from Fig. 2a also does not maintain the required speed because its SR falls below the required value 1 V/μs. With the reduced supply voltage and increased load, only the four-stage comparator from Fig. 3c preserves the desired SR.

As opposed to the classical comparators, the proposed topologies allow wider operation range for V_{sense}, specifically for the lower-end values.

With regard to energy consumption per single conversion cycle of a slope ADC, the proposed comparators outperform their classical counterparts. They require 500 times less energy on average than the other comparators. It should be noted that the classical two-stage dynamic comparator from Fig. 2b requires small energy (0.19 pJ) per single-state transition. This amount is similar to the energy consumed by the proposed two-stage comparator from Fig. 3a which is 0.18 pJ. However, the classical comparator must change its state 1000 times during a single A/D conversion cycle resulting in a total energy consumption of 190 pJ, which is similar to that obtained for the continuous-time comparator (140 pJ).

4 Conclusions

The proposed comparator shows a set of properties adequate for applications in CMOS image sensors, such as low energy consumption (0.5 pJ), small area (25–45 μm^2), wide range of input voltage (0.2–1.8 V), and simple design requiring no bias signals or additional power-down mechanisms. In contrast to conventional solutions, the proposed comparator can operate at a supply voltage (1 V) reduced to almost half of its nominal value (1.8 V). This feature makes it attractive also for applications other than image sensors, especially for low-voltage and low-power systems.

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